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Study of the baby-moss @ L268

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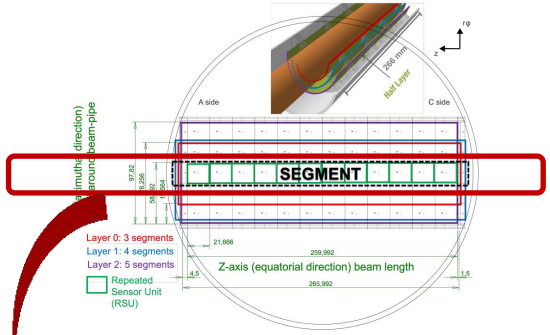
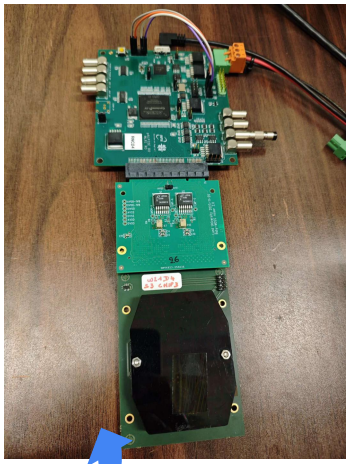
Babymoss - from ALICE ITS report



CMOS wafer



Babymoss

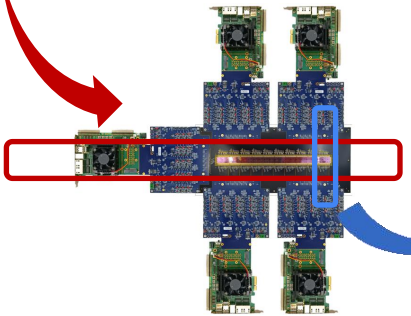
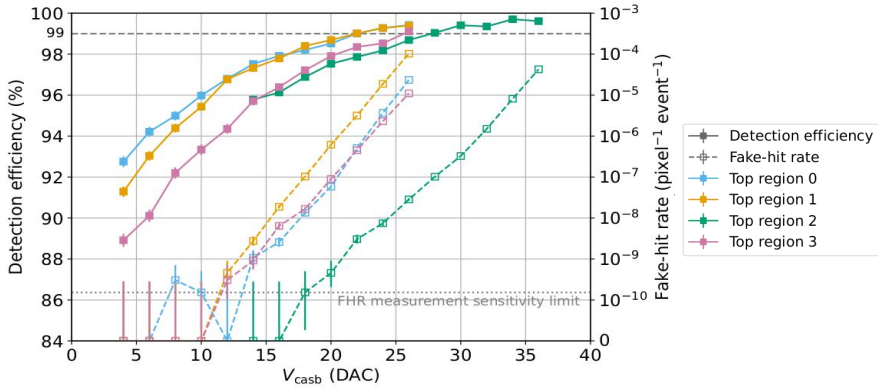


Figure 3.27: Photograph of the MOSS test system.

MOSS



small design differences in each region

	Region 0	Region 1	Region 2	Region 3
TOP	Standard	Larger input transistor (M1)	Larger discriminator input transistor (M11)	Larger common-source transistor (M2)
BOTTOM	Standard	Standard	Standard	Slightly different layout

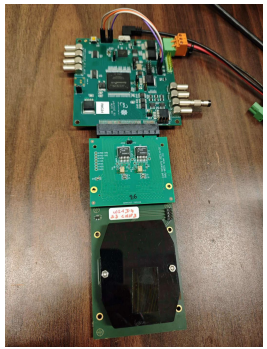
ALICE, Technical Design Report of the ITS Upgrade, page 40, Fig. 3.30; page 46, Fig. 3.33

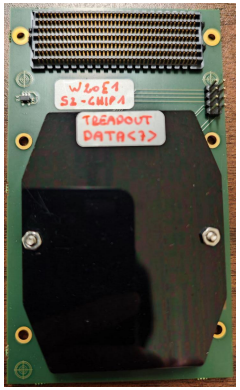
Default setups

DAC units:

IBIAS = 62
IBIASN = 100
IDB = 50
IRESET = 10
VCASB = 15
VCASN = 64
VSHIFT = 192

A. W21D4 S3 CHIP3
B. W20E1 S2 CHIP1
C. W20E1 S2 CHIP3





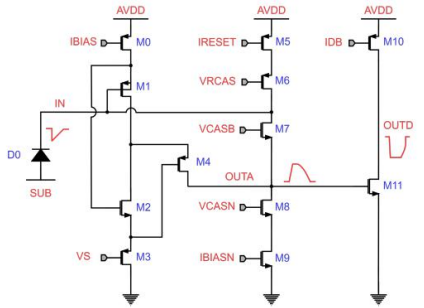


Figure 3.40: Simplified schematic of the pixel front-end amplifier and discrimination sections.

Short term target:

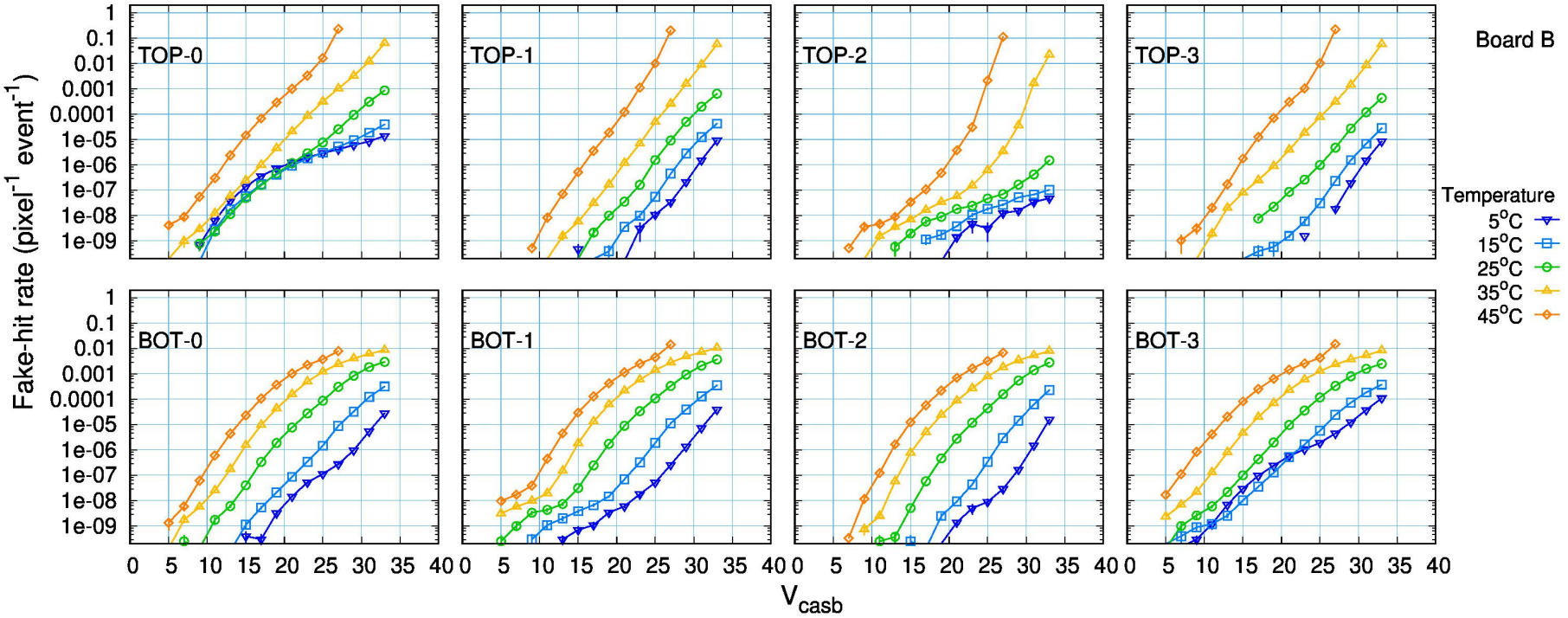
- Understand the performance of the baby-moss under different configures (Vcasb dependence..)
- The temperature dependence of the noise level
- The performance after the radiation expose

Temperature test with climatic chamber

- Take 5~10 mins to heat/cool the climatic chamber (change ~10°C)
- Scan 5°C, 15°C, 25°C, 35°C, 45°C with different V_{casb}
- 50k~100k events for each configuration, ~3h for the V_{casb} scan at each temperature

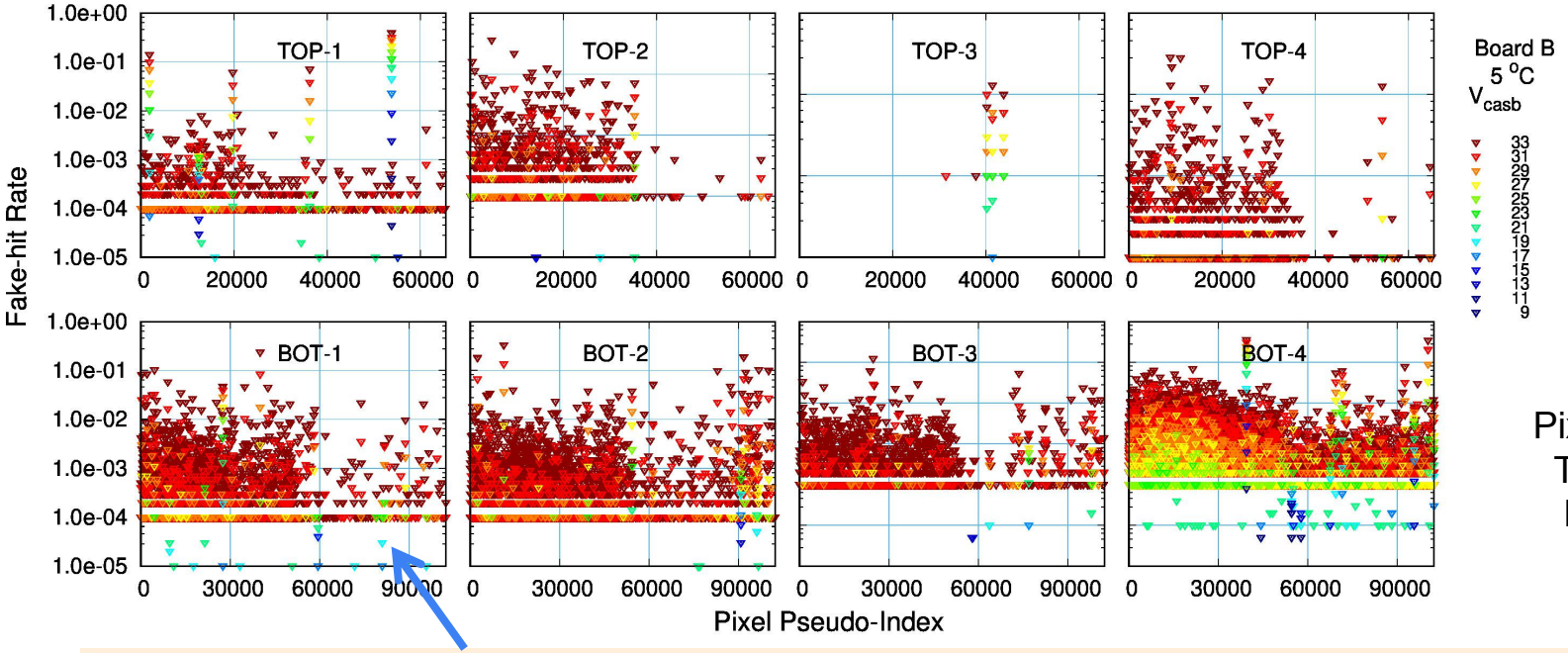
- Set the chamber temperature near the room temperature - relative unstable (±1°C), otherwise (± 0.5°C)

FHR vs V_{casb} @ different T



- lower temperature gives the lower Fake-Hit Rate (FHR)

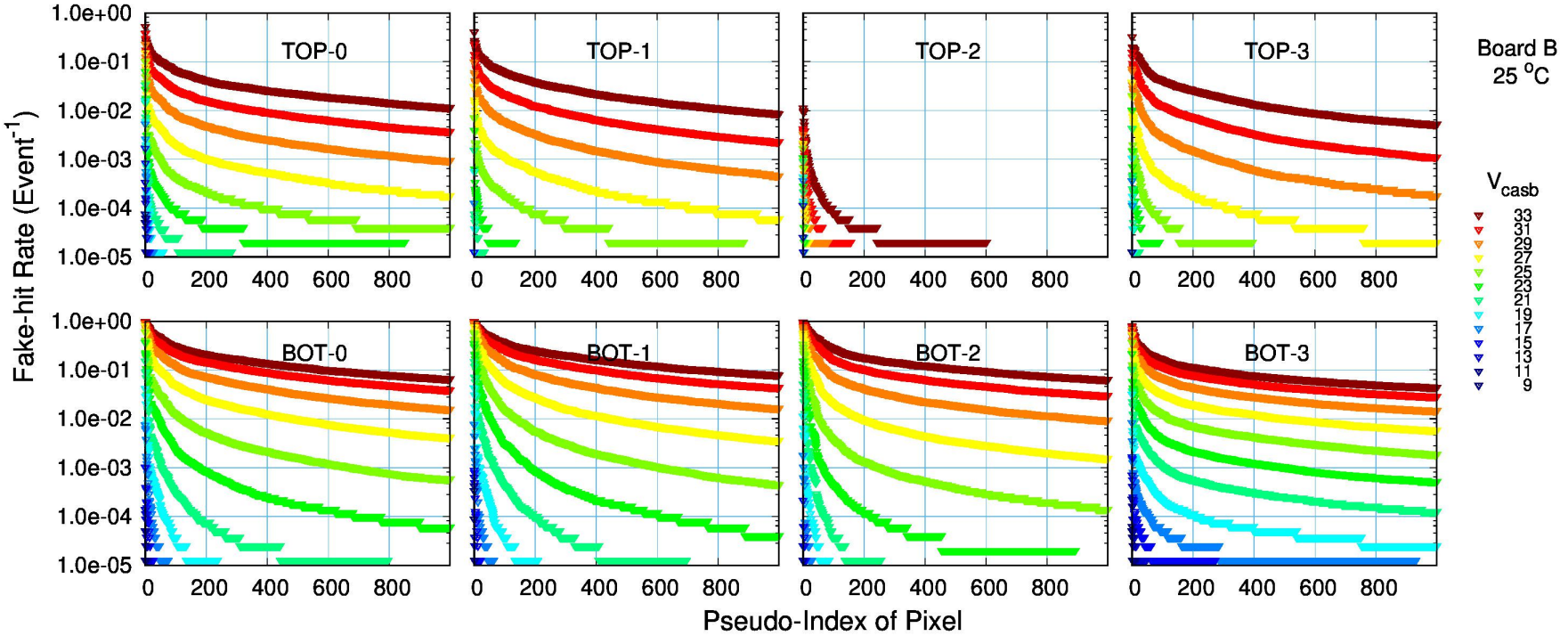
Where are the hot pixels?



Pixels:
Top: 256x256
Bot: 320x320

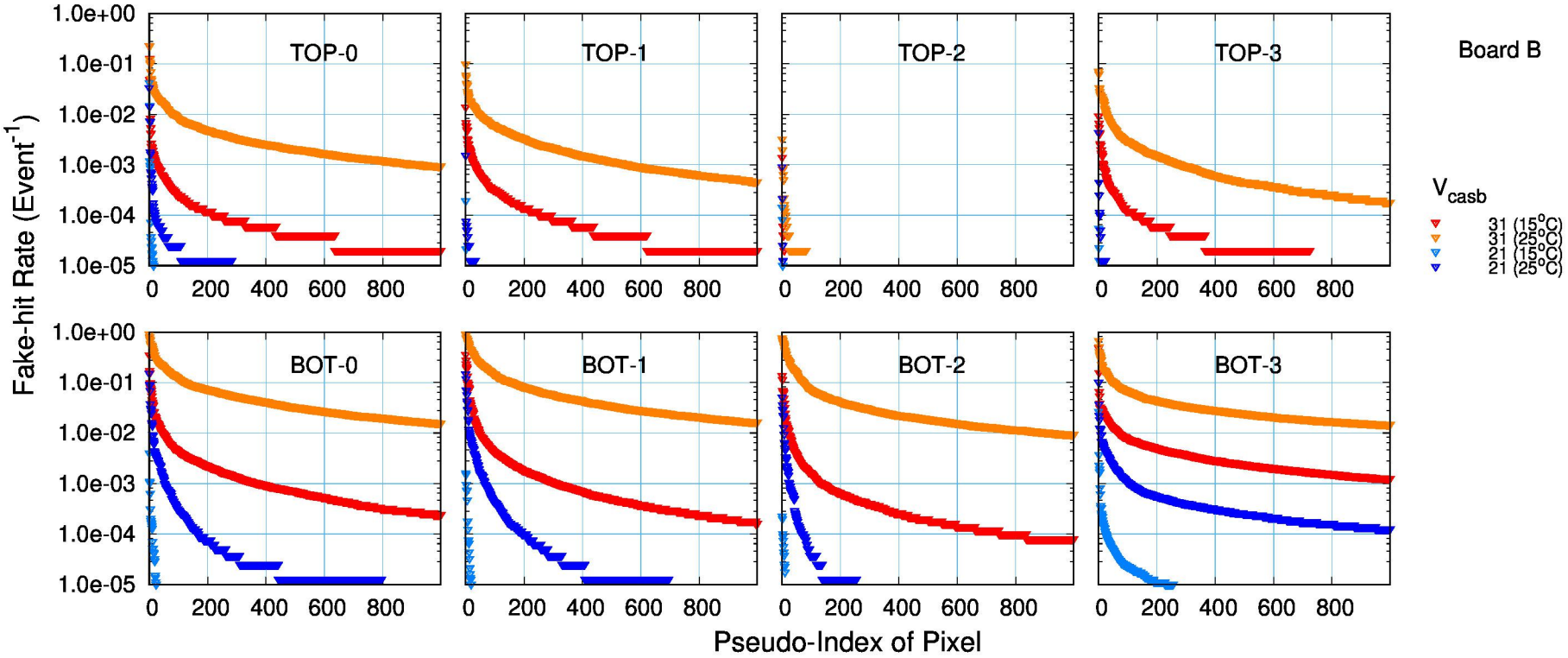
- 2D hit map are very random, so shown a Psedo-index vs FHR (eg. Index = X*256+Y)
- Some of the pixels are fired every time, which should be masked out
- Most of the pixels are random fired

FHR vs Pixel Index @ 25 C

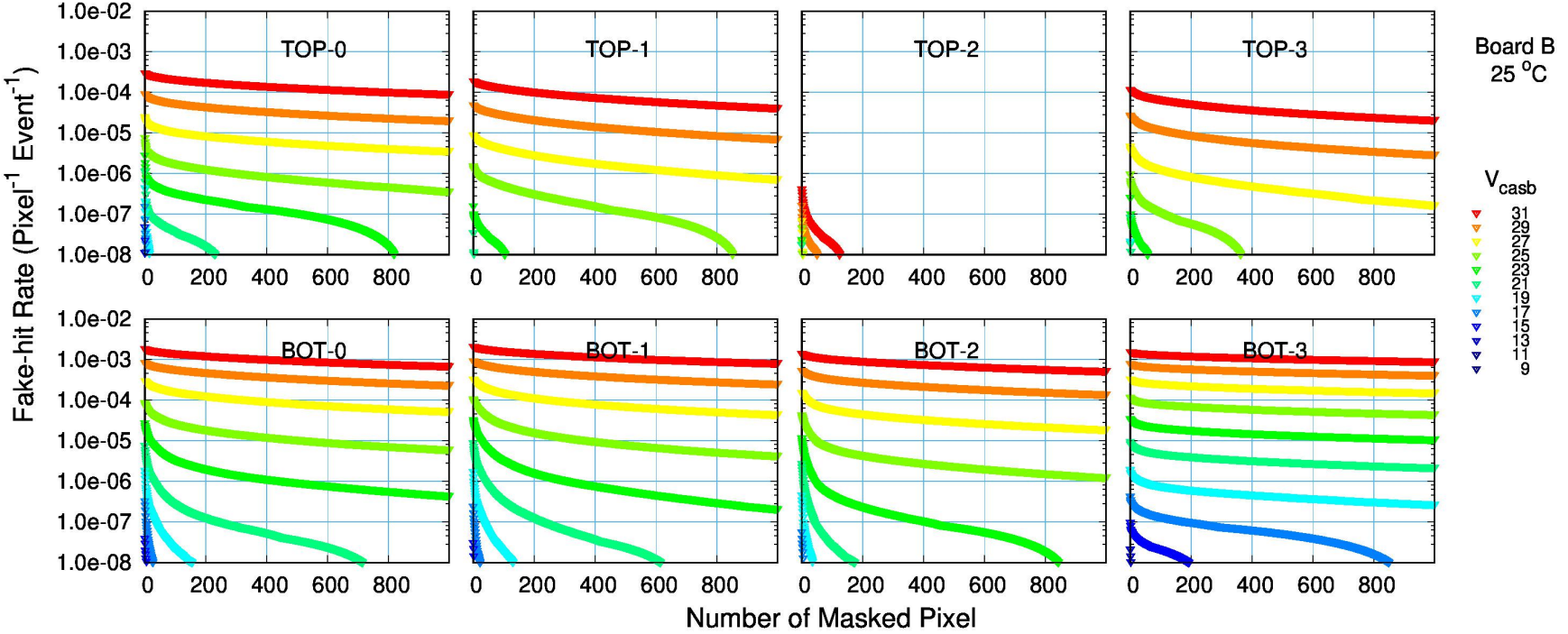


- In total: TOP: 256x256=65536 Pixels; BOT: 320x320=102400 Pixels
- Reorder all the Psedo-index form high to low, and plot it vs FHR

FHR vs Pixel Index @ different T



FHR vs Number of Masked Pixels



- FHR as a function of number of masked Pixels

Summary and Outlook

- We studied the FHR at different temperatures with different Vcasb
- Calibrated the on board thermistor (- last presentation)
- We will build the cooling loop by ourselves for the future beam test, study the performance of the cooling loop

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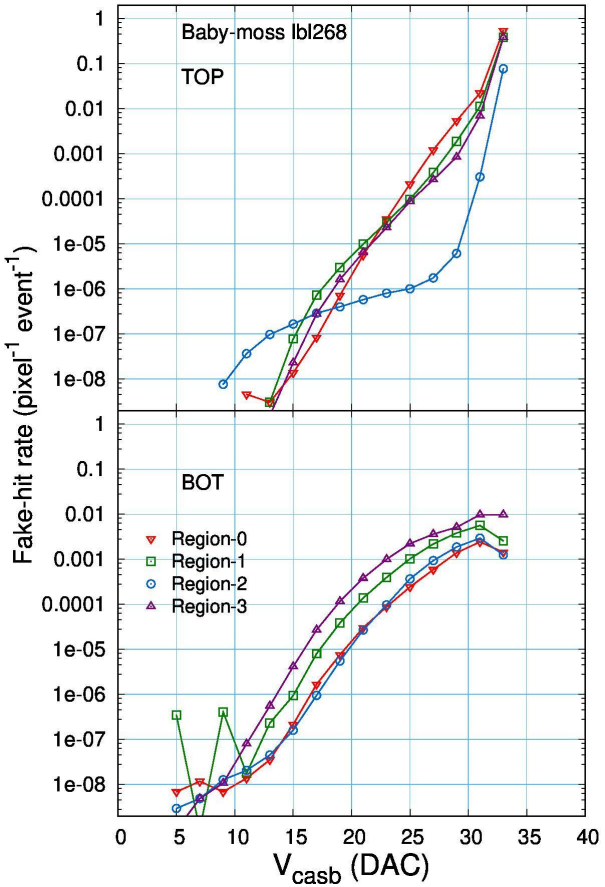
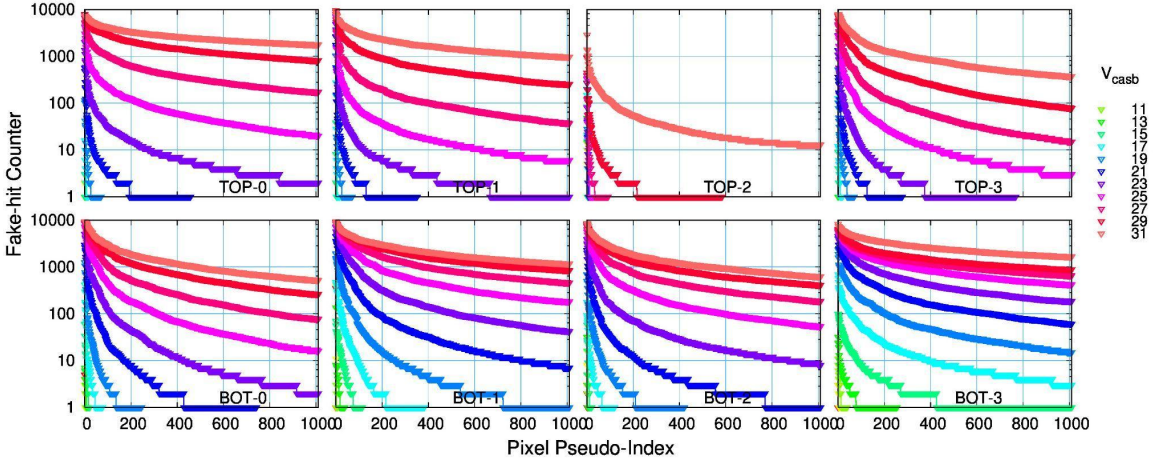
Materials from the last presentation

Board A - **W21D4 S3 CHIP3** (20240906) - 10k events



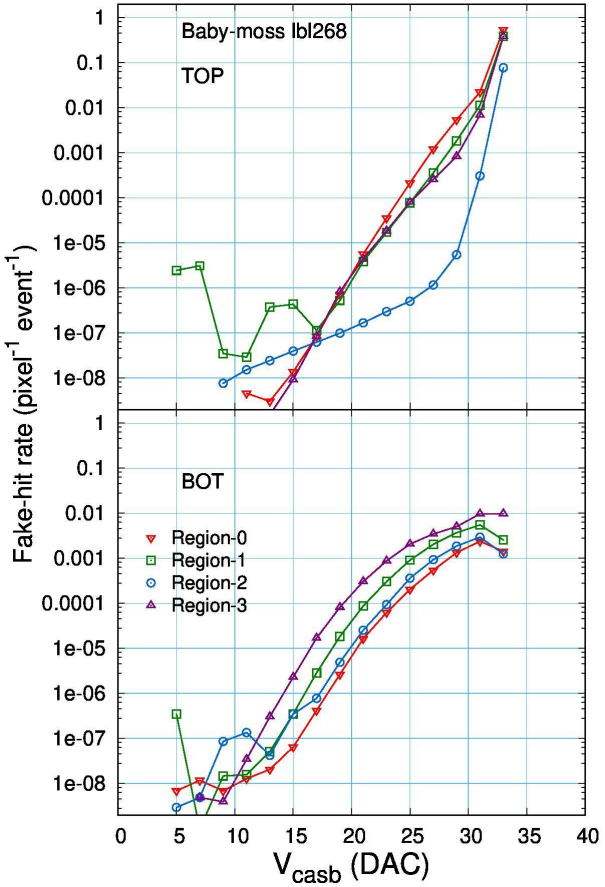


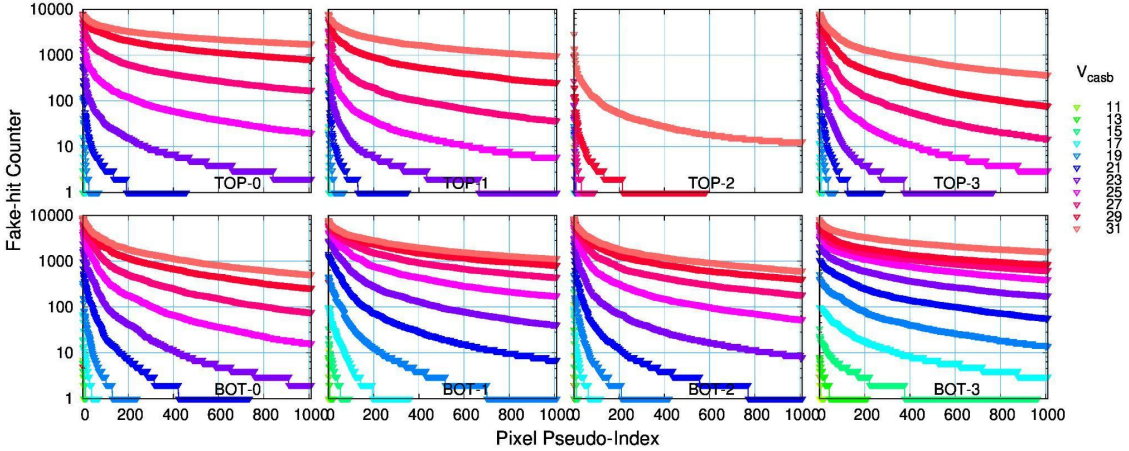
Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=15

Masked pixels

	R-0	R-1	R-2	R-3
TOP	5	6	4	0
BOT	3	12	6	20

Board A - **W21D4 S3 CHIP3** (20240906) - 10k events





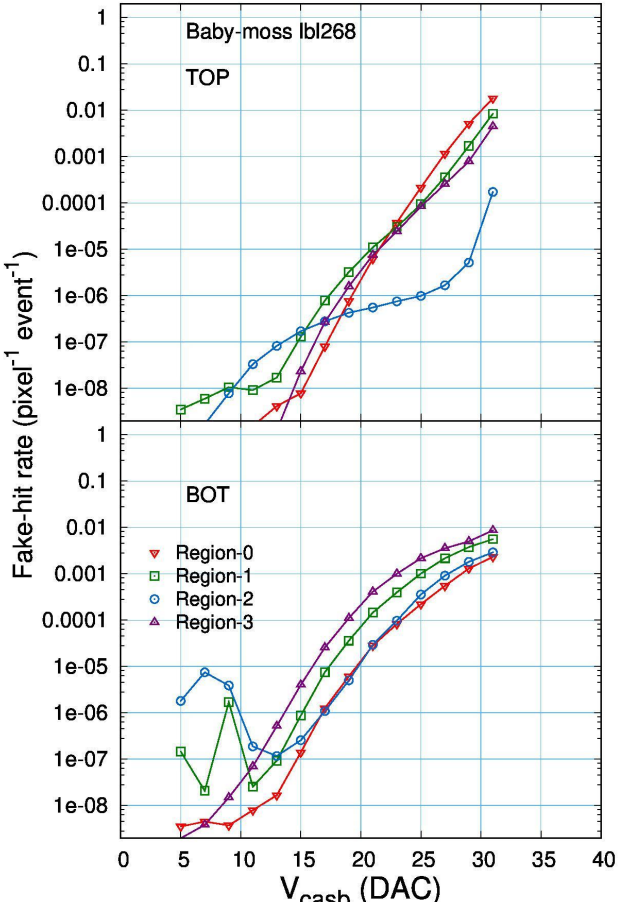
Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=17

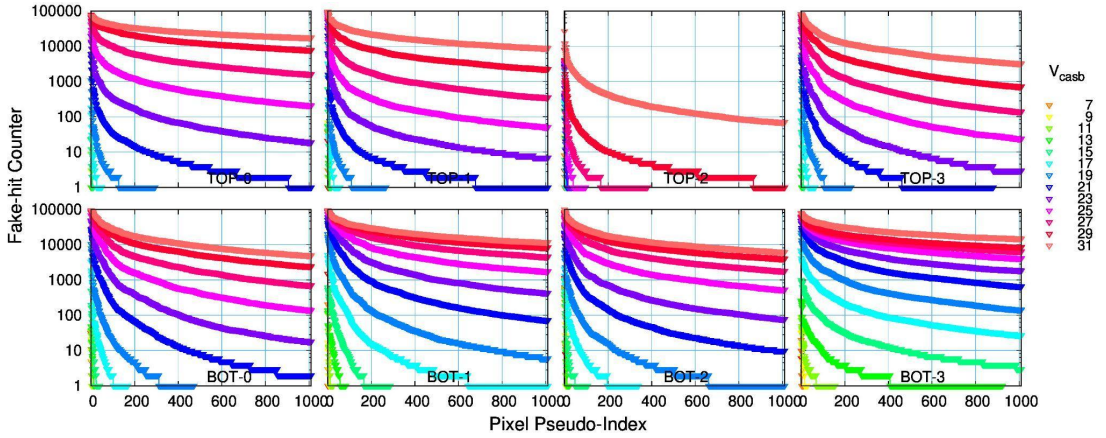
Masked pixels

	R-0	R-1	R-2	R-3
TOP	5	7	5	1
BOT	9	34	6	69

No significant different with mask @ V_{casb}=15 and V_{casb}=17

Board A - **W21D4 S3 CHIP3** (20240918) - 100k events



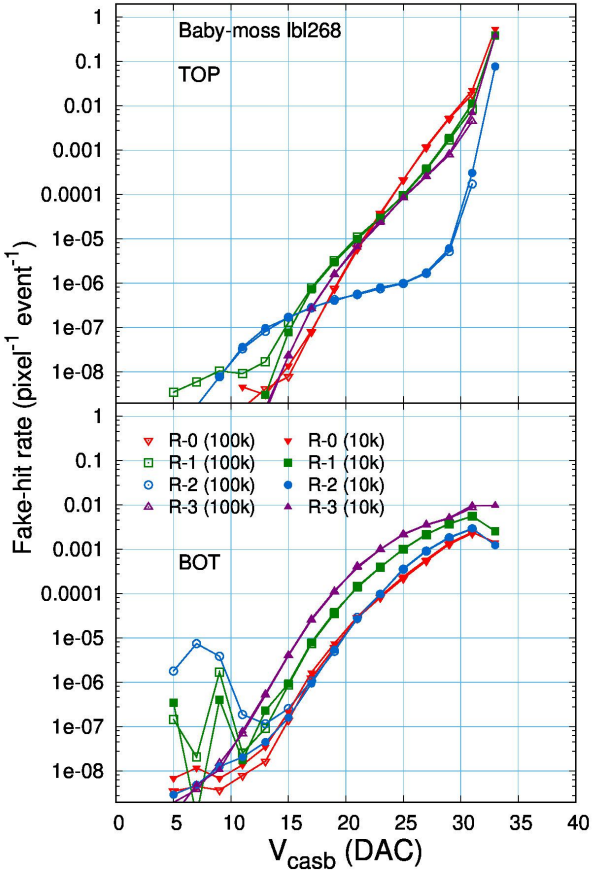


Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=15

Masked pixels

	R-0	R-1	R-2	R-3
TOP	4	5	3	0
BOT	6	13	6	18

10k vs 100k



10k

Masked pixels

	R-0	R-1	R-2	R-3
TOP	5	6	4	0
BOT	3	12	6	20

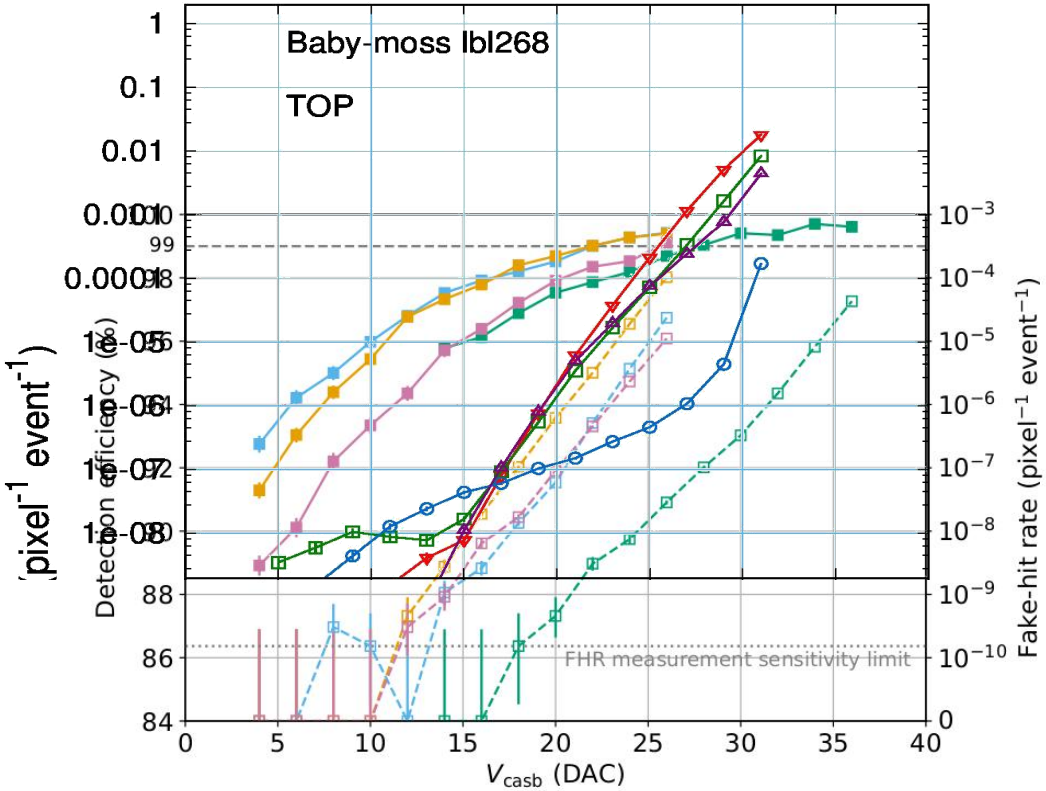
100k

Masked pixels

	R-0	R-1	R-2	R-3
TOP	4	5	3	0
BOT	6	13	6	18

- No significant difference with 10k or 100k events
- 10k should be sufficient enough for this test

Layer-over comparison with ALICE tests



ITS report
- Top region 0
- Top region 1
- Top region 2
- Top region 3

Baby-moss A
- Region-0
- Region-1
- Region-2
- Region-3

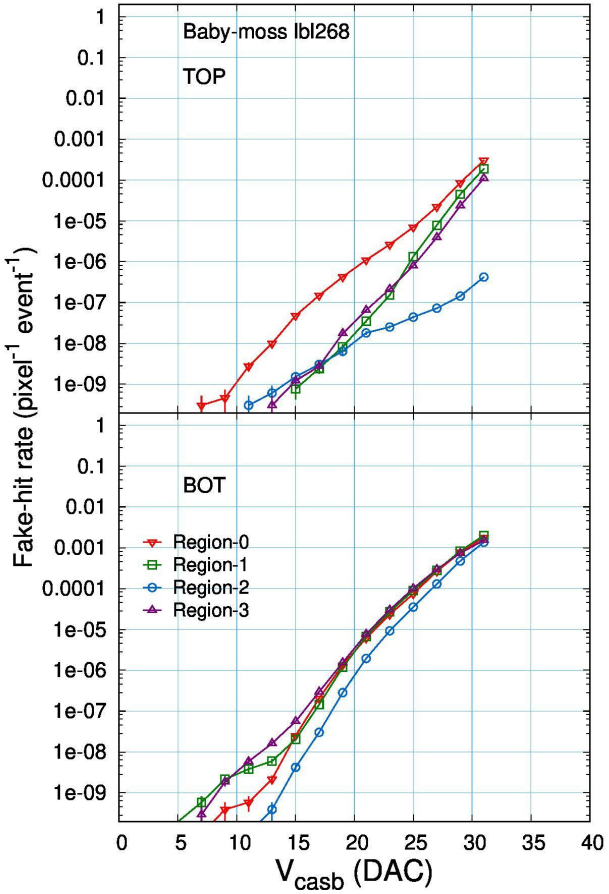
small design differences in each region

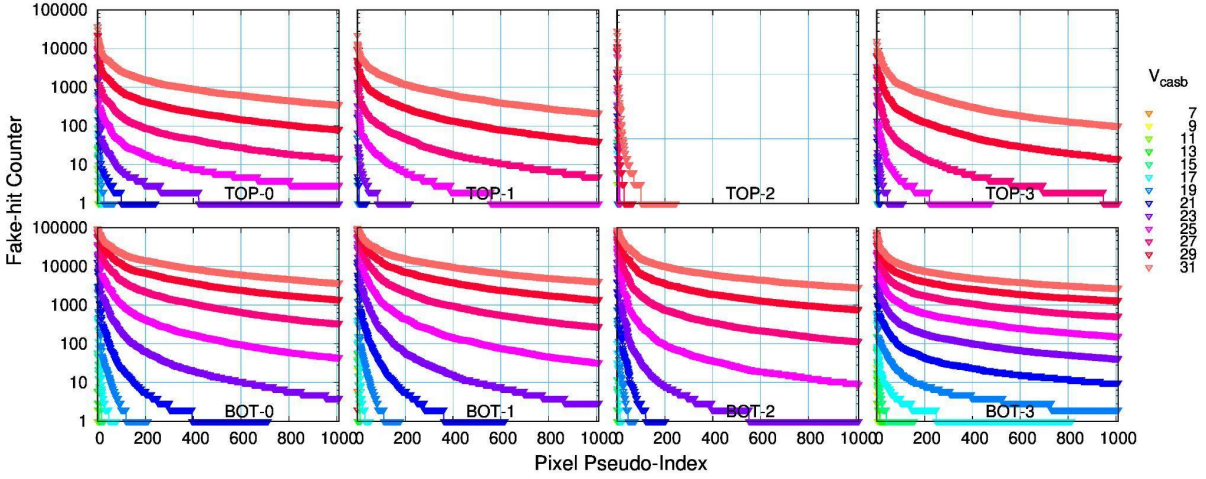
	Region 0	Region 1	Region 2	Region 3
TOP	Standard	Larger input transistor (M1)	Larger discriminator input transistor (M11)	Larger common-source transistor (M2)
BOTTOM	Standard	Standard	Standard	Slightly different layout

- Good consistence for Region-0,1,3
- Some differences for Region-2

Individual differences?

Board B - **W20E1 S2 CHIP1** (20240918) - 100k events



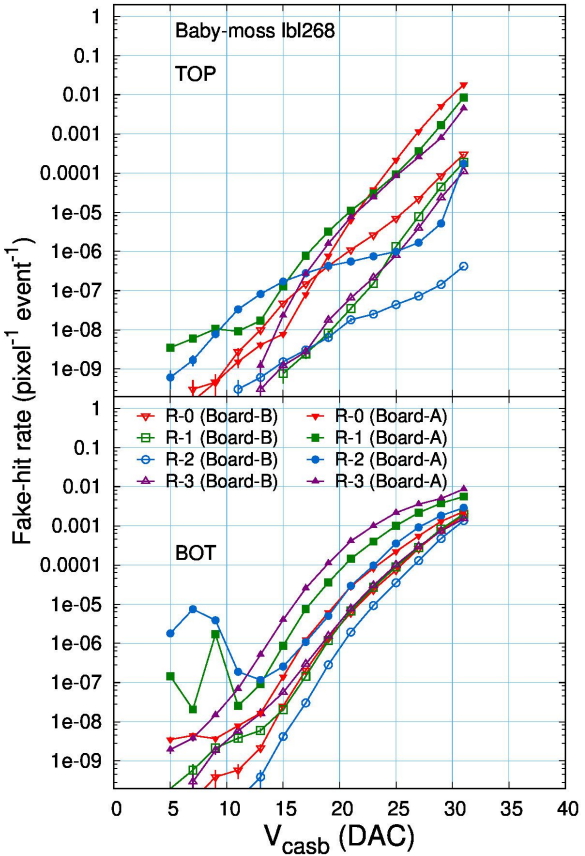


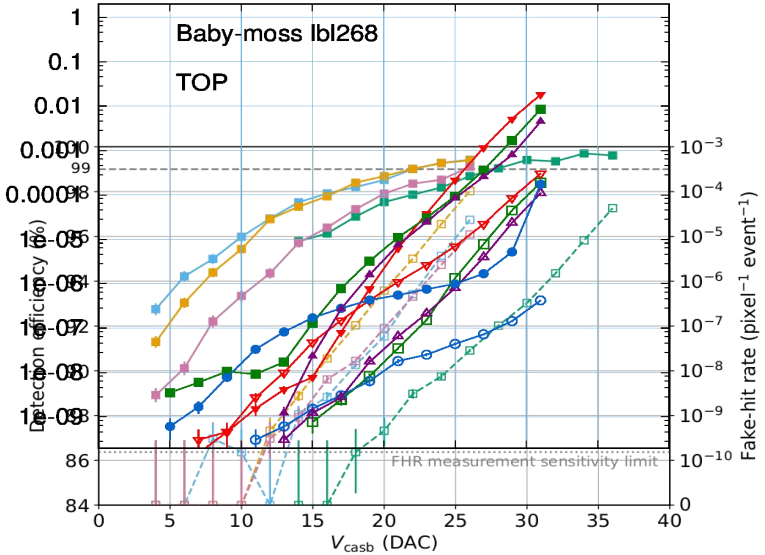
Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=15

Masked pixels

	R-0	R-1	R-2	R-3
TOP	0	0	0	0
BOT	0	0	0	2

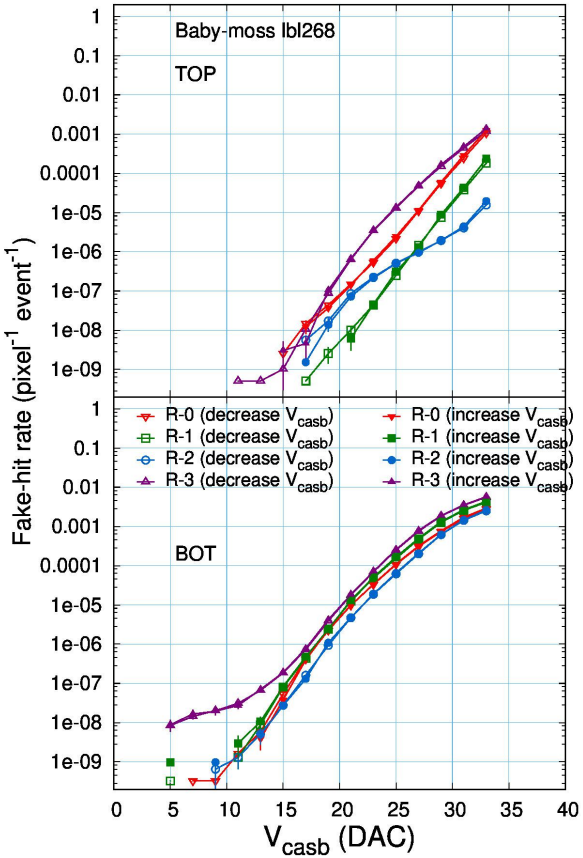
Board-A vs Board-B



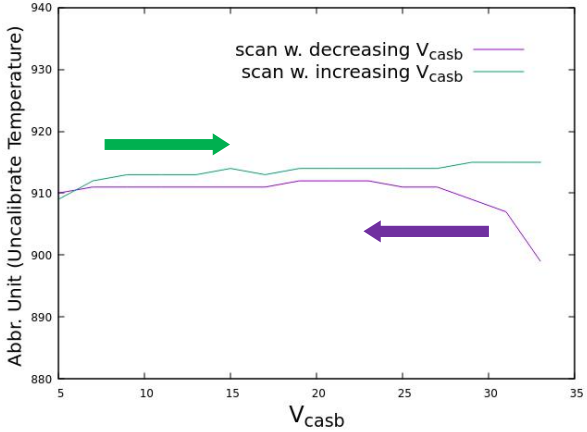


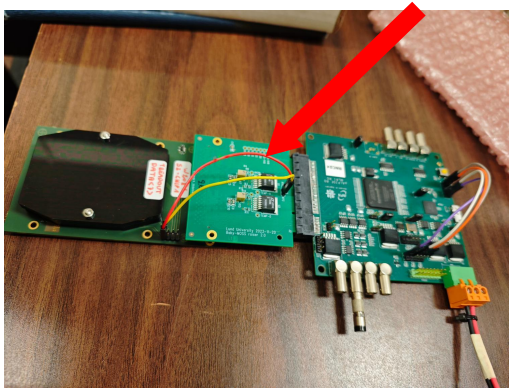
- The performance of individual chips has noticeable differences
- The trend of the Fake-hit rate (also checked Board-C) is consistent with the example in the ALICE ITS report

Order of scaning - w. Board-C



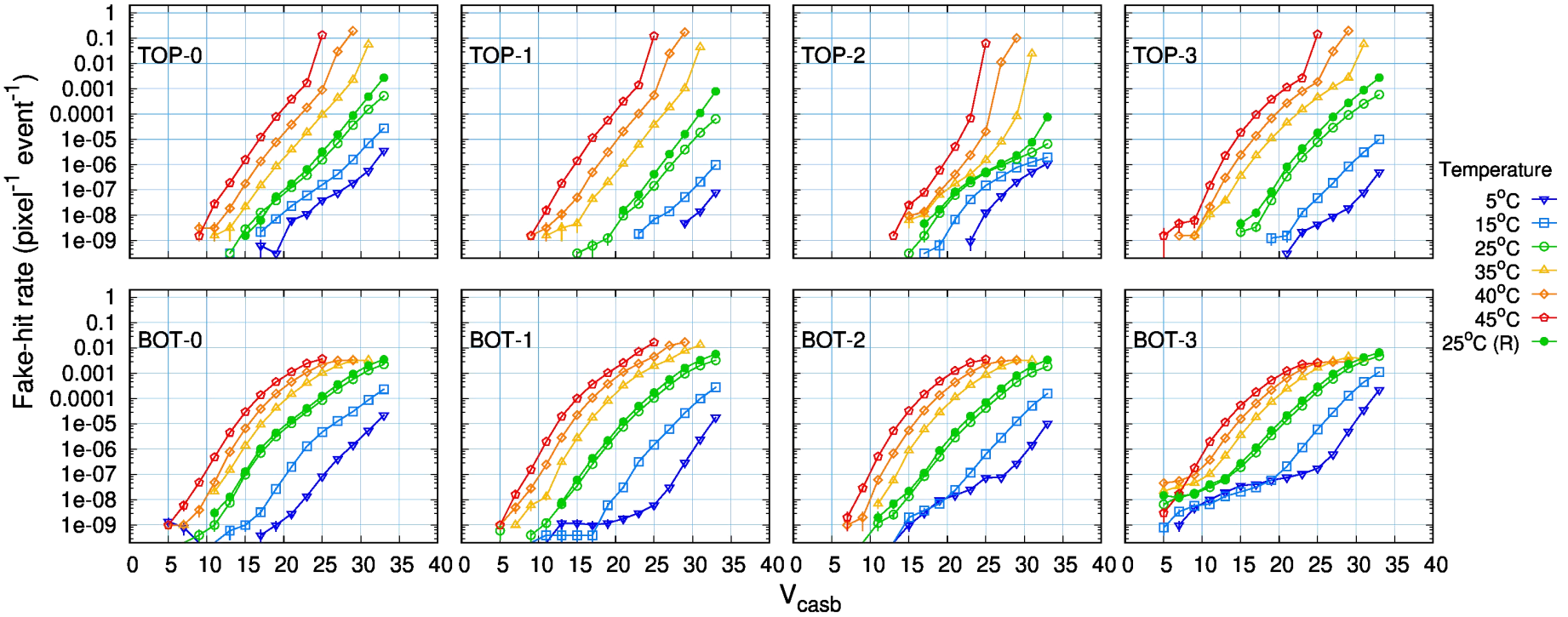
Will the order of scaning affect the results?





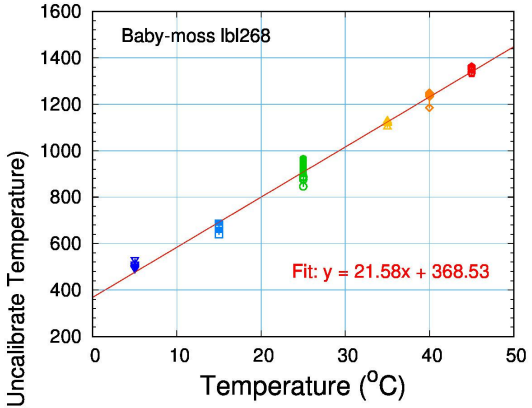
- The temperature read by thermistor resistance shows some difference (electronic warming up) - the scale is unknown
- No significant difference in Fake-hit Rate no matter scanning from large or small Vcasb in the current scale

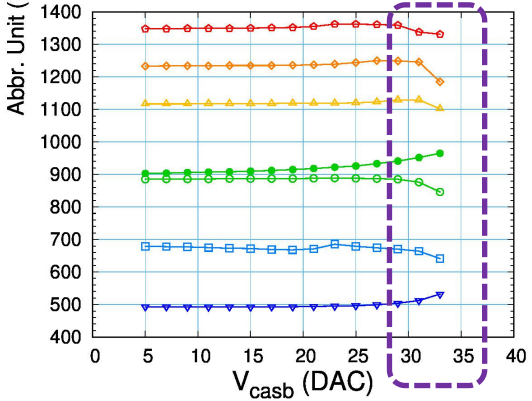
Fake-hit Rate vs Temperature (Board-C)

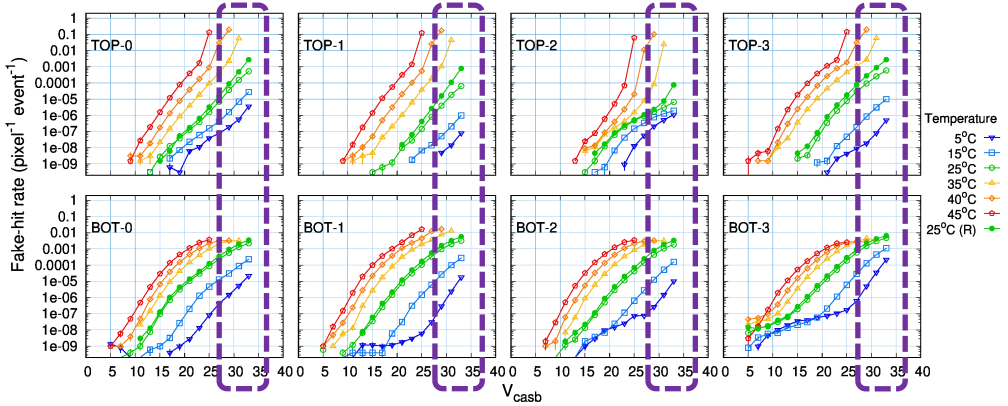


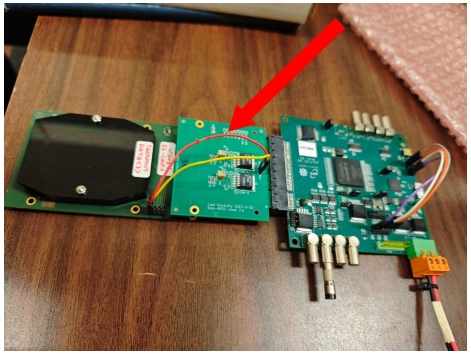
- High Temperature → High noise, as expected
- Noise levels are consistent at the same temperature after a run in a hot temperature (45°C)

Temperature sensor (thermistor resistance)









- There are some small variation at the beginning of the test
- The thermistor resistance follows the linear relation to the set temperature

Summary & Outlook

For Fake Rate Test:

- No significant different with masking @ Vcasb=15 and Vcasb=17
- No significant difference with 10k or 100k events - 10k should be sufficient enough
- Good consistence for Region-0,1,3, some differences for Region-2 compare with ALICE report
- The performance of individual board has noticeable differences, the trend of the Fake-hit rate are consistent
- No significant difference in Fake-hit Rate no matter scanning from large or small Vcasb in the current scale

Test with Climatic Chamber:

- High Temperature → High noise, as expected
- Noise levels are consistent at the same temperature after a run in a hot temperature (45°C)
- The thermistor resistance follows the linear relation to the set temperature

To to next:

- Temperature test with other boards
- Noise test after radiation exposure

Amplifier setups

DAC units:

IBIAS = 62
IBIASN = 100
IDB = 50
IRESET = 10
VCASB = 15
VCASN = 64
VSHIFT = 192

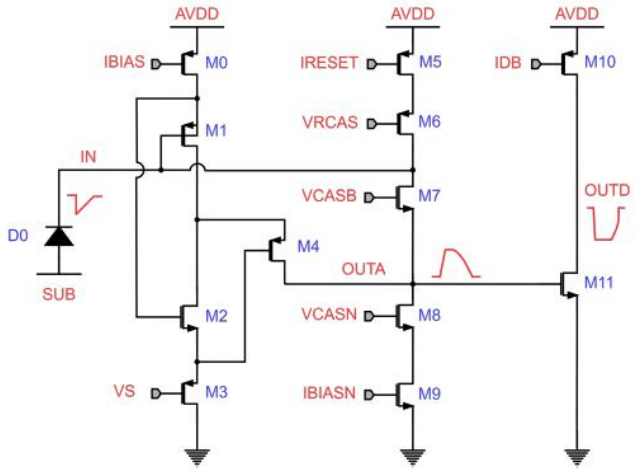
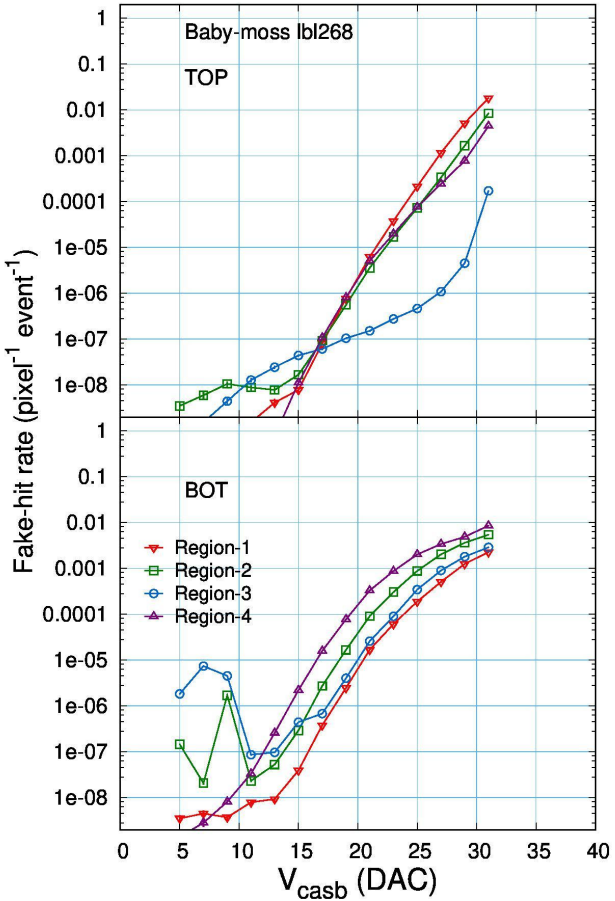
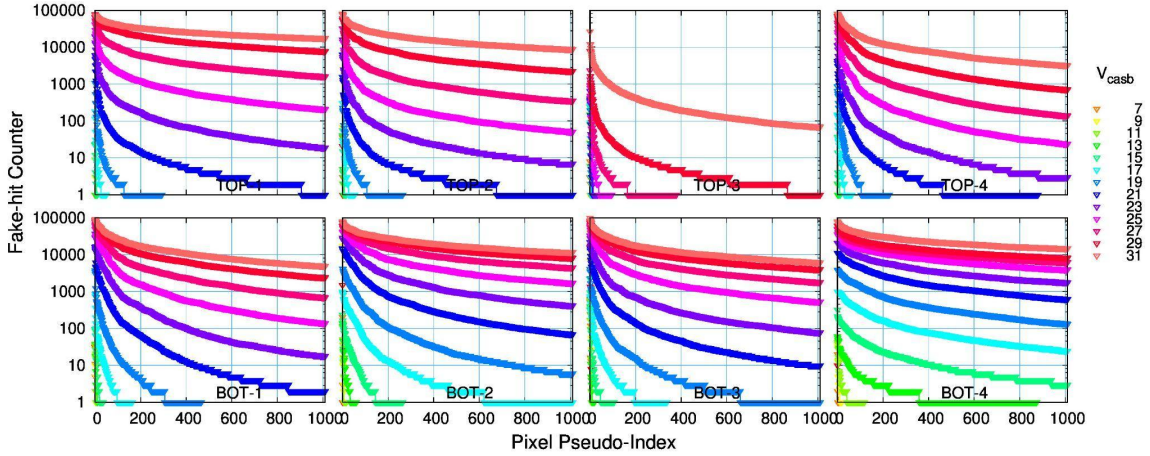


Figure 3.40: Simplified schematic of the pixel front-end amplifier and discrimination sections.

Board A - **W21D4 S3 CHIP3** (20240918) - 100k events



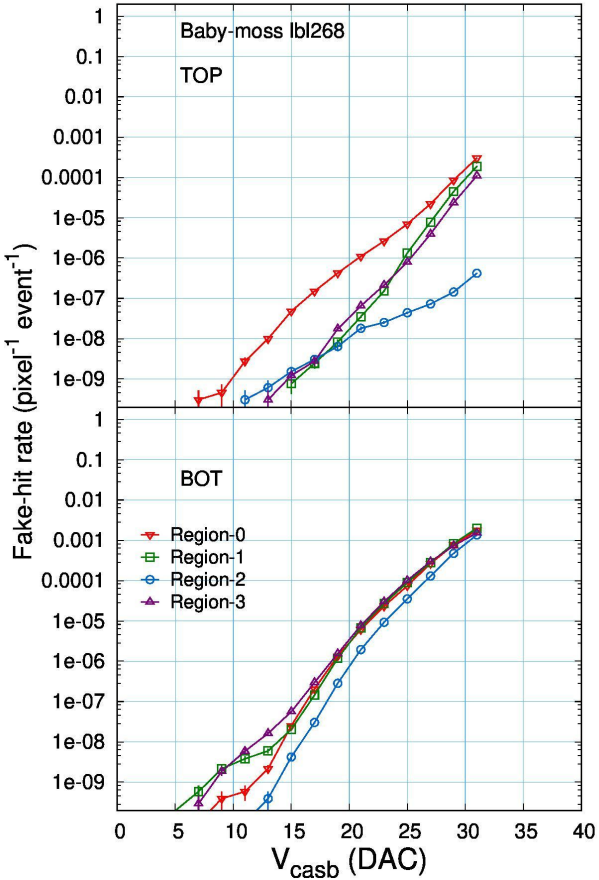


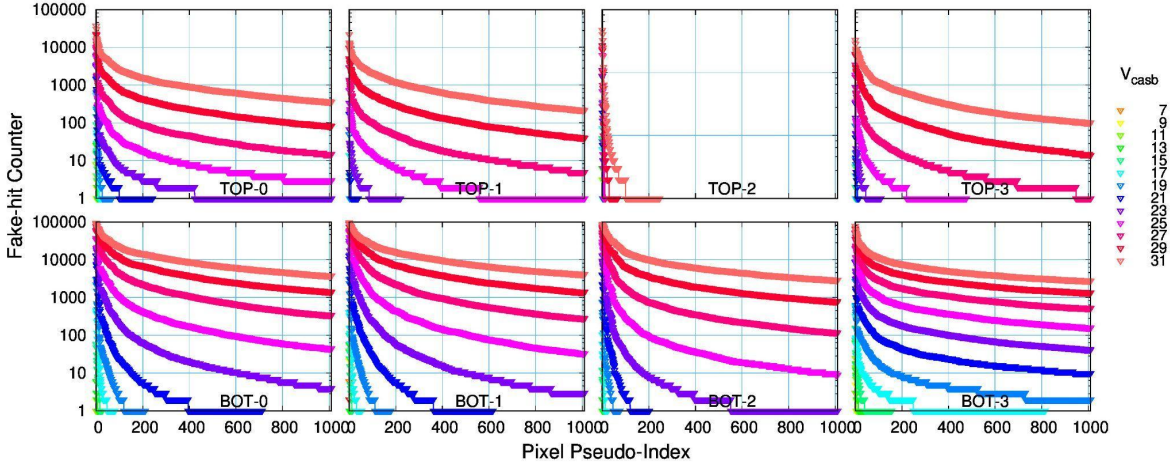
Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=17

Masked pixels

	R-0	R-1	R-2	R-3
TOP	4	7	4	1
BOT	11	35	8	67

Board B - **W20E1 S2 CHIP1** (20240918) - 100k events



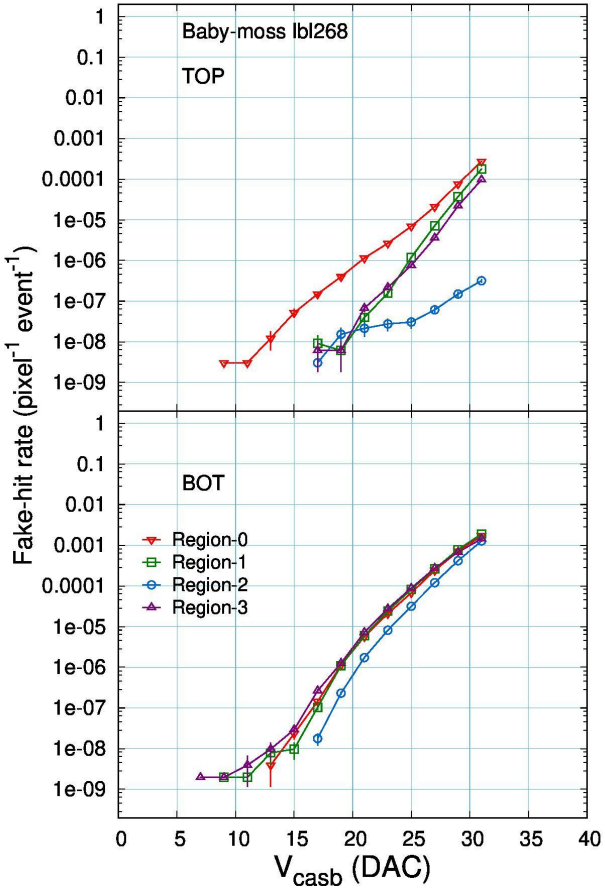


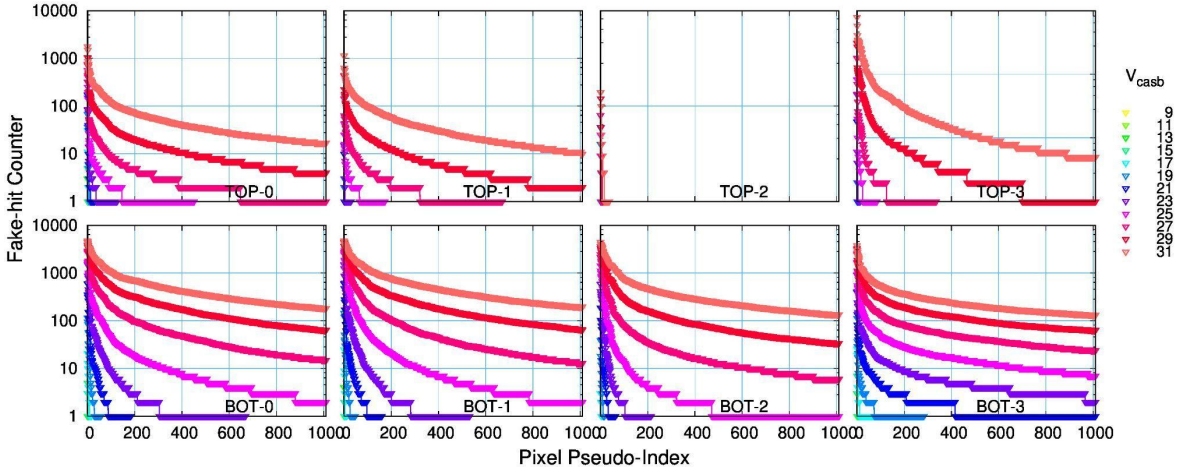
Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=17

Masked pixels

	R-0	R-1	R-2	R-3
TOP	0	0	0	0
BOT	0	0	0	2

Board B - **W20E1 S2 CHIP1** (20240918) - 5k events



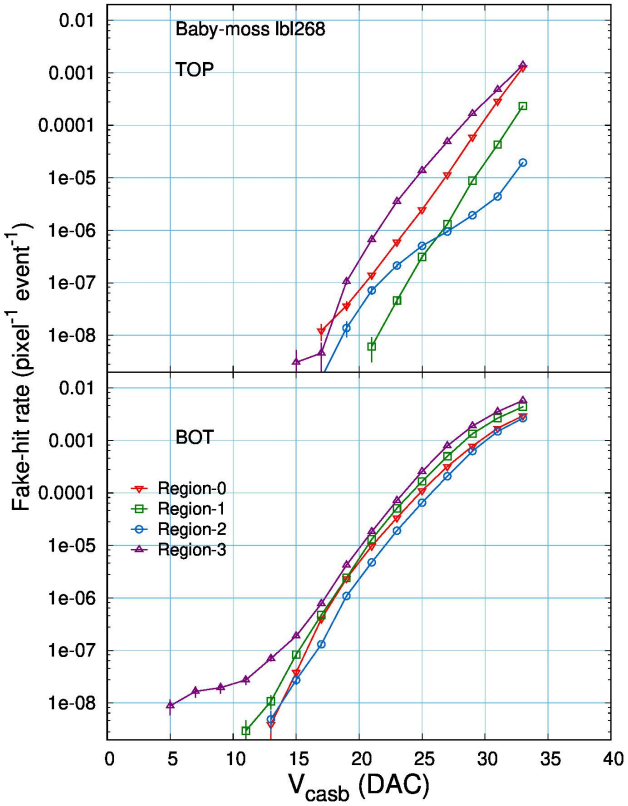


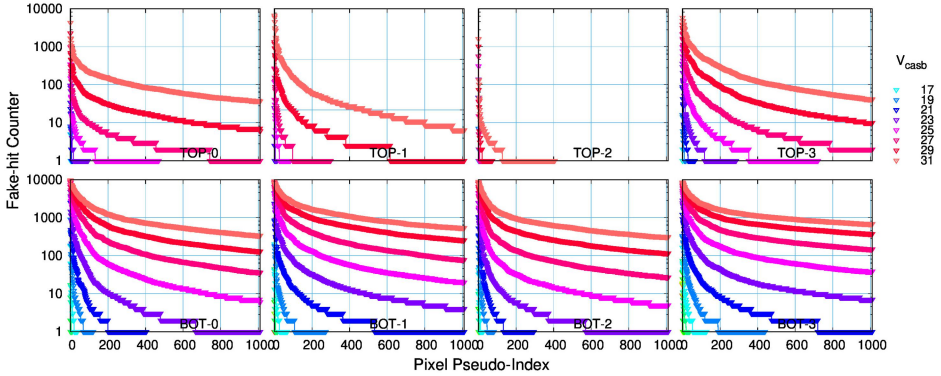
Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=15

Masked pixels

	R-0	R-1	R-2	R-3
TOP	0	0	0	0
BOT	0	0	0	2

Board C - **W20E1 S2 CHIP3** (20240924) - 10k events



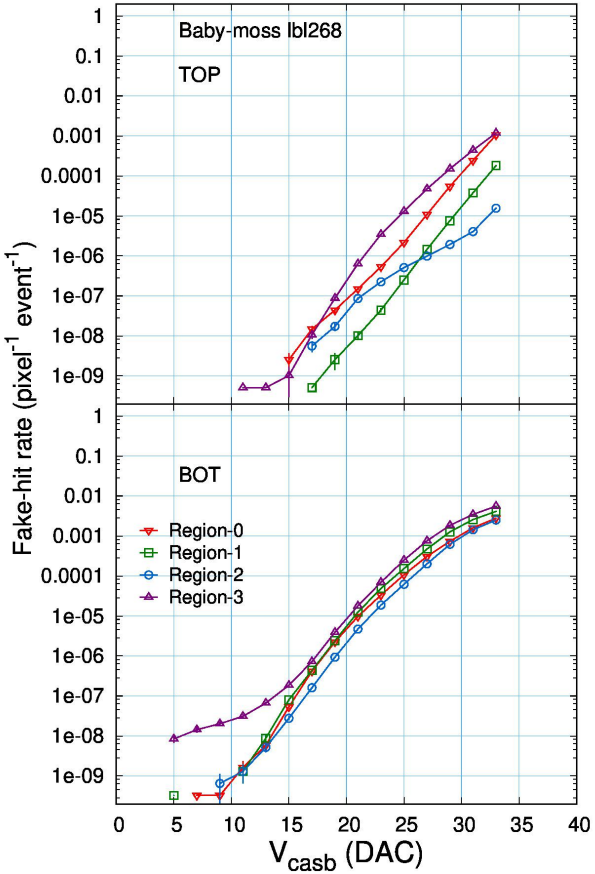


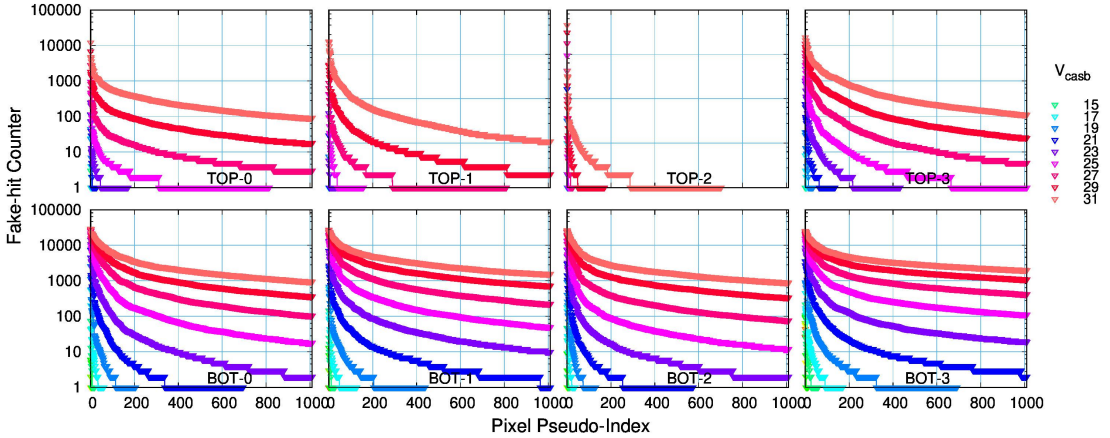
Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=15

Masked pixels

	R-0	R-1	R-2	R-3
TOP	0	0	0	0
BOT	1	0	0	2

Board C - **W20E1 S2 CHIP3** (20240924) - 30k events





Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=15

Masked pixels

	R-0	R-1	R-2	R-3
TOP	0	0	0	0
BOT	1	0	0	2