WBS 1.05 Detector Readout

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CUPID LBNL Project Review
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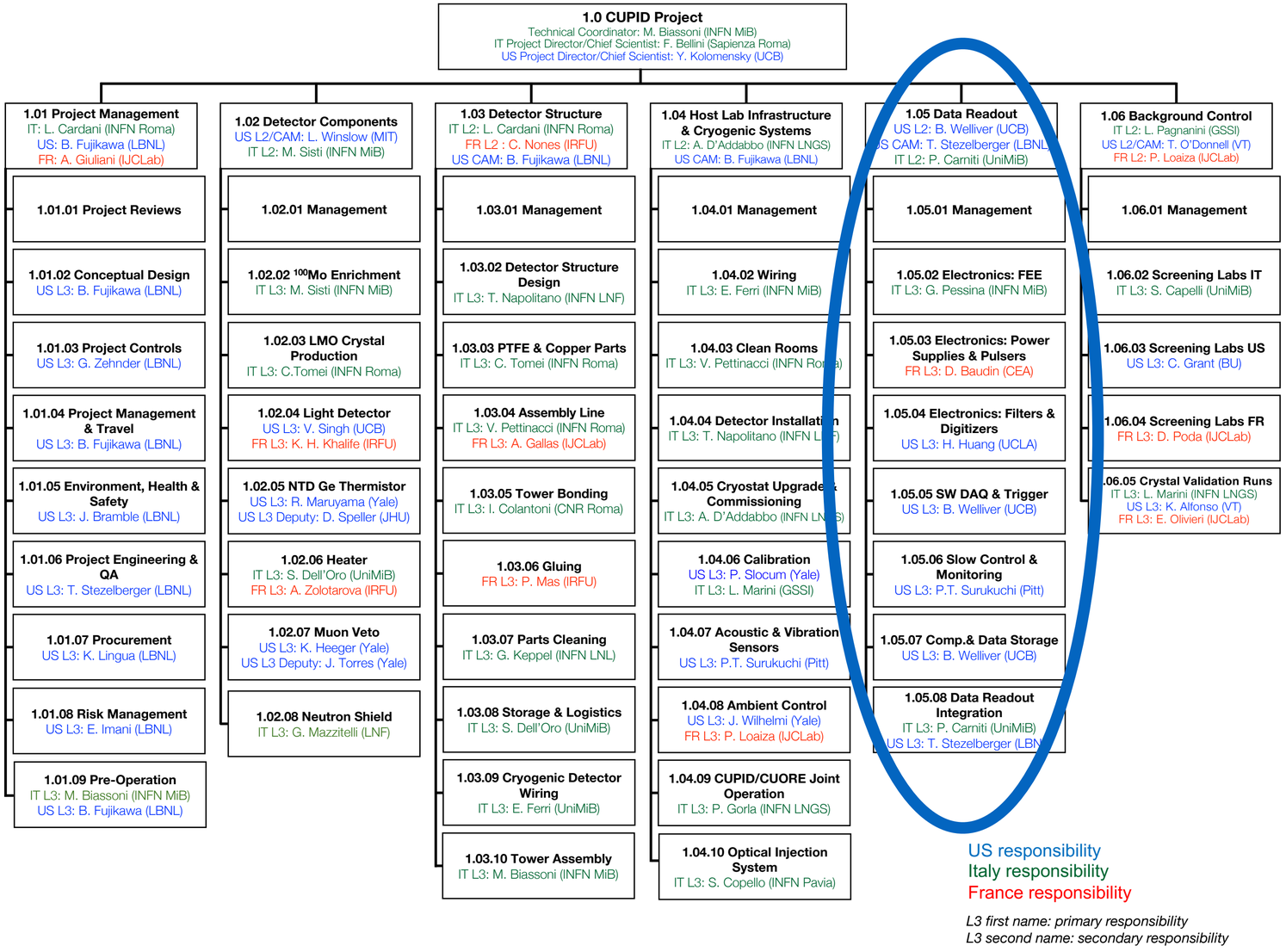
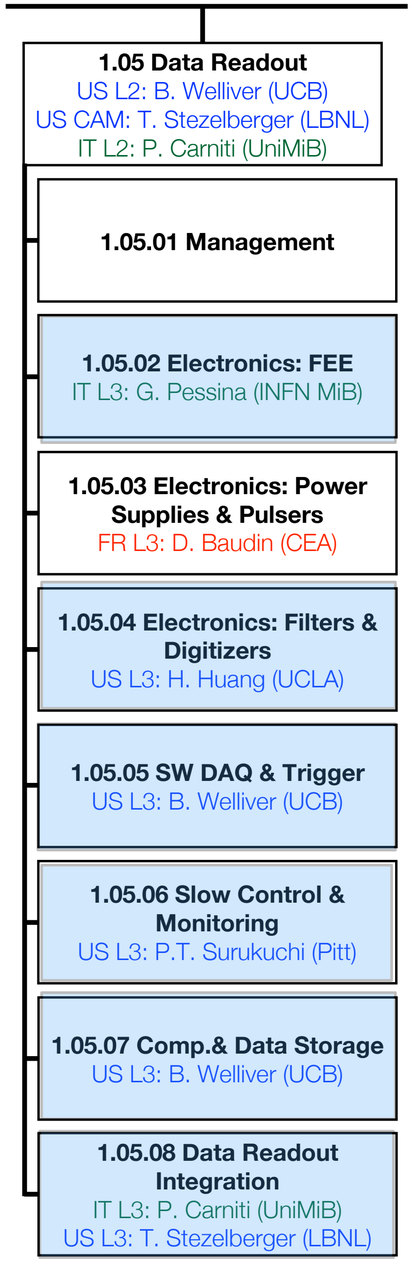
Berkeley
UNIVERSITY OF CALIFORNIA

Outline

- Overview
- Requirements
- Technical Readiness of subsystems
- Risks
- Interface with other subsystems
- Cost & Schedule
- Summary

WBS Organization

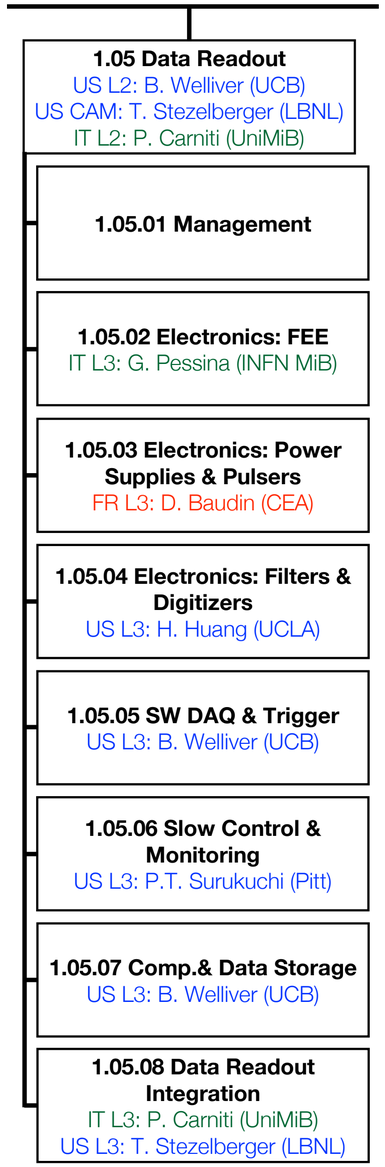




- L2/L3 reflect expertise with CUORE electronics or SW systems
- If 2 L3's are present the top is the primary responsible
  - Secondary for extra expertise

Contain US Project Scope

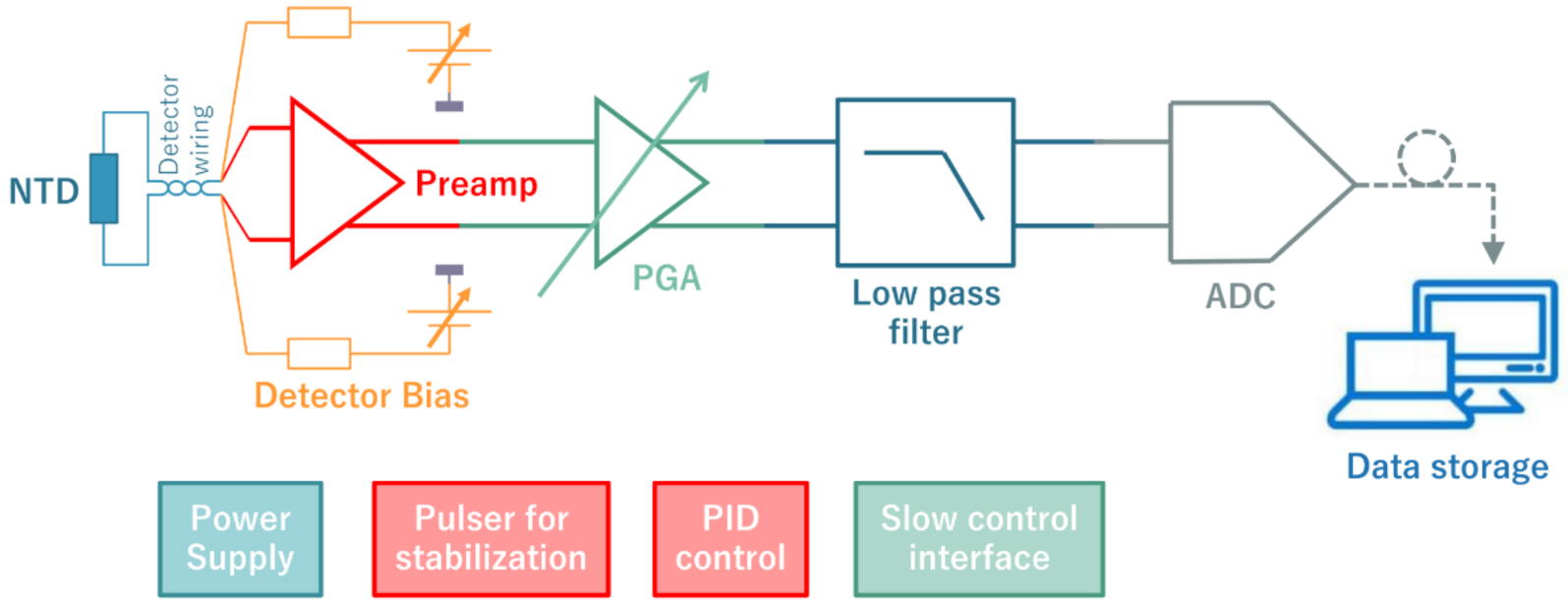
WBS Organization



- L2 Managers
  - Paolo Carniti - MiB
  - Bradford Welliver - UC Berkeley
  - US CAM: Thorsten Stezelberger - LBNL
- L3 Managers
  - Gianluigi Pessina - INFN MiB
  - Pranava Teja Surukuchi - Pitt
  - David Baudin - CEA
  - Huan Huang - UCLA

WBS 1.05: Overview

- In CUORE electronics design was done in IT and testing/ production in USA
- For CUPID, lead country responsible for an entire L3 package
  - Avoid cascading delays from single institute doing design or production of entire electronics system
- Design based off of *technically mature* and *proven* CUORE electronics
- Technical updates and specific optimizations for CUPID
- Working hardware prototypes exist

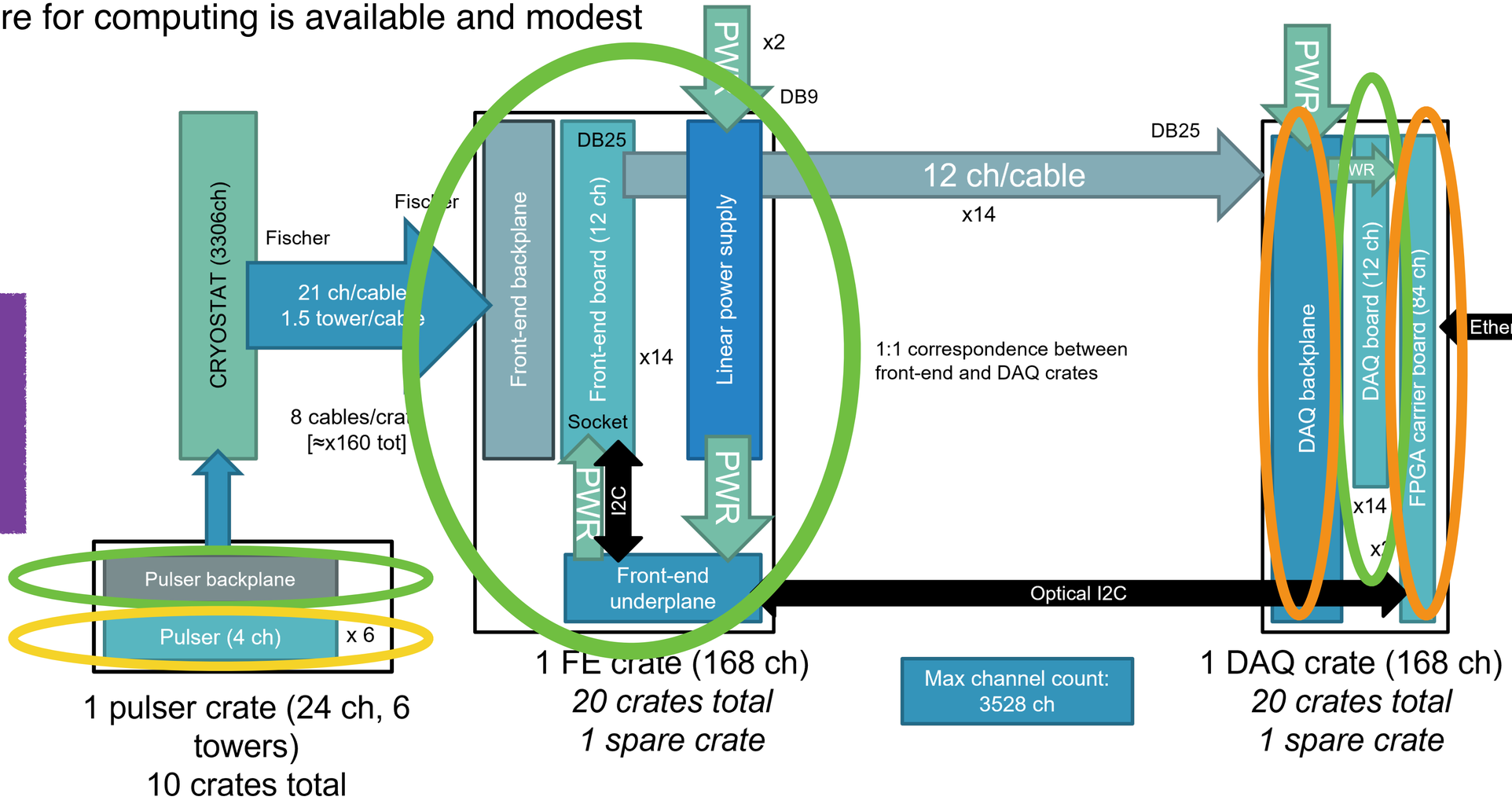


- **What's new?**
- WBS 1.05.03
  - HV power supplies for NTL
- WBS 1.05.04 is new
  - Well motivated combination of two components in CUORE readout chain
  - Working prototypes already

WBS 1.05 Technical Readiness

- The overall readiness of this WBS is quite mature
  - Hardware designs and prototypes exist for all components
  - Minor redesign of digitizers accounted for
- Commercial hardware for computing is available and modest

Available
Waiting Delivery
Minor redesign



WBS 1.05 KPPs

- Key performance parameters identified which drive project success

Description	Threshold	Objective
WBS 1.05	Delivery to LNGS of room-temperature electronics and sensor systems with the following performance requirements: >95% of the required channel count satisfy technical specifications; uptime>99%	Delivery to LNGS of room-temperature electronics and sensor systems meeting or exceeding technical requirements as demonstrated with a fully deployed system

WBS 1.05.02 Front End Electronics: Requirements

- Italian design and scope in Stage 1 - US procurement in Stage 2
- These requirements are on the front end electronics (FEE) and digitizers
- Readout bandwidth must be sufficient for fast light detector risetime
  - Mitigates background due to pile-up of 2νββ decays
- The input noise at the front end for the LD must be low enough to not significantly impact NTL gain
  - Depends upon intrinsic LD sensitivity (uV/keV)
  - Impacts pile-up background and energy resolution
- The input noise at the front end for the LMO must be sufficiently small as to not impact the energy resolution at $Q_{\beta\beta}$
  - Depends upon intrinsic LMO sensitivity (uV/keV)

Requirement	Value	WBS Level	High Level Requirement Connections	Top Level Science Requirement
Readout Bandwidth	≥ 5 kHz	2	Light detector rise time Pileup background Combined Signal Selection Efficiency	Total background (1e-4 cnt/keV/kg/yr) Total signal efficiency (0.67)
LMO readout input noise	< 1 keV	3	LMO detector intrinsic gain	Energy resolution 5 keV @ Qbb
LD readout input noise	< 20 eV	3	Light detector S/N(σ) after NTL Pileup BI Alpha/beta discrimination efficiency Radioactive background Combined signal selection efficiency Light detector intrinsic gain NTL gain on S/N	Pile-up background < 5e-5 ckky Energy resolution 5 keV @ Qbb

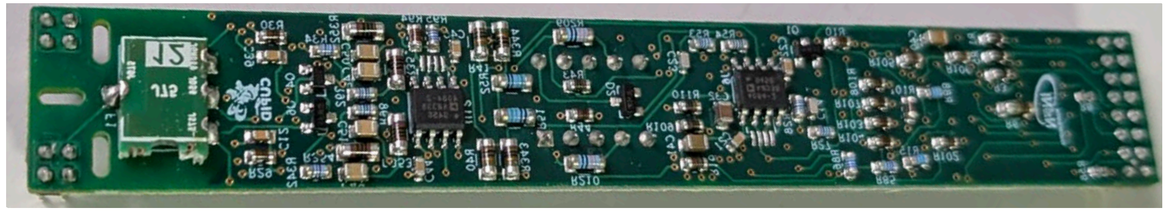
WBS 1.05.02 FEE: Technical Specifications

- Technical specifications for the front end electronics
- Design specifications are similar to CUORE or in applicable cases specific to CUPID updates
- Majority of these requirements derive from the baseline resolution requirements
- Technical requirements are met in recent prototypes

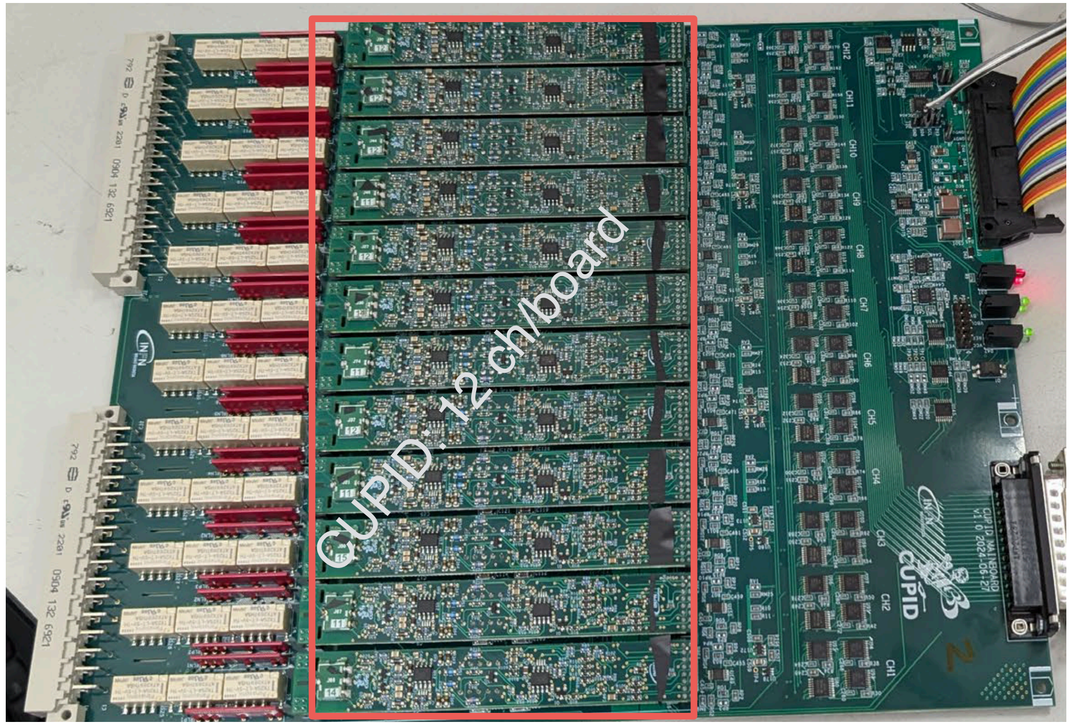
Technical Specification	Value	Note
Detector bias range	± 100 V	
Detector bias resolution	16 bit	
Detector bias stability	100 ppm/°C	
Bias resistor range	2 GΩ - 60 GΩ	
Preamplifier series noise	3.5 nV/sqrtHz 1.5 nV/sqrtHz	Low power (LMO) High power (LD)
Input Current	1.5 pA	At 40°C
Offset drift	< 1 µV/°C	
Offset correction	± 36 mV	
Offset correction resolution	16 bit	
Preamplifier gain	100 - 400	
PGA gains	1 - 4	
Gain stability	< 10 ppm/°C	
Power Consumption	220 mW/channel 380 mW/channel	Low power (LMO) High power (LD)

WBS 1.05.02 FEE: Conceptual Design

- Front-end electronics
  - Italian scope Stage 1, expertise from MiB,
  - US Procurement in Stage 2
- Utilize the same readout scheme as in CUORE
  - Preamp, PGA, biasing system all hosted on single board (“mainboard”)
- Mature and proven capability to operate O(1000) channels for years with no downtime
- Technical updates to boards to improve upon design
  - Different load resistors for heat vs light channels due to different NTD impedances
  - Increase max differential voltage on bias resistors: 100V (reduces parallel noise contribution via allowing larger bias resistors)
  - Series noise reduction for lower impedance of LD
  - Lower power consumption
- Boards exist
- JFET vendor selected and 20k procured by Italy

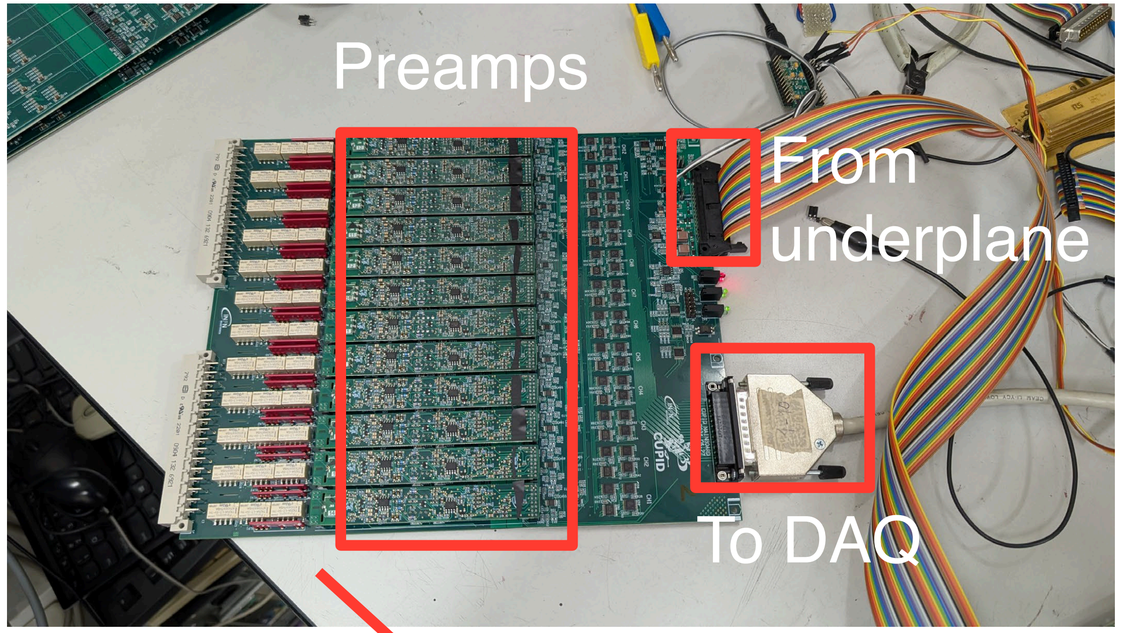


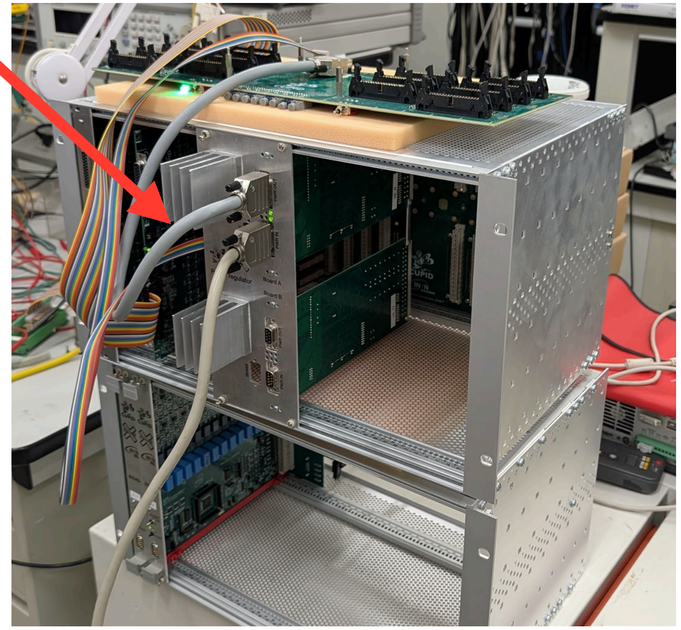
CUPID style preamp



WBS 1.05.02 FEE: Required R&D

- Main R&D efforts focused on a few items
- Optimizing JFET characterization testing to increase throughput
- Board characterization & calibration
- Firmware and software development for control
  - Motherboard firmware written in Python
  - Almost all functionality has been tested





14 mainboards can be inserted into each crate

WBS 1.05.02 FEE: Risks

- Risks identified and put into risk registry with mitigation strategies suggested
- Most risks are associated with potential supply chain issues with electronics components or computing hardware
- Cost, Schedule Contingency are sufficient to cover the risks and uncertainty at this stage of the project

Risk ID	L2	L3	Description	Consequence	Likelihood	Cost Impact	Schedule Impact	Technical Scope	Impact Ranking	Mitigation
105010059	5	1	Spare components may be misplaced	may not be possible to mitigate board failures	Unlikely	Significant (S)	Significant (S)	Significant (S)	Significant (S)	Keep detailed custodianship plan and documentation updated at all times
105020057	5	2	Preamp JFET do not meet spec	noise contributions to detector from electronics chain may increase	Unlikely	Marginal (M)	Significant (S)	Marginal (M)	Significant (S)	Identify JFET and vendor well in advance and procure components with spares that meet our requirements
105020058	5	2	Electronics components lifetime	may be difficult to procure replacements for electronics components	Unlikely	Significant (S)	Significant (S)	Significant (S)	Significant (S)	Procure a suitable number of spare parts and boards and store them in proper environment
105020063	5	2	Front end electronics location	need to modify mounting	Unlikely	Marginal (M)	Marginal (M)	Marginal (M)	Marginal (M)	board prototype designs and available space are known ahead of time
105020075	5	2	Thermal budget in faraday room	Need to implement additional cooling of Faraday room	Unlikely	Marginal (M)	Marginal (M)	Marginal (M)	Marginal (M)	Test power dissipation of new designs and identify ways to lower TDP
105020123	5	2	Long lead time of electronics components	delivery of electronics boards may take longer	Unlikely	Marginal (M)	Significant (S)	Marginal (M)	Significant (S)	Watch vendor lead times and consider more than one source

WBS 1.05.02 FEE: Interfaces

- Interface Control Documents started
- Keeps track of various interfaces between subsystems
- L2 manager responsible for top level document and delegate to L3 as appropriate

Interface	Description
Wiring (WBS 1.04.02)	Ensure compatible electrical and mechanical connections and layout at top of the cryostat
Power supplies & Pulsers (WBS 1.05.03)	Captures electrical and mechanical connections to the linear power supplies that power electronics
Filters and Digitizers (WBS 1.05.04)	Captures the electrical and mechanical connections to the digitizer and filter boards
Crystal Validation Runs (WBS 1.06.05)	Allows to possible use of prototype boards in crystal validation runs

WBS 1.05.03 Power Supplies & Pulsers: Requirements

- The injected heater pulse system is used for thermal gain correction
  - Direct impact on energy resolution
  - Requires very narrow spread for targeted input energy
- French scope

Requirement	Value	WBS Level	High Level Requirement Connections	Top Level Science Requirement
Pulser Energy spread @ 2615 keV	100 eV FWHM	3		Energy resolution 5 keV @ $Q_{\beta\beta}$

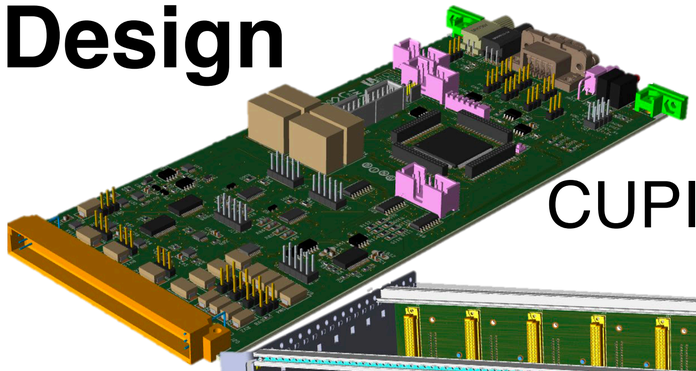
WBS 1.05.03 PS & Pulers: Technical Specifications

- Technical specifications for the pulser and power supplies
- Technical requirements are met in recent prototypes, or for the case of commercial supplies exist and are available on the market

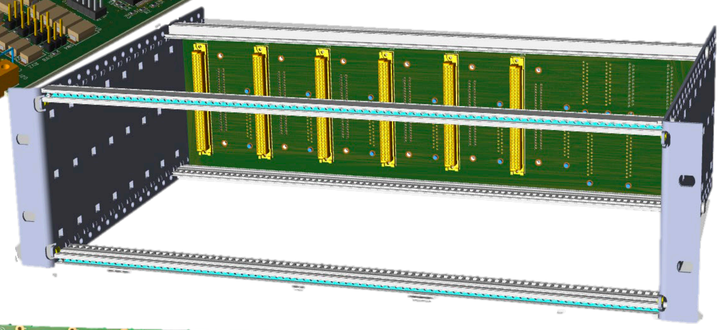
Technical Specification	Value	Note
LPS output voltage	± 5 V	
LPS output current	4 A	
LPS stability	2 ppm/°C	
LPS noise	50 nV/sqrtHz 20 nV/sqrtHz	at 1 Hz at 1 kHz
LPS PSRR	60 dB	
Commercial supply output range	5 V - 120 V	floating
Commercial supply ripple	5 mVpp	
Pulser stability	2 ppm/°C	
Pulser resolution	16 bit	

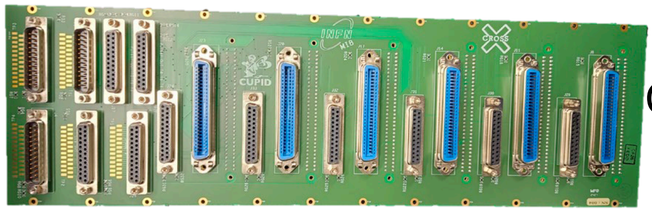
WBS 1.05.03 PS & Pulers: Conceptual Design

- French scope
- CUORE system used 3 stage power supply
  - AC/DC, DC/DC, and linear regulator with only the first being commercial
  - CUPID will simplify by removing the DC/DC stage
- Will use a suitably low-noise AC/DC commercial stage
- Linear regulator will see some minor technical updates
- Pulser boards generate short voltage pulses to heater resistors glued to crystals
  - Simulates particle events in a controlled fashion
  - Slow stabilization of cryostat temperature
  - Thermal gain correction of detector channels
- CUORE demonstrated board thermal stability of < 0.3 ppm/°C
- Minor technical updates to improve versatility
  - Double number of independent channels per board: 2 —> 4 (57 pulsers to cover all towers)
  - 1 LED driver with tunable 12-bit output current
  - Ultra-low power microcontroller (STM Cortex M33)
  - Optical trigger
  - CANbus control

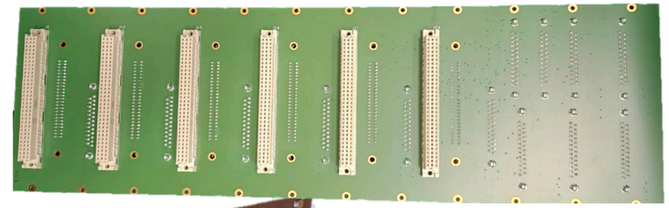


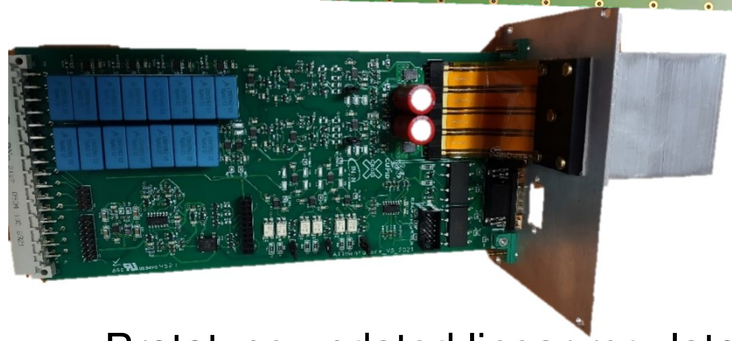
CUPID Pulser





CUPID Pulser backplane





Prototype updated linear regulator

WBS 1.05.03 PS & Pulers: Required R&D

- NTL light detectors will require additional dedicated HV supplies
  - Noise and output current not as strict
  - Will use a multi-channel programmable commercial solution
  - Use a custom distribution board for cryostat interface & leakage current monitoring
  - Evaluating requirements and scheme (max voltage, max current)
- Firmware and debugging prototype pulser boards
- Procure and evaluate samples of commercial AC/DC supplies

WBS 1.05.03 PS & Pulers: Risks

- Risks identified and put into risk registry with mitigation strategies suggested
- Most risks are associated with potential supply chain issues with electronics components or computing hardware
- Cost, Schedule Contingency are sufficient to cover the risks and uncertainty at this stage of the project

Risk ID	L2	L3	Description	Consequence	Likelihood	Cost Impact	Schedule Impact	Technical Scope	Impact Ranking	Mitigation
105030061	5	3	Power supply noise	baseline resolution may worsen	Unlikely	Marginal (M)	Marginal (M)	Significant (S)	Significant (S)	Iteratively prototype supplies to verify sufficient noise performance
105030062	5	3	Power supply load drive	Need to add more supplies to provide current	Unlikely	Significant (S)	Marginal (M)	Marginal (M)	Significant (S)	produce & procure more power supplies

WBS 1.05.03 PS & Pulers: Interfaces

- Interface Control Documents started
- Keeps track of various interfaces between subsystems
- L2 manager responsible for top level document and delegate to L3 as appropriate

Interface	Description
Wiring (WBS 1.04.02)	Ensures electrical and mechanical connections to the cryostat wiring form pulser boards is consistent
Optical Injection System (WBS 1.04.10)	Details the electrical and mechanical connections and how the pulser controls the OIS
Front-end Electronics (WBS 1.05.02)	Captures electrical and mechanical connections between the FEE and the linear power supplies as well as required power load
Filters and Digitizers (WBS 1.05.04)	Captures the electrical and mechanical connections to the digitizer and filter boards as well as connection the power supply and required load
Crystal Validation Runs (WBS 1.06.05)	Allows to possible use of prototypes in crystal validation runs

WBS 1.05.04 Filter & Digitizer Board: Requirements

- The filter and digitizer system has a requirement connection in the form of the required sampling rate for the LD bandwidth

Requirement	Value	WBS Level	High Level Requirement Connections	Top Level Science Requirement
Sampling Rate	≥ 10 kHz	2	Light detector rise time Pileup background Combined Signal Selection Efficiency	Total background (1e-4 cnt/keV/kg/yr) Total signal efficiency (0.67)

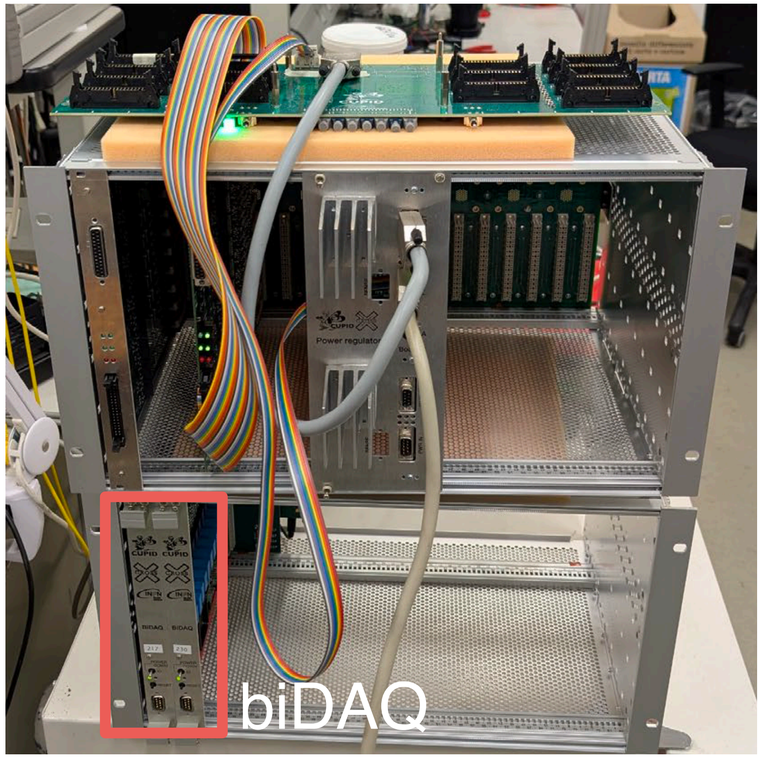
WBS 1.05.04 Filter & Digitizer: Technical Specifications

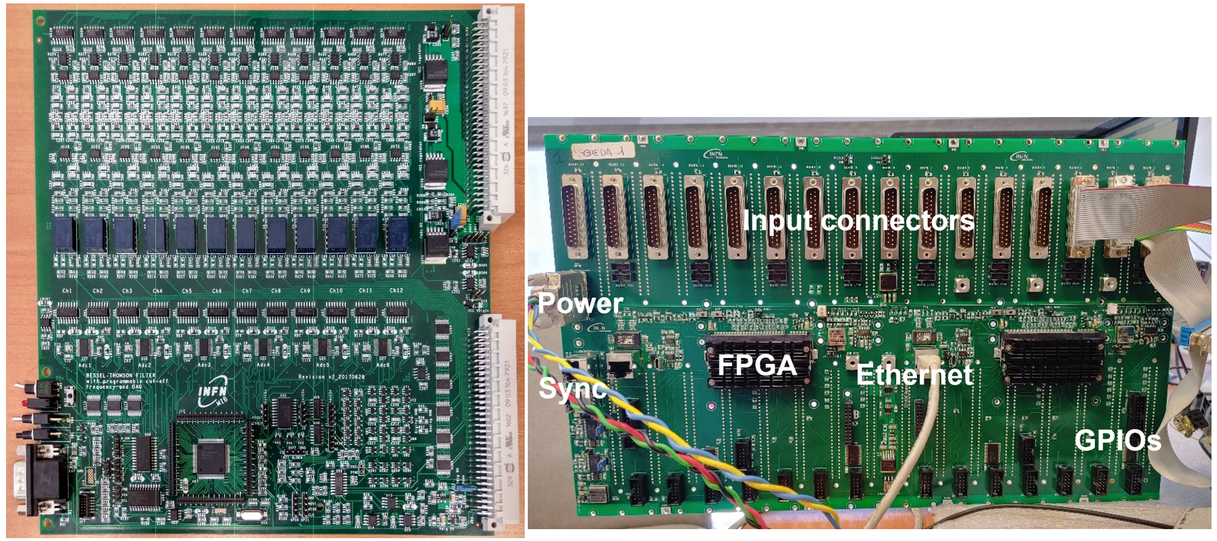
- Technical specifications for the filter and digitizer boards
- Technical requirements are met in recent prototypes

Technical Specification	Value	Note
Filter cut-off range	25 Hz - 2.5 kHz	programmable
Filter cut-off resolution	8 bit	
Sampling frequency	> 10 kHz	25 kHz supported
Resolution	24 bit	
Input Noise	600 nV/channel 180 nV/channel	at 1 Hz at 1 kHz

WBS 1.05.04 Filter & Digitizer: Conceptual Design

- CUPID will use a custom board that integrates filter + digitizer
- Prototype boards already exists from MiB - Italy (biDAQ)
- Digitally selected filter cutoffs for independent heat and light detector settings
- Saves space, power, and have control over board firmware
  - ~2x less power consumption than CUORE boards
  - 5x less power overall when considering removal of NI digitizers and associated crates
- 12 channels per board, 16 boards per backplane
- FPGA control for acquisition + clock sync with other boards (PLL, backplane connectors for daisy chaining)





Example of Updated Prototype Bessel + Digitizer (BiDAQ)

Digitally select filter cut-offs in range from 24 Hz - 2500 Hz

24-bit delta-sigma ADCs

Up to 25 kHz sampling per channel

Gain calibration, external ADC clock

FPGA for easy modifications

WBS 1.05.04 Filter & Digitizer: Required R&D

- Update to move FPGAs off backplane and onto dedicated control cards
  - Easier replacement if FPGA fails + allows for update to current FPGA design
  - Enclustra Mars ZX3: pin-to-pin compatible with current FPGA (Mars MA3 with Altera Cyclone V SoC FPGA) + tool chains compatible
  - Electrical engineering effort allocated for task
- Consider increase of filter cutoff x2
- Firmware development
  - Adaptation of existing firmware for ZX3 or other FPGA module

WBS 1.05.04 Filter & Digitizer: Risks

- Risks identified and put into risk registry with mitigation strategies suggested
- Most risks are associated with potential supply chain issues with electronics components or computing hardware
- Cost, Schedule Contingency are sufficient to cover the risks and uncertainty at this stage of the project

Risk ID	L2	L3	Description	Consequence	Likelihood	Cost Impact	Schedule Impact	Technical Scope	Impact Ranking	Mitigation
105040064	5	4	Packet loss from digitizer to SW DAQ	data loss may occur	Unlikely	Marginal (M)	Significant (S)	Significant (S)	Significant (S)	throughput testing of board data streaming and SW processing with prototypes to determine safe loading & consider alternative packet scheme if needed
105040100	5	4	FPGA long lead times	Production of functional digitizer boards and firmware development may be delayed	Likely	Marginal (M)	Significant (S)	Marginal (M)	Significant (S)	Examine multiple venders and utilize commonly available FPGA
105040107	5	4	Air cooling not sufficient	May need to water cool	Unlikely	Marginal (M)	Marginal (M)	Marginal (M)	Marginal (M)	Measure TDP of crates

WBS 1.05.04 Filter & Digitizer: Interfaces

- Interface Control Documents started
- Keeps track of various interfaces between subsystems
- L2 manager responsible for top level document and delegate to L3 as appropriate

Interface	Description
Acoustic and Vibration Sensors (WBS 1.04.07)	Captures electrical and mechanical connections to auxiliary sensors through additional input lines so they may be digitized
Front-end Electronics (WBS 1.05.02)	Captures electrical and mechanical connections between to the FEE to allow for data acquisition
Power Supplies and Pulsers (WBS 1.05.03)	Captures the electrical and mechanical connections to the digitizer and filter boards as well as connection the power supply and required load
Data Acquisition (WBS 1.05.05)	Captures electrical and mechanical connections, as well as communication protocol with computers running software DAQ allowing for data to be saved to disk
Crystal Validation Runs (WBS 1.06.05)	Allows to possible use of prototypes in crystal validation runs

WBS 1.05.05 Software DAQ: Requirements

- The software DAQ system has requirements related to timing
- Relative timing between various DAQ machines + digitizer boards and muon veto system
  - Coincidence analysis requires accurate timing between channels of the detector and the muon system
- Absolute timing accuracy to the real world has constraints from other physics
  - Supernova neutrino interactions provide possible strict requirements (highly dependent upon proximity of supernova)

Requirement	Value	WBS Level	High Level Requirement Connections	Top Level Science Requirement
Absolute time accuracy	< 1 ms	2		Other physics
Relative timing	0.1 ms	2		Total Background (1e-4 cnt/keV/kg/yr)

WBS 1.05.05 Software DAQ: Technical Specifications

- Technical specifications for DAQ
- These are modest requirements for computing power and data throughput
  - Assumes 12 total DAQ machines
  - Other configurations besides 6 LMO + 6 LD machines perfectly fine

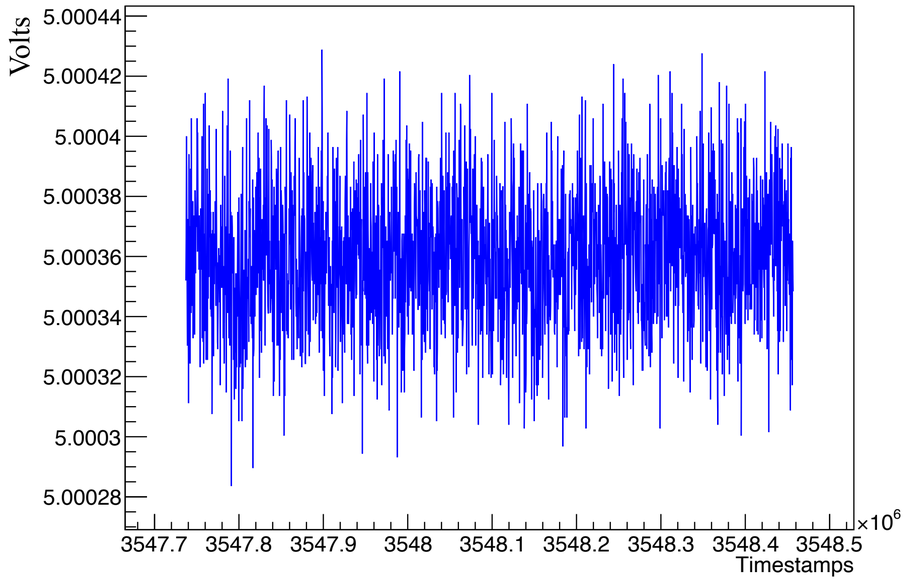
Technical Specification	Value	Note
Acquired Sampling Rate	2 kS/s 10 kS/s	LMO LD
Channel / Computer	266 285	LMO LD
Data Rate / Computer	2.1 MB/s 11.4 MB/s	LMO LD
Continuous Data Rate	1.1 TB/day 5.9 TB/day	LMO LD

WBS 1.05.05 Software DAQ: Conceptual Design

- DAQ software in C++ for interface with digitizer boards
  - ROOT6 / ROOT7 file format for output
- Must run across multiple parallel computers
  - Estimate of 12 DAQ computers
  - Well within current computing capabilities
- Intra-DAQ synchronization done via 10 MHz Rb clock
- Synchronization to external world via GPS clock + low-latency NTP or PTP network
- Control
  - Eclipse Mosquitto implementation of MQTT
  - Basic structure for messages generated using lightweight JSON library
  - Control structure being tested
- Readout
  - Able to acquire and parse packets from digitizers
  - Multithreaded process to avoid blocking acquisition of signals
  - IO routines being tested

		Byte offset			
		0	1	2	3
Word offset	0	RTP byte	Payload type	Sequence number	
	1	Timestamp			
	2	SSRC identifier			
	3	Payload header			
	4	Payload data 0			
	...	...			
	N+4	Payload data N			
	N+5	Footer			

RTP Packet Structure from digitizer



Acquired waveform from digitizer via DAQ

WBS 1.05.05 Software DAQ: Required R&D

- Determine details of timing protocols to use for real world sync and for intra-board
- Most (all) of the remaining R&D is software development

WBS 1.05.05 Software DAQ: Risks

- Risks identified and put into risk registry with mitigation strategies suggested
- Most risks are associated with potential supply chain issues with electronics components or computing hardware
- Cost, Schedule Contingency are sufficient to cover the risks and uncertainty at this stage of the project

Risk ID	L2	L3	Description	Consequence	Likelihood	Cost Impact	Schedule Impact	Technical Scope	Impact Ranking	Mitigation
105050108	5	5	Software development delays	Software DAQ is delayed	Unlikely	Marginal (M)	Marginal (M)	Marginal (M)	Marginal (M)	Development is pushed forward and active recruiting to keep development team at level of at least 2

WBS 1.05.05 Software DAQ: Interfaces

- Interface Control Documents started
- Keeps track of various interfaces between subsystems
- L2 manager responsible for top level document and delegate to L3 as appropriate

Interface	Description
Detector Structure Design (WBS 1.03.02)	Required for installation location of the DAQ computer hardware
Acoustic and Vibration Sensors (WBS 1.04.07)	Captures need to acquire and store a small number of auxiliary sensor data alongside the CUPID detector data
Front-end Electronics (WBS 1.05.02)	Captures electrical and mechanical connections to the FEE to allow for slow control communication
Power Supplies and Pulsers (WBS 1.05.03)	Captures the electrical and mechanical connections between the software DAQ machines to the pulser electronics, and in particular insertion of digital pulser trigger flags.
Filters and Digitizers (WBS 1.05.04)	Captures the electrical and mechanical interface between the digitizer boards and the DAQ machines as well as communication for slow control
Slow Control and Slow Monitoring (WBS 1.05.06)	Includes any slowcontrol connections that may be sent through the software DAQ computing hardware to other electronics.
Crystal Validation Runs (WBS 1.06.05)	Allows to possible testing of DAQ software in crystal validation runs

WBS 1.05.06 Slowcontrol & Slowmonitor: Requirements

- The slowcontrol/monitoring (SC & SM) system has a requirement related to the need to display realtime data and issue timely alerts

Requirement	Value	WBS Level	High Level Requirement Connections	Top Level Science Requirement
Monitoring Cryogenics	Realtime	3	Background data taking uptime	Livetime (10 yr)

WBS 1.05.06 SC & SM: Technical Specifications

- Technical specifications for slowcontrol and slow monitoring
- Slowcontrol protocol based on what electronics boards will support
- Slowmonitoring system needs to run continuously
- Parts tracking databases are coordinated with other WBS and provides a central repository to access

Technical Specification	Value	Note
Slowcontrol Protocol	MQTT	
Slowmonitor Storage	20 TB	
Alerts	Email Phone	Realtime Realtime
System Uptime	Continuous	
Parts Tracking	PSQL DB	Centralized repository

WBS 1.05.06 SC & SM: Conceptual Design

- CUORE uses an online web application called the CUORE Online Run Check (CORC) to monitor detector channels + cryogenic hardware status (temperatures, pressures, etc)
  - Provides quick (live) data for assessment of data taking or cryostat performance
  - Ability for users to interact with data and visualize different useful parameters
  - Flag data during sub-optimal times of performance to remove from analysis
  - Issue alarms (email + phone) when cryostat parameters stop updating or go out of range
- Development of new software not started yet but exploratory work at examining industry supported platforms (e.g., Grafana)
- Slow control protocols for electronics defined: MQTT
  - Work not started yet on developing control software but will profit from DAQ work with similar protocol

WBS 1.05.06 SC & SM: Required R&D

- Most (all) of the remaining R&D is software development related

WBS 1.05.06 SC & SM: Risks

- Risks identified and put into risk registry with mitigation strategies suggested
- Most risks are associated with potential supply chain issues with electronics components or computing hardware
- Cost, Schedule Contingency are sufficient to cover the risks and uncertainty at this stage of the project

Risk ID	L2	L3	Description	Consequence	Likelihood	Cost Impact	Schedule Impact	Technical Scope	Impact Ranking	Mitigation
105060109	5	6	Software development delays	Project would need to consider less flexible options to ensure monitoring	Unlikely	Marginal (M)	Marginal (M)	Marginal (M)	Marginal (M)	Explore options to avoid significant “reinventing the wheel” in monitoring software

WBS 1.05.06 SC & SM: Interfaces

- Interface Control Documents started
- Keeps track of various interfaces between subsystems
- L2 manager responsible for top level document and delegate to L3 as appropriate

Interface	Description
LMO Crystal Production (WBS 1.02.03), Light Detector (WBS 1.02.04), NTD Ge Thermistor (WBS 1.02.05), Heater (WBS 1.02.06), Muon Veto (1.02.07), PTFE Parts (WBS 1.03.03), Copper Parts (WBS 1.03.04), Assembly Line (WBS 1.03.05), Tower Bondering (WBS 1.03.06), Gluing (WBS 1.03.07), Parts Cleaning (WBS 1.03.08), Storage and Logistics (WBS 1.03.09), Cryogenic Detector Wiring (WBS 1.03.10), Tower Assembly (WBS 1.03.11), Clean Rooms (WBS 1.04.03), Detector installation (WBS 1.04.04), Cryostat Upgrade & Commissioning (WBS 1.04.05), Screening Labs IT (WBS 1.06.02), Screening Labs US (WBS 1.06.03), Screening Labs FR (WBS 1.06.04), Crystal Validation Runs (1.06.05)	Parts tracking and other databases
Muon Veto (WBS 1.02.07), Calibration (WBS 1.04.06), Acoustic and Vibration Sensors (WBS 1.04.07), Ambient Control (WBS 1.04.08), SW DAQ (WBS 1.05.05), Computer and Data Storage (WBS 1.05.07)	Slowmonitoring

WBS 1.05.07 Computing & Networking: Requirements

- The computing and data storage system has a requirement related to the need to process ongoing live data in order for timely diagnostics

Requirement	Value	WBS Level	High Level Requirement Connections	Top Level Science Requirement
Real time data processing	< 1 hr	3	Background data taking uptime	Livetime (10 yr)

WBS 1.05.07 Computing: Technical Specifications

- Technical specifications computing and data storage
- Relate to need to store one year of data and to quickly move this data around
- HPC cluster requirement is to ensure no single point of failure

Technical Specification	Value	Note
Data storage	2.6 PB	1 year of data
Networking	100 Gbps	Onsite data throughput
HPC Clusters	> 2	Redundancy of computing power and back up of data
Number Servers Onsite	> 2 High performance > 2 DB Servers	For data production For database hosting

WBS 1.05.07 Computing: Conceptual Design

- Sufficient computing and storage resources are available for reasonable prices
  - All commercial hardware — computing power & data density increase yearly
  - Exploit this by delaying purchase of resources until as late as reasonable
  - CUPID is not a “big data" scale experiment
- Networking requirements increased
  - CUPID will generate about 80 MB/s just from data taking—> current gigabit/fiber can handle this easily
  - Challenge: easily stream this data across world (possible GridFTP services needed)
- Data management plan based off of CUORE but with modifications for larger footprint
  - Backups on different on and offsite locations
  - RAID6 for copies of raw data on servers
  - Tape archive

WBS 1.05.07 Computing: Required R&D

- Develop data management plan in detail
- Examine possible strategies for mitigating slow rebuild times with RAID and large volumes
- Define options for fast international data transfers

WBS 1.05.07 Computing: Risks

- Risks identified and put into risk registry with mitigation strategies suggested
- Most risks are associated with potential supply chain issues with electronics components or computing hardware
- Cost, Schedule Contingency are sufficient to cover the risks and uncertainty at this stage of the project

Risk ID	L2	L3	Description	Consequence	Likelihood	Cost Impact	Schedule Impact	Technical Scope	Impact Ranking	Mitigation
105070065	5	7	CPU/HDD shortage for computing	Costs for required computing and data storage will increase	Unlikely	Significant (S)	Marginal (M)	Marginal (M)	Significant (S)	Continue monitoring vendor updates and forecasts for supply

WBS 1.05.07 Computing: Interfaces

- Interface Control Documents started
- Keeps track of various interfaces between subsystems
- L2 manager responsible for top level document and delegate to L3 as appropriate

Interface	Description
LMO Crystal Production (WBS 1.02.03)	Captures required storage based on design of LMO detectors
Light Detector (WBS 1.02.04)	Captures the required storage space needed based on the design parameters of light detectors
NTD Ge Thermistor (WBS 1.02.05)	Captures storage requirements based on design of the NTD (i.e, the sampling rates)
Muon Veto (WBS 1.02.07)	Captures the need to store muon veto system trigger data
Acoustic and Vibration Sensors (WBS 1.04.07)	Captures need to store auxiliary sensor data
Front-end electronics (WBS 1.05.02)	Captures the data storage and data transfer requirements of data acquired from the detector
Power Supplies and Pulsers (WBS 1.05.03)	Provides for the data storage and networking related to pulser board communication
Filter and Digitizer (WBS 1.05.04)	Provides for the data storage and networking related to digitizer board communication
Software DAQ (WBS 1.05.05)	Provides for the data storage and networking related to the acquisition of all digitized data from the CUPID experiment
Crystal Validation Runs (WBS 1.06.05)	Captures the required footprint for data acquired from the crystal validation runs and any computing resources that may be needed to analyze data

WBS 1.05.08 Integration: Requirements

- The integration subsystem has a requirement that the entire readout chain works together

Requirement	Value	WBS Level	High Level Requirement Connections	Top Level Science Requirement
Functional readout system	-	2		All

WBS 1.05.08 Integration: Conceptual Design

- This activity is dependent upon the other WBS 1.05 subsystems to provide functional prototypes to test integration
- As the prototyping process involves using all subsystems the development process tests integration
- A grounding scheme will be enforced on all installed components
- Final integration of the subsystems in Stage 1 and Stage 2 will occur onsite

WBS 1.05.08 Integration: Required R&D

- All interfaces between electronics boards are already defined
- Develop grounding plan

WBS 1.05.08 Integration: Risks

- Risks identified and put into risk registry with mitigation strategies suggested
- Most risks are associated with potential supply chain issues with electronics components or computing hardware
- Cost, Schedule Contingency are sufficient to cover the risks and uncertainty at this stage of the project
- No significant risks identified for this system due to nature of development process.

WBS 1.05.08 Integration: Interfaces

- Interface Control Documents started
- Keeps track of various interfaces between subsystems
- L2 manager responsible for top level document and delegate to L3 as appropriate

Interface	Description
Muon Veto (WBS 1.02.07)	Captures the required interface of the muon veto subsystem into the DAQ
Acoustic and Vibration Sensors (WBS 1.04.07)	Captures need to acquire auxiliary sensor data on digitizers
Front-end electronics (WBS 1.05.02)	Captures the front-end electronics as part of the readout chain integration.
Power Supplies and Pulsers (WBS 1.05.03)	Captures the power supplies and pulsers as part of the readout chain integration.
Filter and Digitizer (WBS 1.05.04)	Captures the filter and digitizer boards as part of the readout chain integration.
Software DAQ (WBS 1.05.05)	Captures the required interface between the DAQ and the digitizers and other electronics.

WBS 1.05: Budget

- Fully loaded resources for US costs
- IT and FR only M&S costs shown

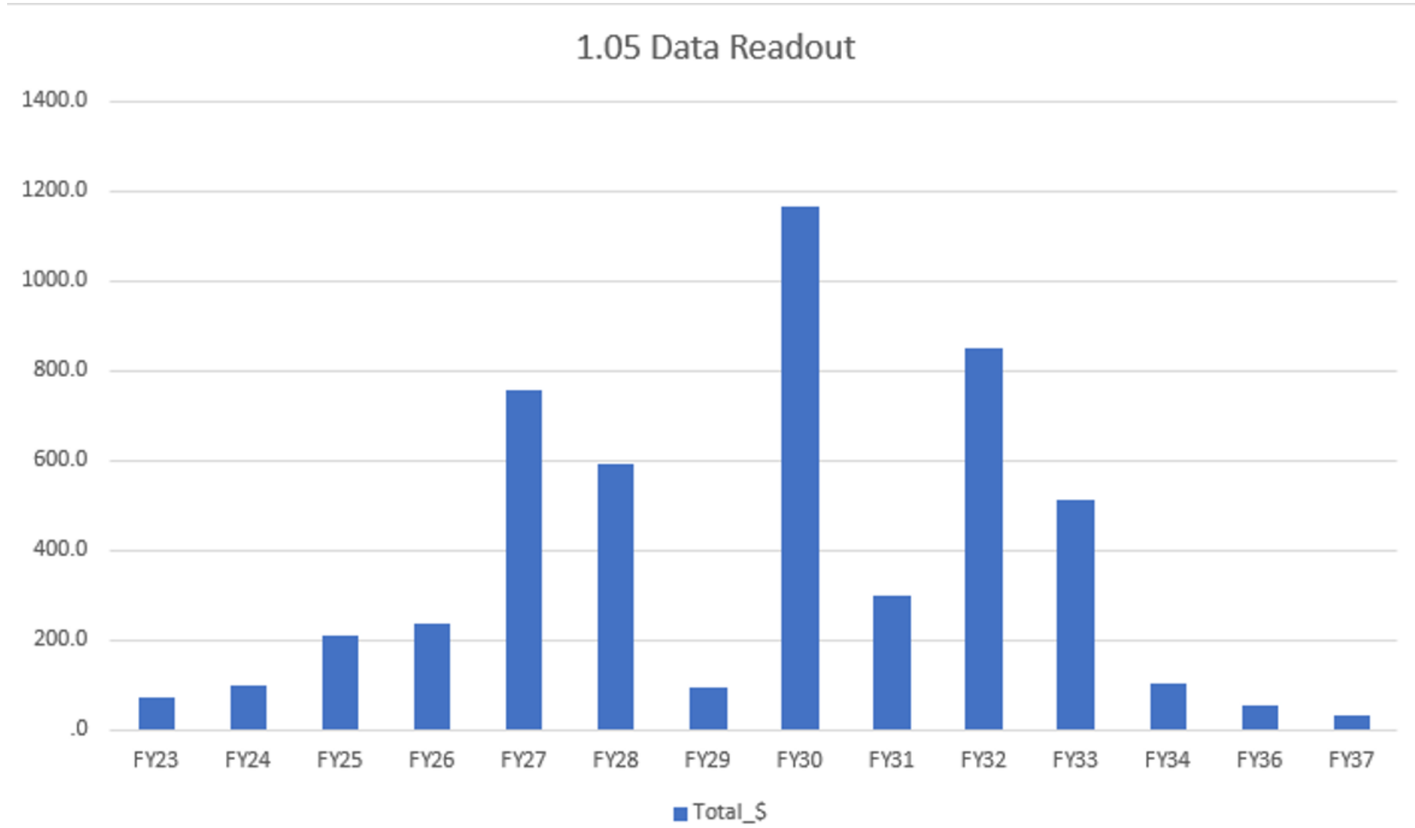
Sum of Value	Column Labels														
	Total_$														Total_$ Total
Row Labels	FY23	FY24	FY25	FY26	FY27	FY28	FY29	FY30	FY31	FY32	FY33	FY34	FY36	FY37	
US	69.4	99.1	210.3	238.3	756.9	591.2	93.1	1165.1	299.5	850.5	514.2	104.1	53.0	32.3	5077.0
Phase 1	69.4	99.1	210.3	238.3	756.9	591.2	93.1								2058.2
Phase 2								1165.1	299.5	850.5	514.2	104.1	53.0	32.3	3018.7
IT	72.6	74.4	199.6	111.2											457.7
Phase 1	72.6	74.4	199.6	111.2											457.7
FR		50.3	50.7	139.3	81.7						198.8	31.9			552.6
Phase 1		50.3	50.7	139.3	81.7										321.9
Phase 2											198.8	31.9			230.6
Grand Total	142.0	223.8	460.6	488.7	838.5	591.2	93.1	1165.1	299.5	850.5	713.0	136.0	53.0	32.3	6087.3

WBS 1.05: Budget

- Breakdown by FY in $k
- Costs reasonable for Staged deployment

Sum of Value	Column Labels
Row Labels	Total_$
Grand Total	5077.0

- Stage 2 has further procurement and addition of 1.05.02 to scope



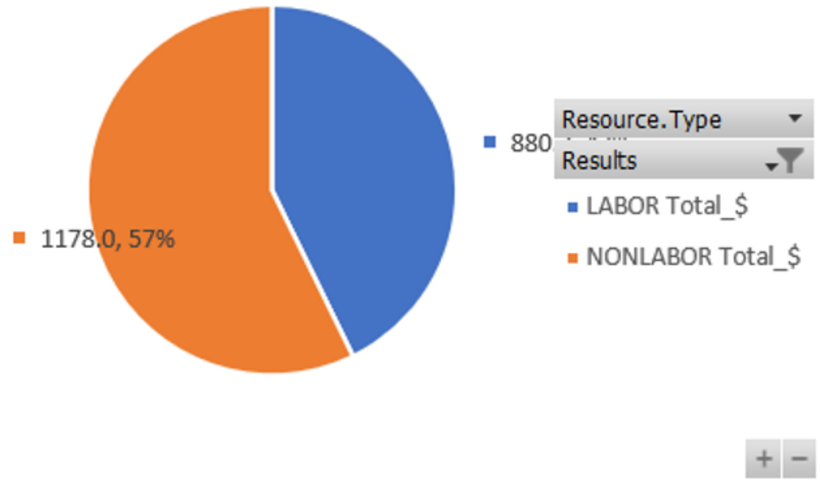
WBS 1.05: Budget

- Breakdown by WBS and Stage
- Stage 2 gains WBS 1.05.02 scope

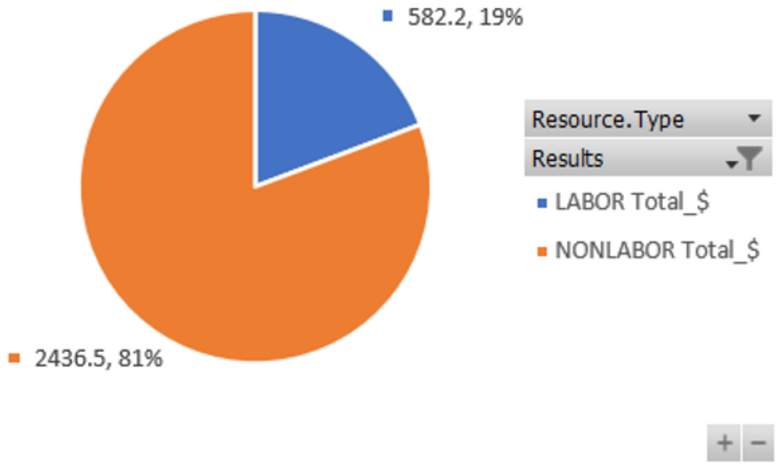
Sum of Value	Column Labels		
Row Labels	HOURS	DOLLARS	Total_$
US	22.5	2273.5	5077.0
Phase 1	15.8	869.5	2058.2
1.05 Data Readout	15.8	869.5	2058.2
1.05.01.01 Data Readout Management	2.3	53.4	352.2
1.05.01.02 OPC: Data Readout Management	.4	13.4	51.5
1.05.04.01 Electronics: Filters & Digitizers	4.3	313.3	620.7
1.05.05 SW DAQ & Trigger	4.7	51.5	199.6
1.05.06 Slow Control & Monitoring	1.7	30.8	101.5
1.05.07 Computing & Data Storage	2.4	307.1	612.6
1.05.08.02 OPC: Test Stand QC and Integration		100.0	120.1
Phase 2	6.7	1404.1	3018.7
1.05 Data Readout	6.7	1404.1	3018.7
1.05.01.01 Data Readout Management	2.6	66.8	539.4
1.05.01.02 OPC: Data Readout Management	.3	8.0	85.3
1.05.02.01 Preamps		165.9	350.6
1.05.02.02 Main Boards	1.5	360.2	781.6
1.05.04.01 Electronics: Filters & Digitizers	1.1	520.7	864.6
1.05.05 SW DAQ & Trigger		51.0	64.7
1.05.07 Computing & Data Storage	1.2	231.5	332.6
Grand Total	22.5	2273.5	5077.0

WBS 1.05: Personnel/manpower requirements

Stage 1

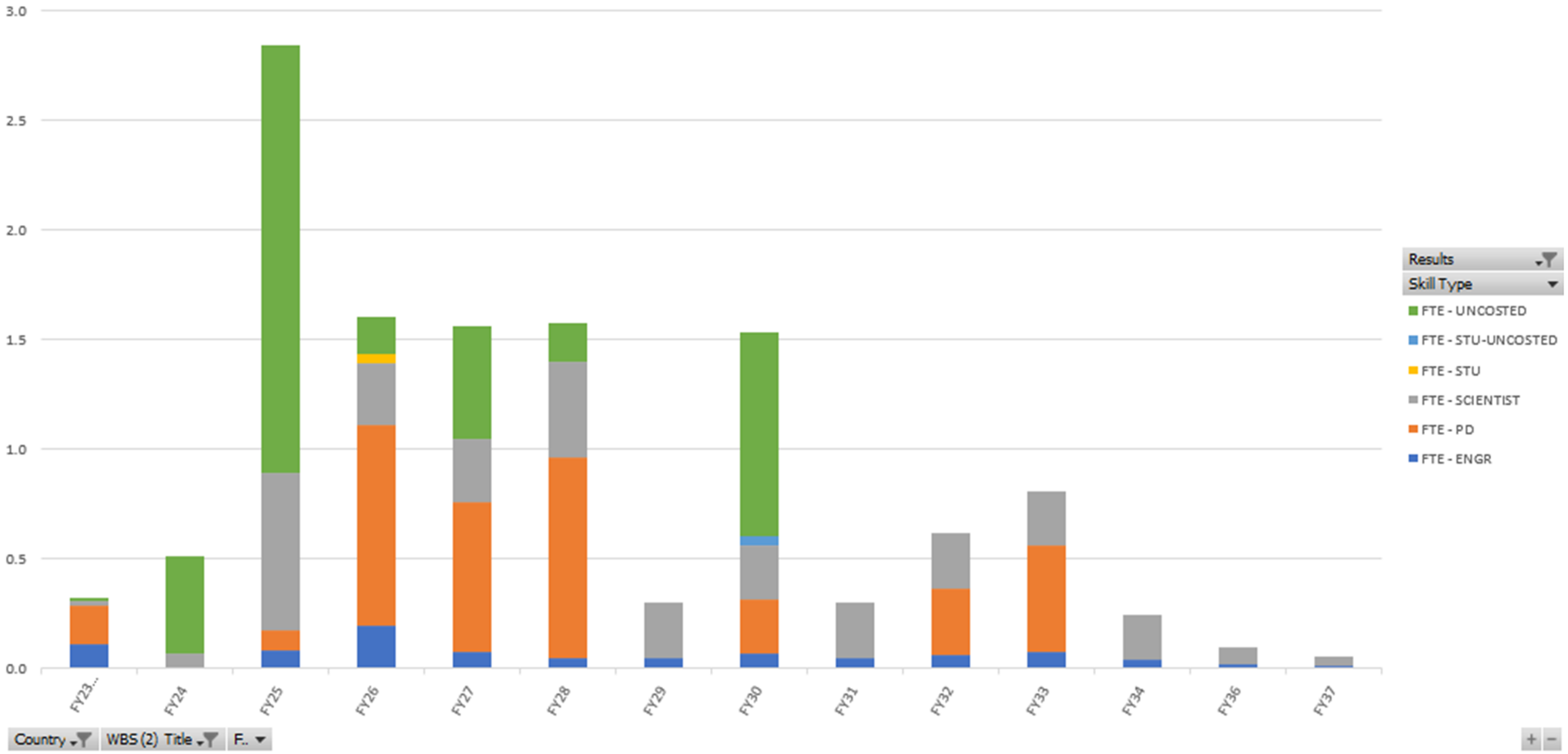


Stage 2



- Costs breakdown by Labor vs Non-labor
- Stage 2 increases non-labor costs due to additional scope + need to purchase 2/3 of subsystem hardware

WBS 1.05: Personnel/manpower requirements



- Labor allocation sufficient to cover Staged deployment stages
- R&D efforts and software development in Stage 1 diminish in Stage 2
- Uncosted labor means to take advantage of base grant support where possible

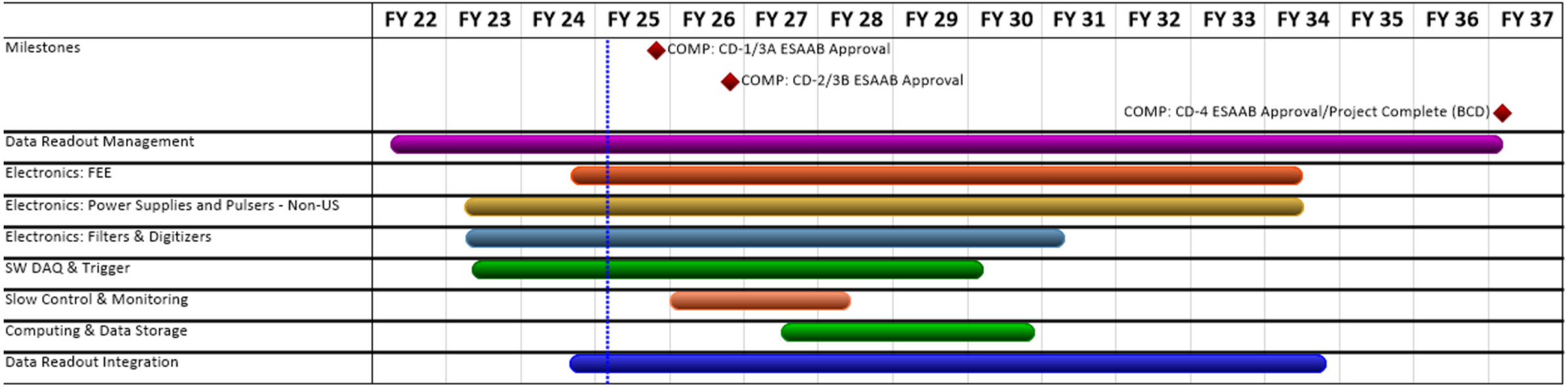
WBS 1.05: Personnel/manpower requirements

Sum of Value	Column Labels													
Row Labels	FY23	FY24	FY25	FY26	FY27	FY28	FY29	FY30	FY31	FY32	FY33	FY34	FY36	FY37
US	0.3	0.5	2.8	1.6	1.6	1.6	0.3	1.5	0.3	0.6	0.8	0.2	0.1	0.1
Phase 1	0.3	0.5	2.8	1.6	1.5	1.6	0.3							
BU	0.0		0.0	0.0	0.1									
LBNL			0.0	0.1	0.1	0.1	0.1							
MIT	0.0	0.1	0.5	0.0	0.0	0.2								
UCB	0.0		0.3	0.2	0.2	0.2	0.3							
UCLA	0.3		0.2	0.3	0.5	0.8								
UNCOSTED	0.0	0.4	2.0	0.2	0.5	0.2								
PITT				0.7	0.1	0.1								
Phase 2					0.0			1.5	0.3	0.6	0.8	0.2	0.1	0.1
BU								0.1		0.3	0.5			
LBNL								0.1	0.0	0.0	0.0	0.0	0.0	0.0
UCB								0.2	0.2	0.2	0.2	0.2	0.1	0.0
UCLA								0.2						
UNCOSTED					0.0			1.0						
Grand Total	0.3	0.5	2.8	1.6	1.6	1.6	0.3	1.5	0.3	0.6	0.8	0.2	0.1	0.1

- Labor breakdown by US institution

WBS 1.05: Schedule

- Fully loaded schedule accounting for Staged deployment
- Not on the critical path in Stage 1
- In Stage 2 on critical path due to desire to purchase computing hardware late as possible
  - Can be pulled in if necessary



WBS 1.05: CDR Review Response

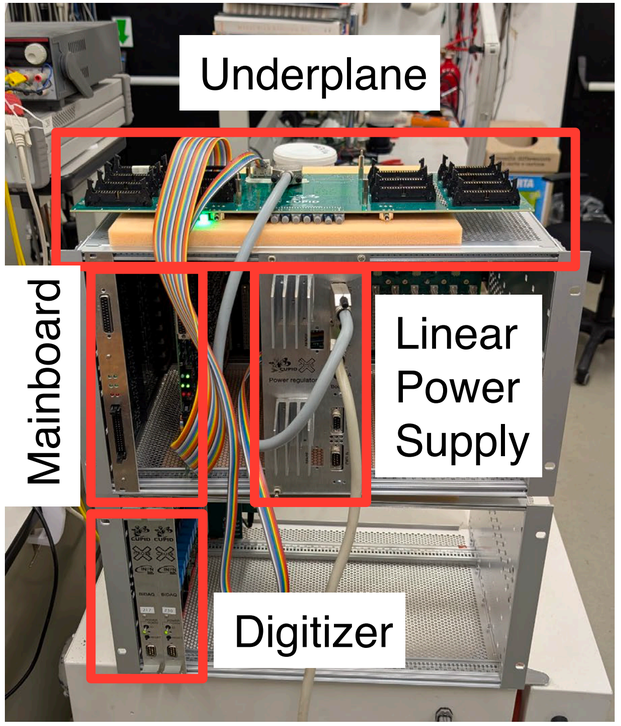
- CDR review last year
- Several recommendations by review committee
- Item 1
  - A: Accomplished with requirements table
  - Wire capacitance is an issue, technical design parameters of FEE chosen to minimize impact on science goal
  - Cross-talk requirement on the wiring set and has link to total background
- Item 2
  - ICDs now exist
- Item 3
  - Added as risk 105020075
- Item 4
  - WBS 1.05.07 responsible for ensuring best practices adhered to
  - Note: we are behind host lab network firewall for added security
- Item 5
  - Added as Risks 105040100 and 105020123

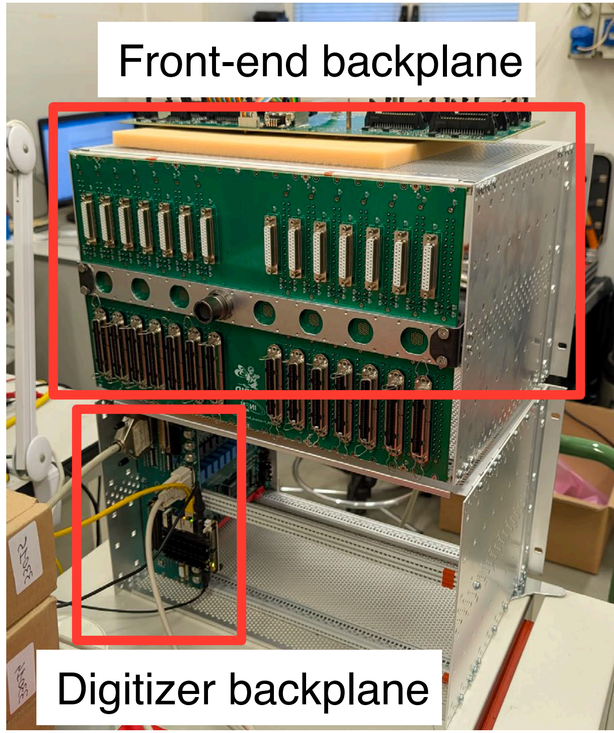
Recommendations

1. Update requirements documentation to reflect the flow down from Science
   a. Explicitly list requirements that drive design decisions and flow down from the science needs of the experiment.
   b. Additionally, what aspects of the design limit the physics capabilities of the experiment, e.g. capacitance of FE cabling limiting energy resolution? Driving source of electronic noise?
   c. In addition, list the electronic cross-talk in the requirements justified from flow-down
2. Create draft Interface Control Documents to at least capture the scope and nature of the interfaces. Consider capturing this at the L2-L2 level to decrease the number of documents.
3. Add a risk to the registry to capture the possibility that the power dissipation in the FEE cannot be improved as much as is expected, including resulting degradation of thermal control and performance.
4. In future reviews, include information about the approach to cybersecurity in addition to which WBS element is ultimately responsible for its design and execution.
5. Consider adding a risk to the registry to capture the possibility that electrical component lead times are longer than anticipated due to supply chain issues.

WBS 1.05: Summary

- Ready to go
- Electronics systems are technical refreshes of existing CUORE designs with specific optimizations to CUPID requirements
- New integrated digitizer+filter boards well motivated and mature
- Computing resources easily covered with commercial hardware and existing cluster resources
- Risks are manageable
- WBS 1.05 has a high technical readiness due to proven designs from CUORE, and use of commercial hardware for computing infrastructure
- Prototypes meeting specifications exist





Prototypes of CUPID electronics chain