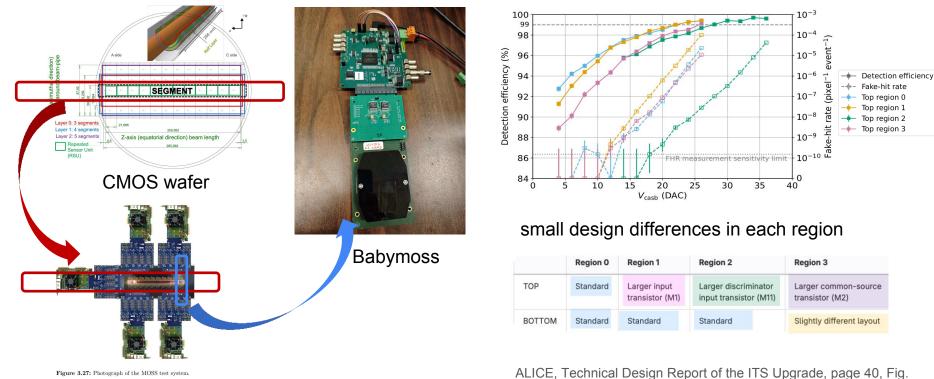


Study of the baby-moss @ L268

Zhenyu Ye, and Yu Hu (胡昱) for LBL group

Babymoss - from ALICE ITS report



3.30; page 46, Fig. 3.33

Figure 3.27: Photograph of the MOSS test system.

MOSS

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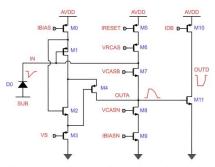
Default setups

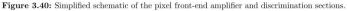
DAC units:

IBIAS = 62 IBIASN = 100 IDB = 50 IRESET = 10 VCASB = 15 VCASN = 64 VSHIFT = 192

A. W21D4 S3 CHIP3 B. W20E1 S2 CHIP1 C. W20E1 S2 CHIP3







Short term target:

- Understand the performance of the baby-moss under different configures (Vcasb dependence..)
- The temperature dependence of the noise level
- The performance after the radiation expose

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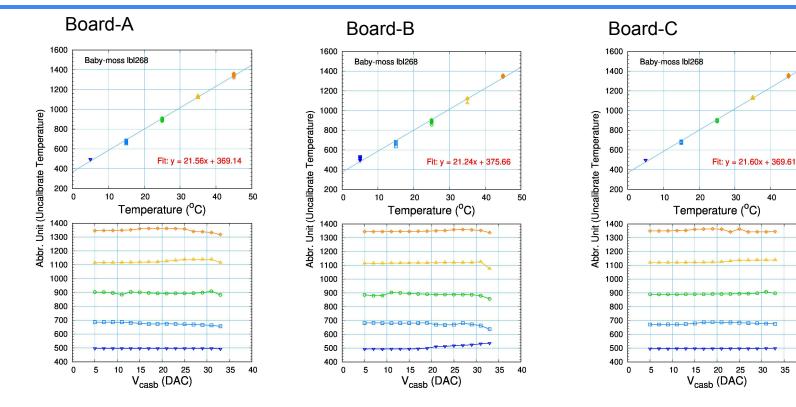
Temperature test with climatic chamber



- We scaned 5°C, 15°C, 25°C, 35°C, 45°C with different V_{casb} using the climatic chamber
- As a calibration to the on-board thermistor

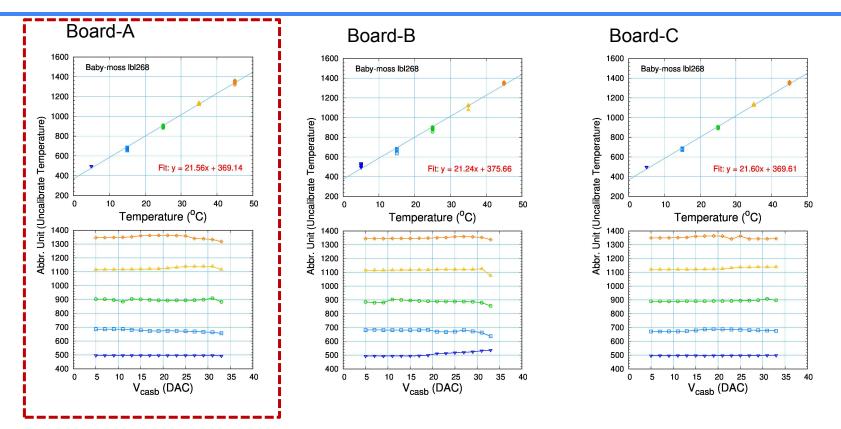


Temperature calibration



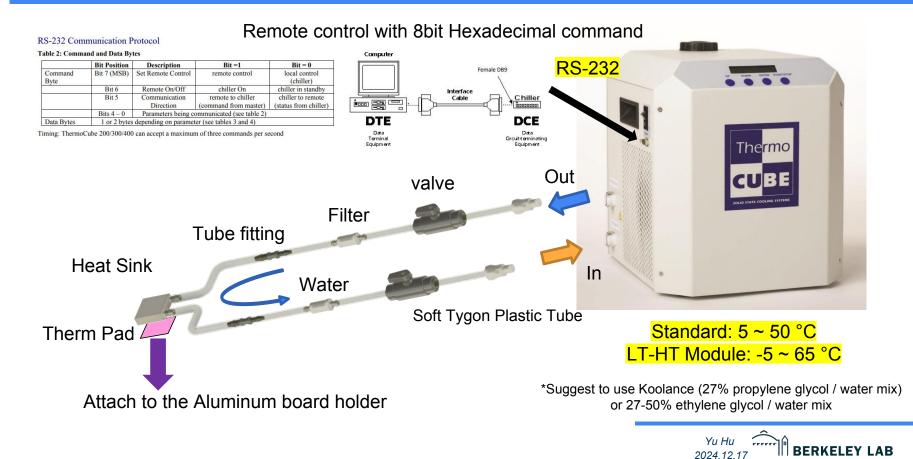


Temperature calibration

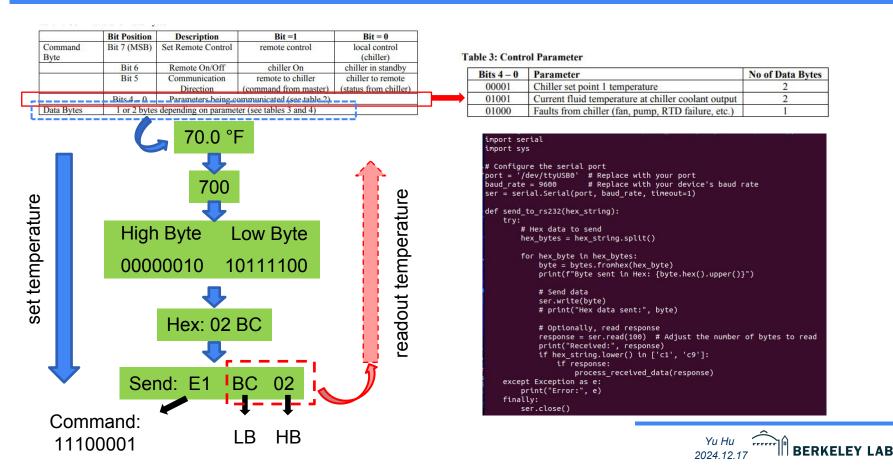




Cooling loop layout



Slow control for the cooling unit

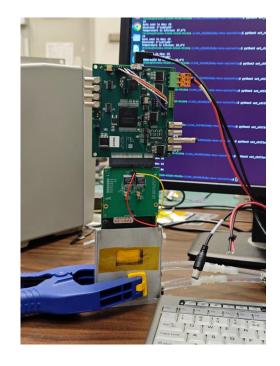


8

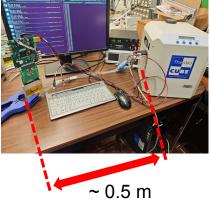
Testing system @ L268

Board-A









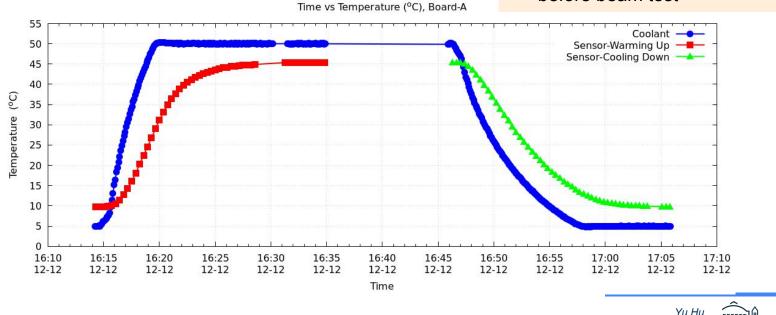


Heating/Cooling efficiency

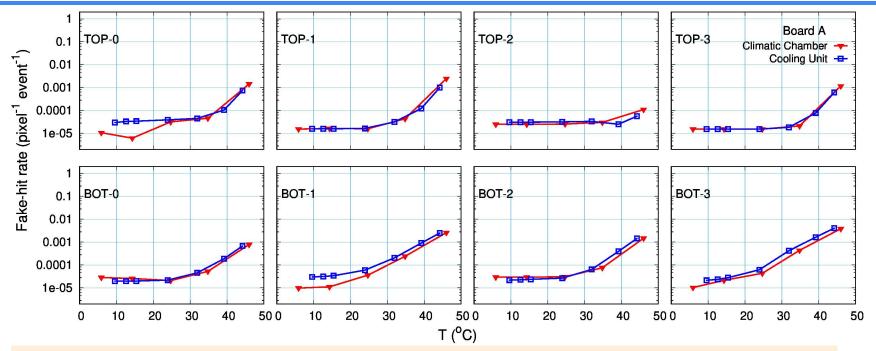
Chiller Temp (°C)	Thermistor Readout (Arb.)	Thermistor Readout (°C)
5	576	9.6
50	1344	45.2

- Under the current configuration, we could reach 10~45 °C within 10 mins.
- We expect a longer time & narrower range once using a longer tube - will test before beam test

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Compare with the tests using climatic chamber



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- FHR are consistent with the tests using climatic chamber
- Slightly higher FHR for TOP-0 and BOT-1 with our cooling unit
 - Light? Will check with a dark tape covered

Summary & Outlook

- We successfully built an efficient cooling loop for the babyMOSS test
- Under the current configuration, we could reach 10~45 °C within 10 mins.

- Threshold scan on-going
- Heating/Cooling efficiency test with longer cooling loop
- Test with Board A,B,C prepare for the beam test @ UC Davis
- Test configurations @ UC Davis



Cyclotron @ UC Davis

Produce high-intensity, external beams of light ions that can be tuned to energies between 4 MeV and 67.5 MeV. The primary particles accelerated are protons, deuterons, helions and alphas.







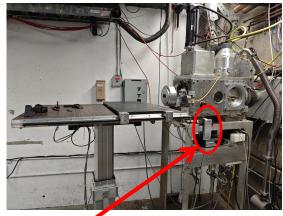
- Scheduled time: 2025.01.21
- Will not take the cooling unit consider the following beam test @JLab

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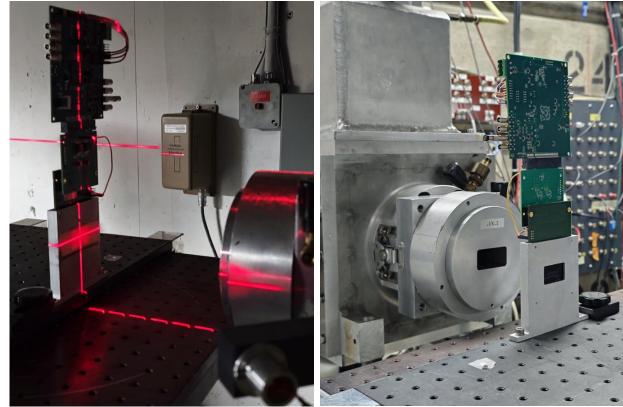
2024 12 17

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Plans for the beam test @ UC Davis

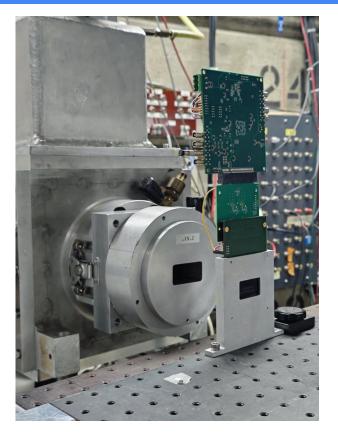


- Controller to adjust the XY position with remote control available
- Two real-time cameras to monitor
- Beam dose monitor/counter
- Different shapes of beam filter/cover, size/shape adjustable





Plans for the beam test @ UC Davis



8 hours testing:

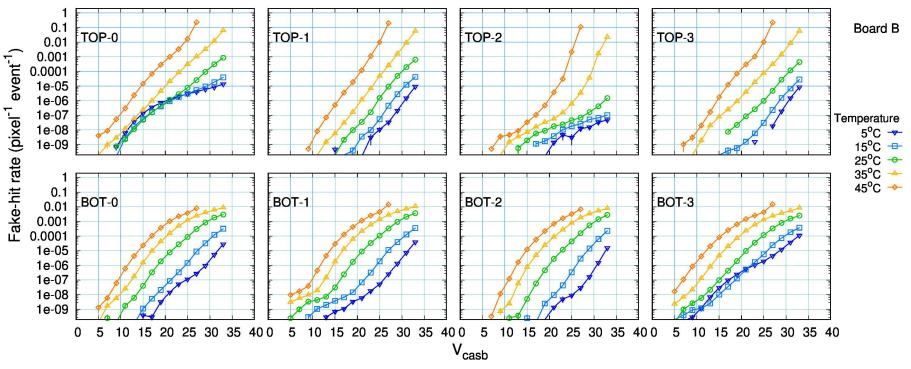
- Goal: Chip expose test under different times/dose
- Plans:
 - 3 babyMOSS (expose) + 1set of readout board (shielded);
 - Expose 3 babyMOSS with different doses (time) change the chips in the middle (~ 5 mins to restore beam);
 - Constantly running FHR tests all the time in the background
- Before the beam tests:
 - Threshold scan under different temperature;
 - Comunicate to the desktop with UC Davis local network/internet





Materials from the last presentation

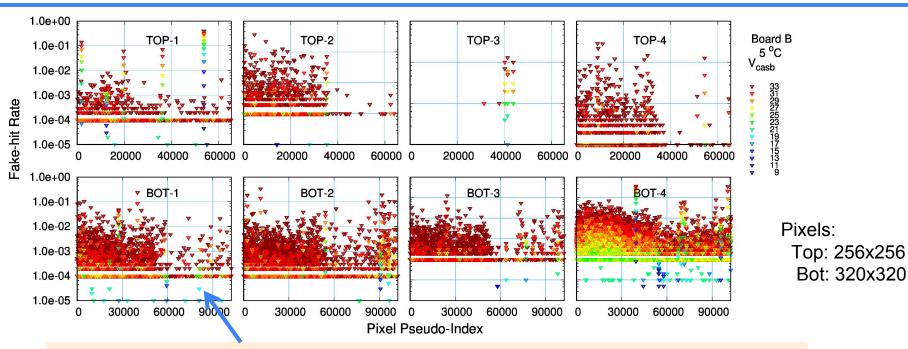
FHR vs V_{casb} @ different T



lower temperature gives the lower Fake-Hit Rate (FHR)



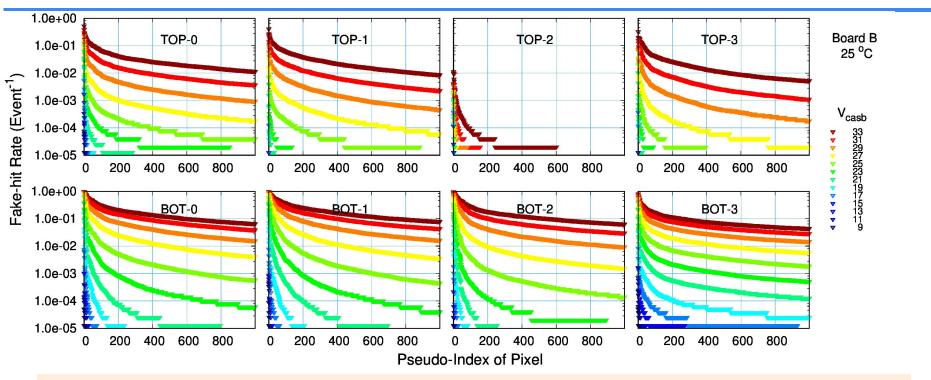
Where are the hot pixels?



- 2D hit map are very random, so shown a Psedo-index vs FHR (eg. Index = X*256+Y)
- Some of the pixels are fired every time, which should be masked out
- Most of the pixels are random fired



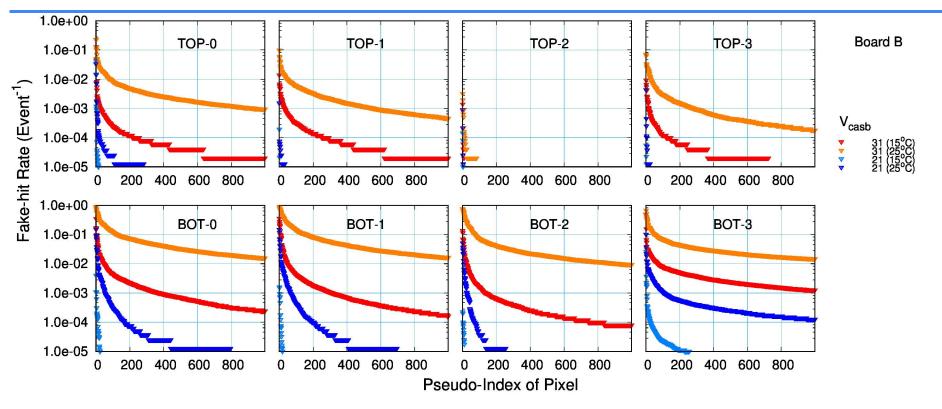
FHR vs Pixel Index @ 25 C



- In total: TOP: 256x256=65536 Pixels; BOT: 320x320=102400 Pixels
- Reorder all the Psedo-index form high to low, and plot it vs FHR

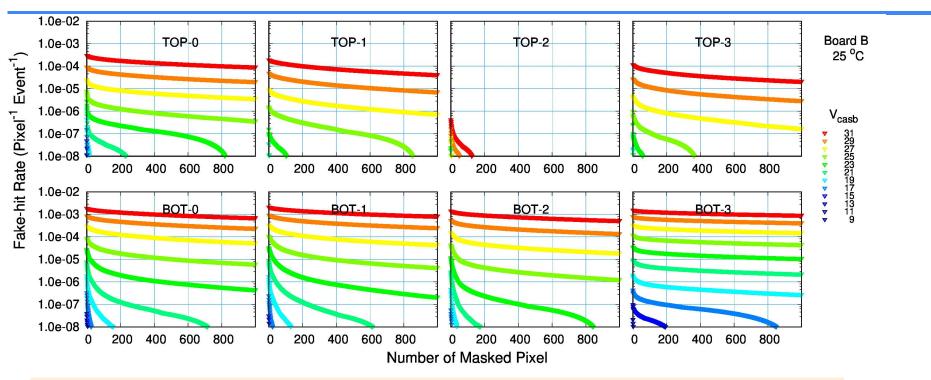


FHR vs Pixel Index @ different T



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FHR vs Number of Masked Pixels



• FHR as a function of number of masked Pixels



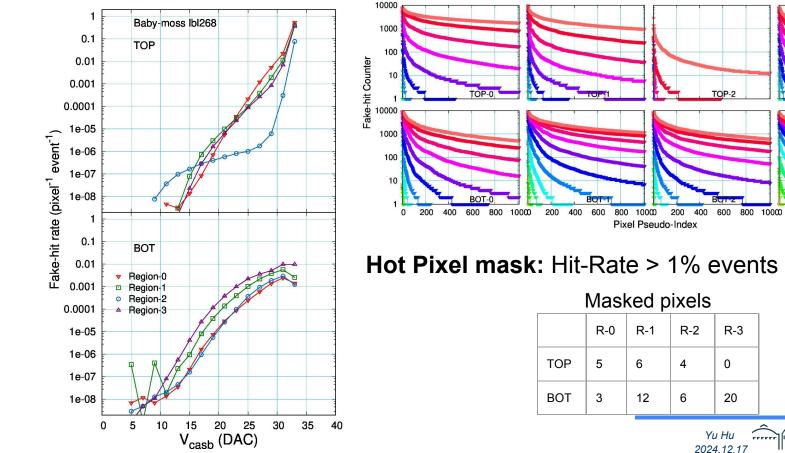
Summary and Outlook

- We studied the FHR at different temperatures with different Vcasb
- Calibrated the on board thermistor (last presentation)
- We will build the cooling loop by ourselves for the future beam test, study the performance of the cooling loop





Board A - W21D4 S3 CHIP3 (20240906) - 10k events



TOP-3

BOT-3

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800 1000

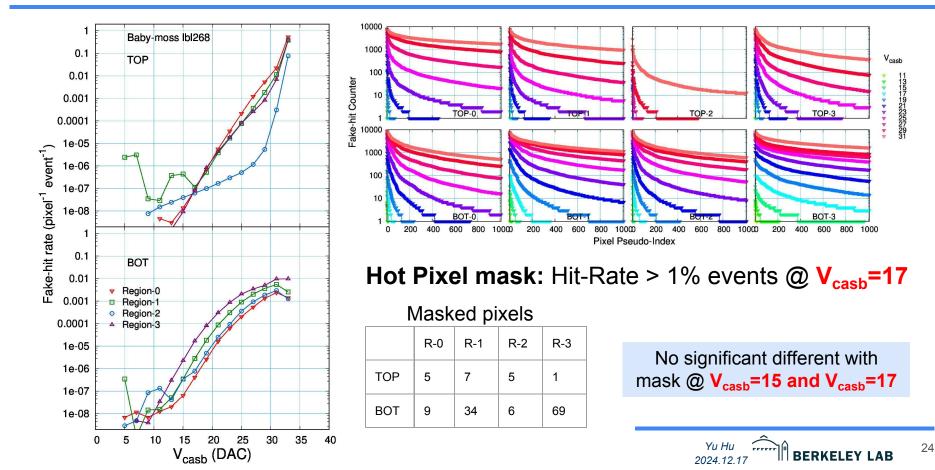
200 400 600 Vcasb

Hot Pixel mask: Hit-Rate > 1% events @ V_{cash}=15

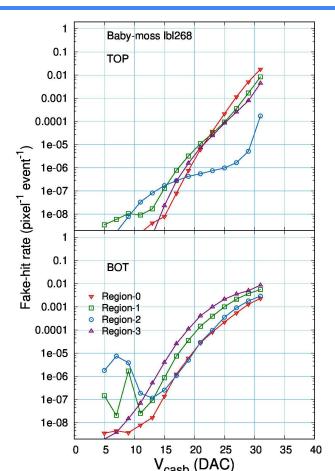
	R-0	R-1	R-2	R-3
TOP	5	6	4	0
BOT	3	12	6	20

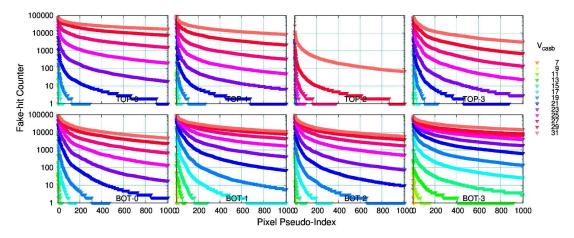
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Board A - W21D4 S3 CHIP3 (20240906) - 10k events



Board A - W21D4 S3 CHIP3 (20240918) - 100k events





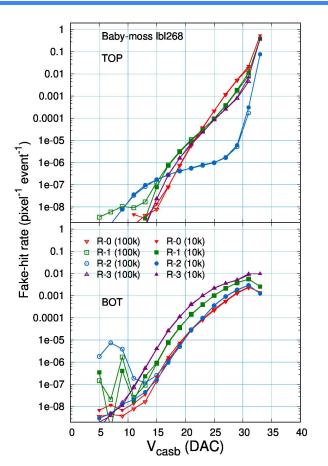
Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=15

Masked pixels

	R-0	R-1	R-2	R-3
ТОР	4	5	3	0
вот	6	13	6	18



10k vs 100k



10k

Masked pixels					
R-0 R-1 R-2 R-3					
TOP	5	6	4	0	
BOT	3	12	6	20	

100k

Masked pixels

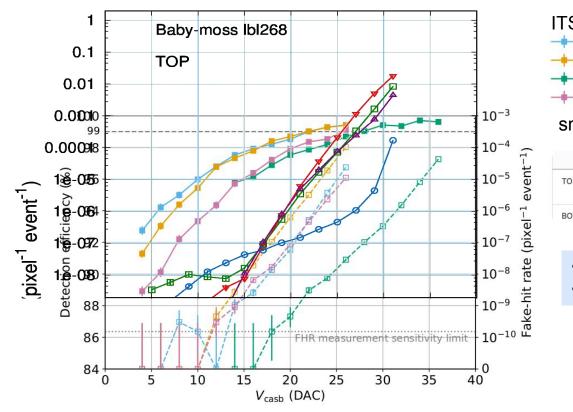
	R-0	R-1	R-2	R-3
TOP	4	5	3	0
BOT	6	13	6	18

No significant difference with 10k or 100k events

10k should be sufficient enough for this test



Layer-over comparison with ALICE tests





small design differences in each region

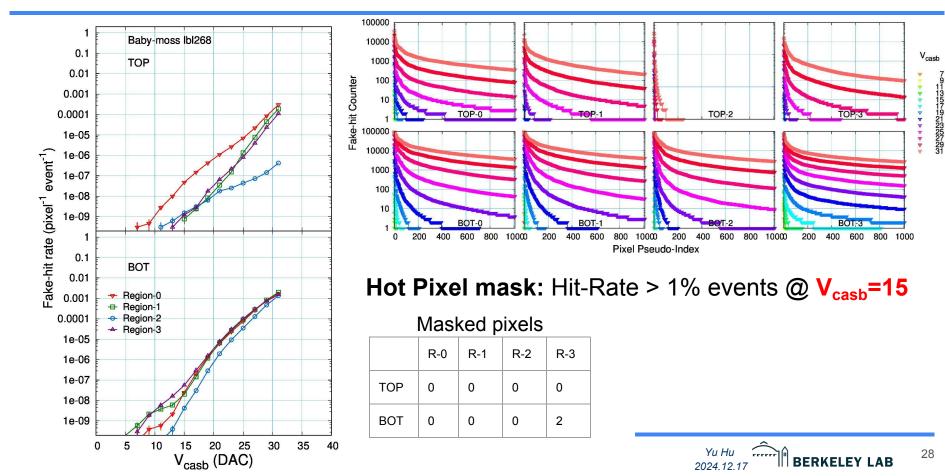
	Region 0	Region 1	Region 2	Region 3
ТОР	Standard	Larger input transistor (M1)	Larger discriminator input transistor (M11)	Larger common-source transistor (M2)
воттом	Standard	Standard	Standard	Slightly different layout

- Good consistence for Region-0,1,3
- Some differences for Region-2

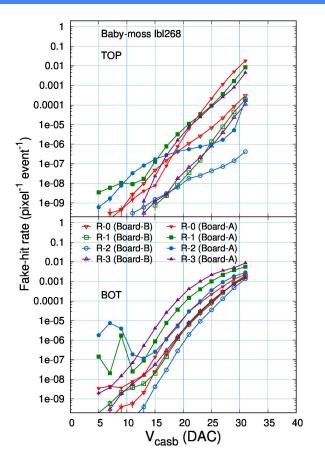
Individual differences?

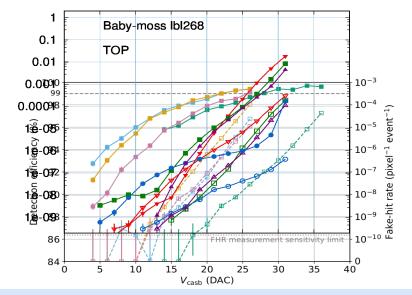


Board B - W20E1 S2 CHIP1 (20240918) - 100k events



Board-A vs Board-B





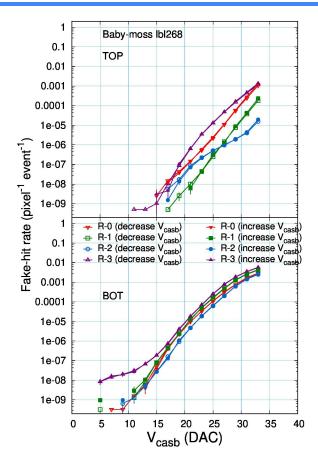
- The performance of individual chips has noticeable differences
- The trend of the Fake-hit rate (also checked Board-C) is consistent with the example in the ALICE ITS report

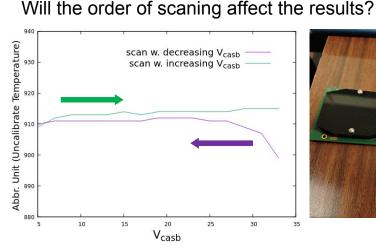
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Order of scaning - w. Board-C



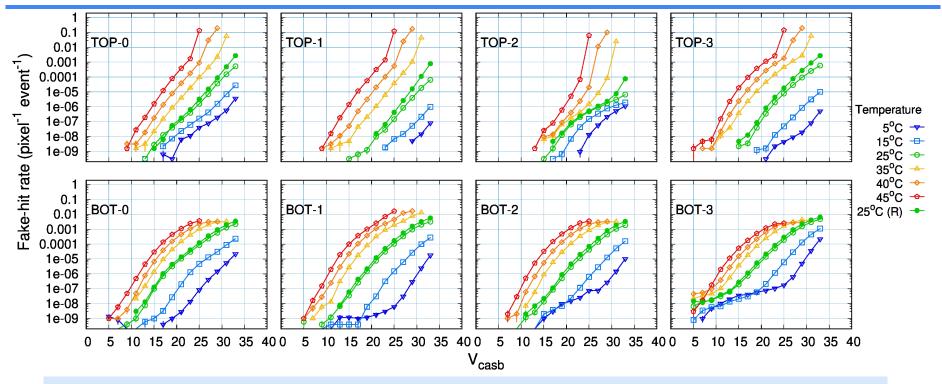




- The temperature read by thermistor resistance shows some difference (electronic warming up) - the scale is unknown
- No significant difference in Fake-hit Rate no matter scanning from large or small Vcasb in the current scale



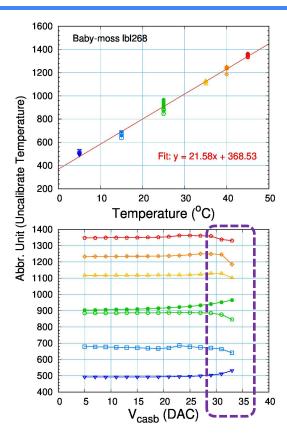
Fake-hit Rate vs Temperature (Board-C)

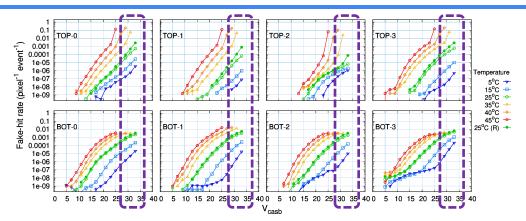


- High Temperature \rightarrow High noise, as expected
- Noise levels are consistent at the same temperature after a run in a hot temperature (45°C)



Temperature sensor (thermistor resistance)







- There are some small variation at the beginning of the test
- The thermistor resistance follows the linear relation to the set temperature



For Fake Rate Test:

- No significant different with masking @ Vcasb=15 and Vcasb=17
- No significant difference with 10k or 100k events 10k should be sufficient enough
- Good consistence for Region-0,1,3, some differences for Region-2 compare with ALICE report
- The performance of individual board has noticeable differences, the trend of the Fake-hit rate are consistent
- No significant difference in Fake-hit Rate no matter scanning from large or small Vcasb in the current scale

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Test with Climatic Chamber:

- High Temperature \rightarrow High noise, as expected
- Noise levels are consistent at the same temperature after a run in a hot temperature (45°C)
- The thermistor resistance follows the linear relation to the set temperature

To to next:

- Temperature test with other boards
- Noise test after radiation exposure

DAC units: IBIAS = 62 IBIASN = 100 IDB = 50 IRESET = 10 VCASB = 15 VCASN = 64 VSHIFT = 192

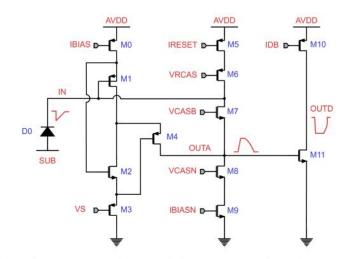
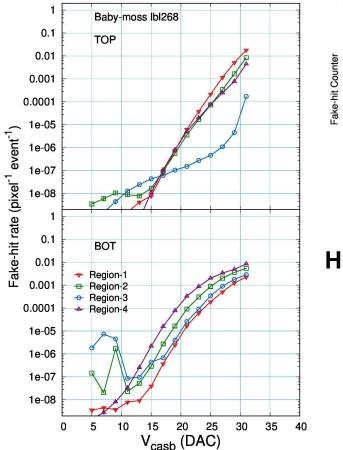
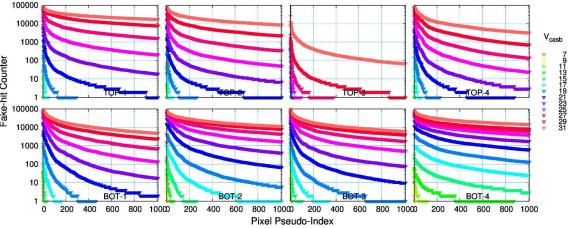


Figure 3.40: Simplified schematic of the pixel front-end amplifier and discrimination sections.



Board A - W21D4 S3 CHIP3 (20240918) - 100k events





Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=17

Masked pixels

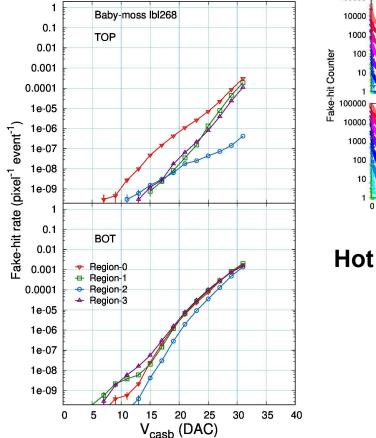
	R-0	R-1	R-2	R-3
TOP	4	7	4	1
вот	11	35	8	67

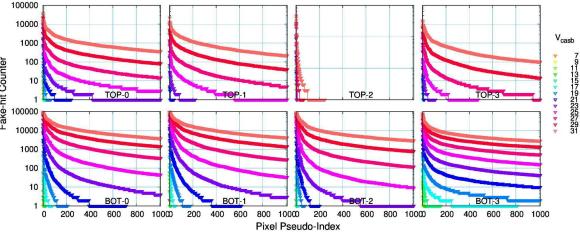
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Board B - W20E1 S2 CHIP1 (20240918) - 100k events





Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=17

Masked pixels

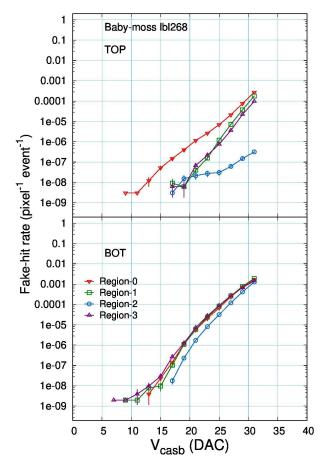
	R-0	R-1	R-2	R-3
TOP	0	0	0	0
вот	0	0	0	2

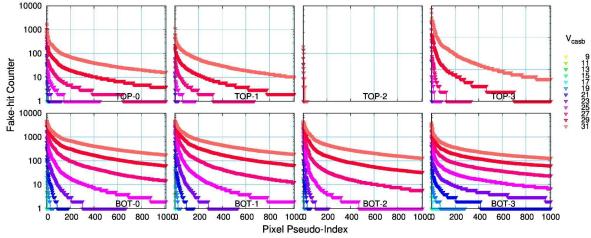
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Board B - W20E1 S2 CHIP1 (20240918) - 5k events





Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=15

Masked pixels

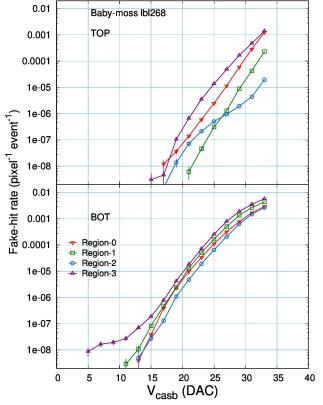
	R-0	R-1	R-2	R-3
TOP	0	0	0	0
вот	0	0	0	2

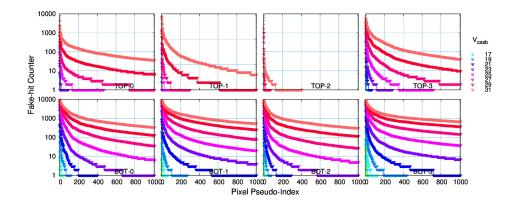
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Board C - W20E1 S2 CHIP3 (20240924) - 10k events





Hot Pixel mask: Hit-Rate > 1% events @ V_{casb}=15

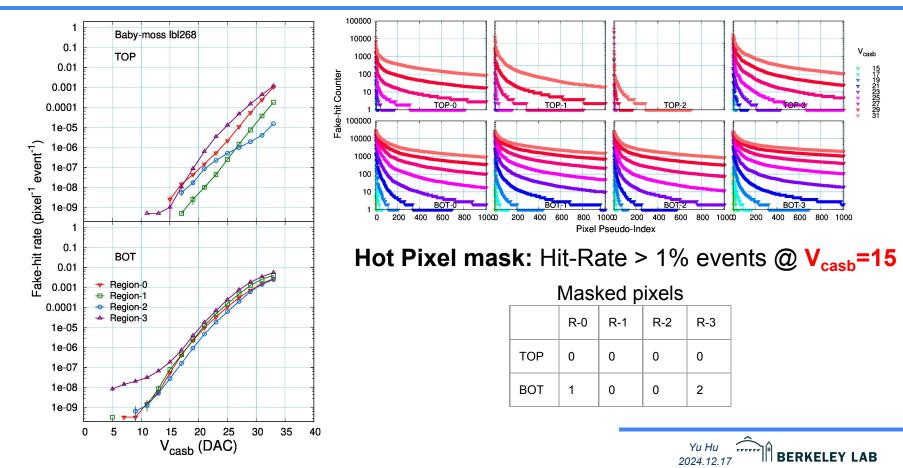
Masked pixels

	R-0	R-1	R-2	R-3
ТОР	0	0	0	0
BOT	1	0	0	2

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Board C - W20E1 S2 CHIP3 (20240924) - 30k events



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