

Analog Photon Processor

Workshop on Hybrid Cherenkov/Scintillation Detection Technologies

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APP concept

- Motivation:
 - We are interested in the number of photoelectrons (PE), and their arrival times
- Can we avoid full digitization?
 - Petabytes exabytes per year in 10⁴ channel systems
 - Power hungry
 - High cost
 - Resolution and dead time (closely spaced pulses)
- Need these parameters to characterize an arbitrary PMT pulse:
 - Leading edge time
 - Trailing edge time get time over threshold (TOT) from edge times
 - Peak amplitude
 - Peak time
 - Total charge (Q)
- Timing resolution limited to an extent by photomultiplier tube transit time spread (TTS)





PE measurement and counting

- How can we determine #PEs ?
- Maximum likelihood estimation
 - Calculate 3-D probability density functions using TOT, Q, peak
 - Obtain good estimate of number of PE in a pulse for 1—8 PE
 - Proof of concept that we only need a few measurements
- Frequency domain
 - Convolve filter response of ideal lognormal pulse with input signal
 - Sensitive to filter kernel, aliasing problems
- Many other approaches: matched filter, interpolation, etc.
- Many approaches work best offline, or are difficult to implement with electronics



PE measurement and counting, cont.

- We can do this with an ASIC, with local analog memory, read out with low cost ADC
- Analog circuit blocks
 - Peak detector
 - Integrator
 - Time to amplitude converter (TAC)
- SNO did this to some extent with TAC, charge (fixed windows)
 - No timing information on second hit
- Some older work in $0.35 \mu m$ process
 - Not good for modern tubes with subns TTS
- Some ASICs exist for this purpose, but "photon counting" mostly





What happens in this case?



Basic requirements of APP

- We'd like to capture PMT pulses with:
 - Risetimes ~1ns or less
 - FWHM ~5ns or less
 - Better than 100ps timing (limited by TTS)
 - ~5—500mV amplitude (up to 100 PE)
 - After 50 PE, probably most information in Q
 - After 1000 PE, tube saturation
 - Motivates 2 gain paths
- Charge integral up to a few microseconds
 - Programmable window for "late" scintillation light
 - After a few unresolved PE, most information also in Q
- We want to re-trigger
 - To catch closely spaced resolved PE
 - Motivates "analog FIFO"
- 1—4 channel chip
 - Channel density probably limited by cables in a PMT system not true for pixelated detectors!



- 1. Leading edge of TOT "event"
- 2. Trailing edge of TOT event
- 3. Integral of TOT event (charge)
- 4. Time of 1st peak in the event
- 5. Amplitude of 1st peak in the event
- 6. Time of 2nd peak in the event
- 7. Amplitude of 2nd peak in the event
- 8. Time of 1st valley in the event
- 9. Amplitude of 2nd valley in the event
- 10. Integral of total charge over a programmable time starting with the 1st event

(Not every measurement needed for every application)

Block diagram (very simplified)





Peak detector circuit simulation

Using TSMC 65nm process



Example #1

- Ping-pong architecture can store 2 closely spaced peaks
 - Second peak is counted as a separate event, and measurements #6—9 are not stored
 - The "long charge" measurement #10 is always a separate analog memory



Metadata: **b111110000** – valid memory locations 4 **timestamps** – leading/trailing edge 1 **timestamp** – "long charge"

Example #2

- Ping-pong architecture can store 2 closely spaced peaks
 - Second peak is counted as a separate event, and measurements #6—9 are not stored
 - The "long charge" measurement #10 is always a separate analog memory
 - If a second peak is never resolved, measurements #6—9 are stored



Metadata: **b11111111** – valid memory locations 2 **timestamps** – leading/trailing edge 1 **timestamp** – "long charge"

Full channel analog simulation

8 memories

buffer mode



cocotb simulation flow



Behavioral model of analog blocks – fast simulation time

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Preliminary area estimate





Conceptual system (a few channels)





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Conceptual system (a detector)



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Next steps

- Many APP analog blocks are complete or nearly complete
- Digital logic being written/simulated
- We are designing a test structure/demonstrator for APP:
 - Commercial FPGA, Ethernet readout
 - 14 bit commercial ADCs with convert trigger, not continuous sampling (ENOB closer to ~12b, really only need 8—10b)
 - ~300 uV / count
 - sub 10ps TAC resolution
 - Probably limited by digitization time
 - Support: calibration, analog sum, trigger, etc.



Example fast comparator layout



Thank you!

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