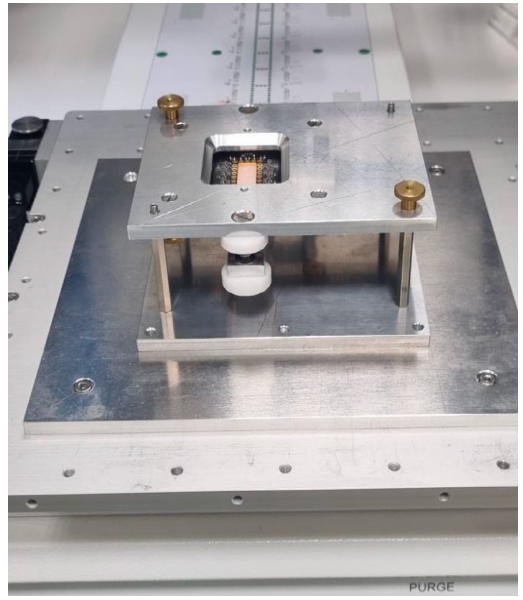
Tasks on Sensorsand Electronics towards TDR

- **SVT Sensor**
  - **ER1 Sensor (babyMOSS)**
    - **FNAL Beam Test:** Data taken in 5-6/2024 by **Tucker**, Danush (UIC); results on incident angle dep. presented at HP2024 by Tucker
    - **BASE SEL Test:** Data taken in 5&7/2024 by Anjali et al.; results reported to ITS3 in 9/2024 by Zhenyu
    - **Davis TID/NIEL Test:** Data taken in 1/2025 by Austin, Shujie, **Yu**, Zhenyu; FHR/THR (see Yu's talk on 5/6) to be reported to ITS3
    - **JLab Beam Test:** Data taking in 4/2025 by **Yu**, Provakar and Zhenyu. Data analysis to be completed by Yu by 6/2025
    - **Assembly onto carrier cards:** Phat (LBL Tech), Nicholas Gellerman (UCB ME UG). Two boards completed. Twenty by 7/2025
  - **ER2 Sensor (MOSAIX)**
    - **Submission:** 6/2025, Receive by the end of 2025
    - **Bench/Beam Tests in EU for ALICE ITS3:** 2026
    - **Bench/Beam Tests in US for SVT (and ITS3):** 2026 (TBC)
  - **EIC-LAS Sensor**
    - **Design & Characterization:** TBC



Tasks on Sensors and Electronics towards TDR

- **SVT AncASIC**
  - **SLDO (serial powering)**
    - **Design:** pre-regulator designed by Amanda Krieger included in 3/2025 submissions by BNL and RAL, receive in 9/2025
    - **Characterization:** 10/2025-3/2026 (TBC)
  - **AncBrain (slow control)**
    - **Design:** FPGA emulation work by Zhengwei ongoing, to be included in 8/2025 submission by BNL, receive in 3/2026
    - **Characterization:** 5/2025-4/2026 (TBC)
- **SVT Readout**
  - **lpGBT/VTRx+**
    - **SVT:** use lpGBT with AncBrain for slow control, use VTRX with sensor for high-speed data
- **SVT Flexible Printed Circuit Board (FPC)**
  - **Disk FPC Prototype**
    - **1st engineering prototype**: Zhengwei/Zhenyu work with LTU to define/design/test the prototype
  - **Domestic Vendor**
    - **OMNI:** Zhenyu/Zhengwei in discussion about 3rd iteration prototype, design in progress
- **AC-LGAD**
  - **BTOF Sensor/ASIC**
    - **Beam Tests:** JLab/DESY in July 2025

SVT WP3 – Electrical Interface

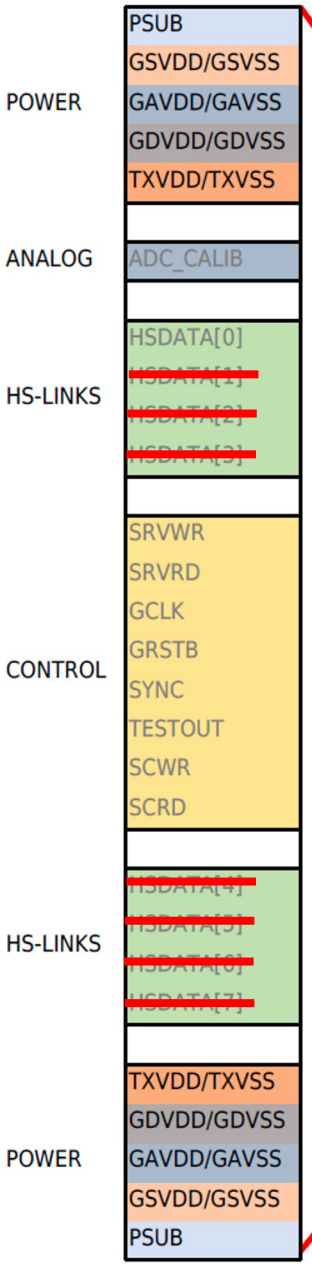
- IT: Trieste
- US: BNL, LANL, LBNL
- UK: Birmingham, Daresbury, Liverpool, Oxford
- UA: RPE LTU

WP3: Electrical Interfaces
Coordinators: Marcello Borri, Zhenyu Ye

WP3: Electrical Interfaces		
3.1	Electrical interfaces IB (L0—2)	
3.1.1		Definition of specifications for FPCs & electrical interconnection
3.1.2		Design & supplier evaluation
3.1.3		Prototyping & testing of module, FPCs & electrical interconnection
3.1.4		Iterative improvements of FPC design & electrical interconnection
3.1.5		FPC design complete & electrical interconnection validated
3.1.6		Pre-production of FPCs for system test, including QC
3.1.7		Production of FPCs for production detector, including QC
3.2	OB HIC (L3--4)	
3.2.1		Definition of specifications for module, FPCs & electrical interconnection
3.2.2		Design & supplier evaluation
3.2.3		Prototyping & testing of module, FPCs & electrical interconnection
3.2.4		Iterative improvements of module design, FPC & electrical interconnection
3.2.5		OB module design complete
3.2.6		Pre-production of FPC for system test, including QC
3.2.7		Production of FPCs for detector grade modules, including QC
3.3	Disks HIC (ED0-4, HD0-4)	
3.3.1		Definition of specifications for module, FPCs & electrical interconnection & back plate
3.3.2		Design & supplier evaluation
3.3.3		Prototyping & testing of module, FPC, electrical interconnection & back plate
3.3.4		Iterative improvements of module design, FPC, electrical interconnection & back plate
3.3.5		Disk module design complete
3.3.6		Pre-production of FPCs for system test, including QC
3.3.7		Production of detector grade FPCs, including QC

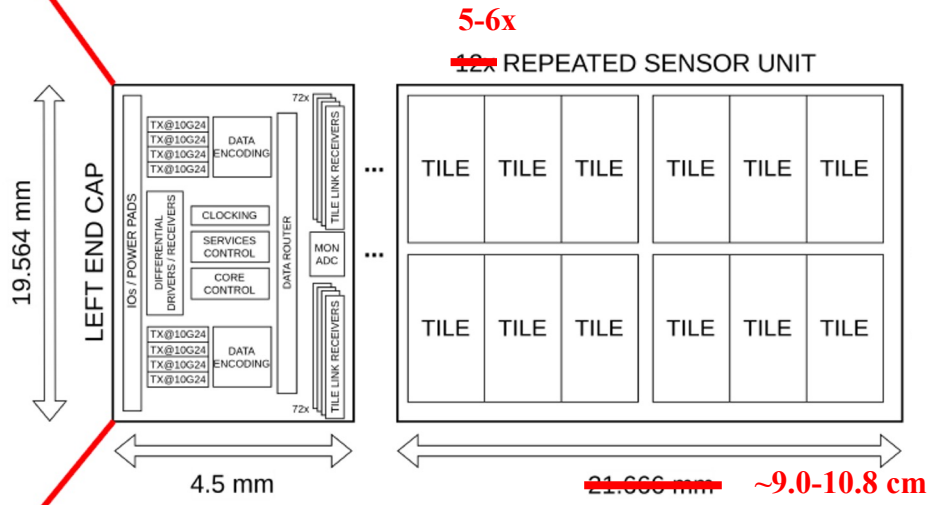
BERKELEY LAB

EIC-LAS



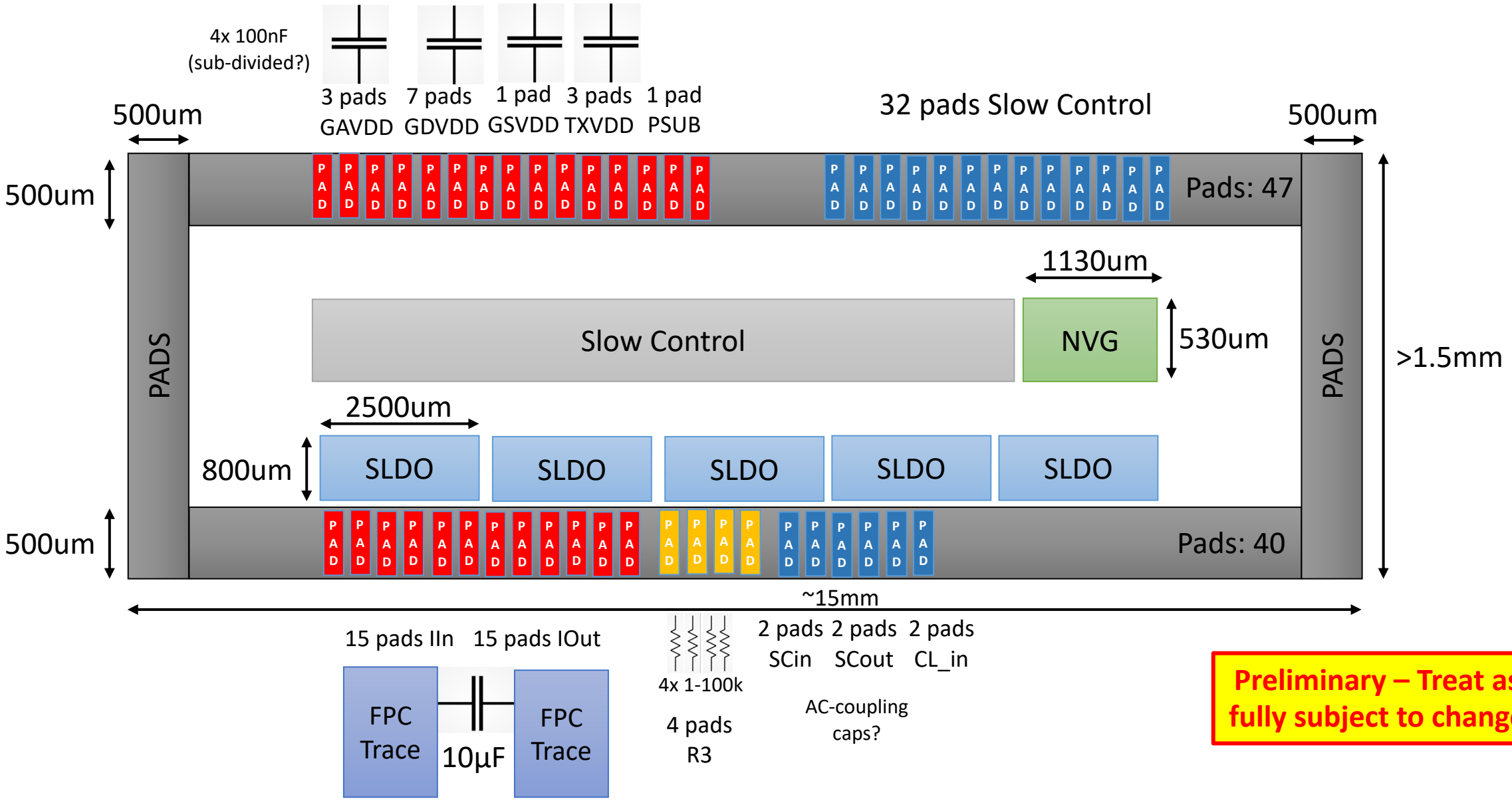
Supply	Typical (mA)	Max (mA)
PSUB (-1.2V)		
GSVDD/GSVSS (1.2V/0V)	40	60
GAVDD/GSVSS (1.2V/0V)	170	270
GDVDD/GDVSS (1.2V/0V)	526	816
TXVDD/TXSVSS (1.8V/0V)	200	300

Signal	Frequency
GCLK	160 MHz
SYNC	N/A
GRSTB	N/A
SRVWR/RD	5 Mbps
SCWR/RD	5 Mbps
HSDATA0	5.12/10.24 Gbps



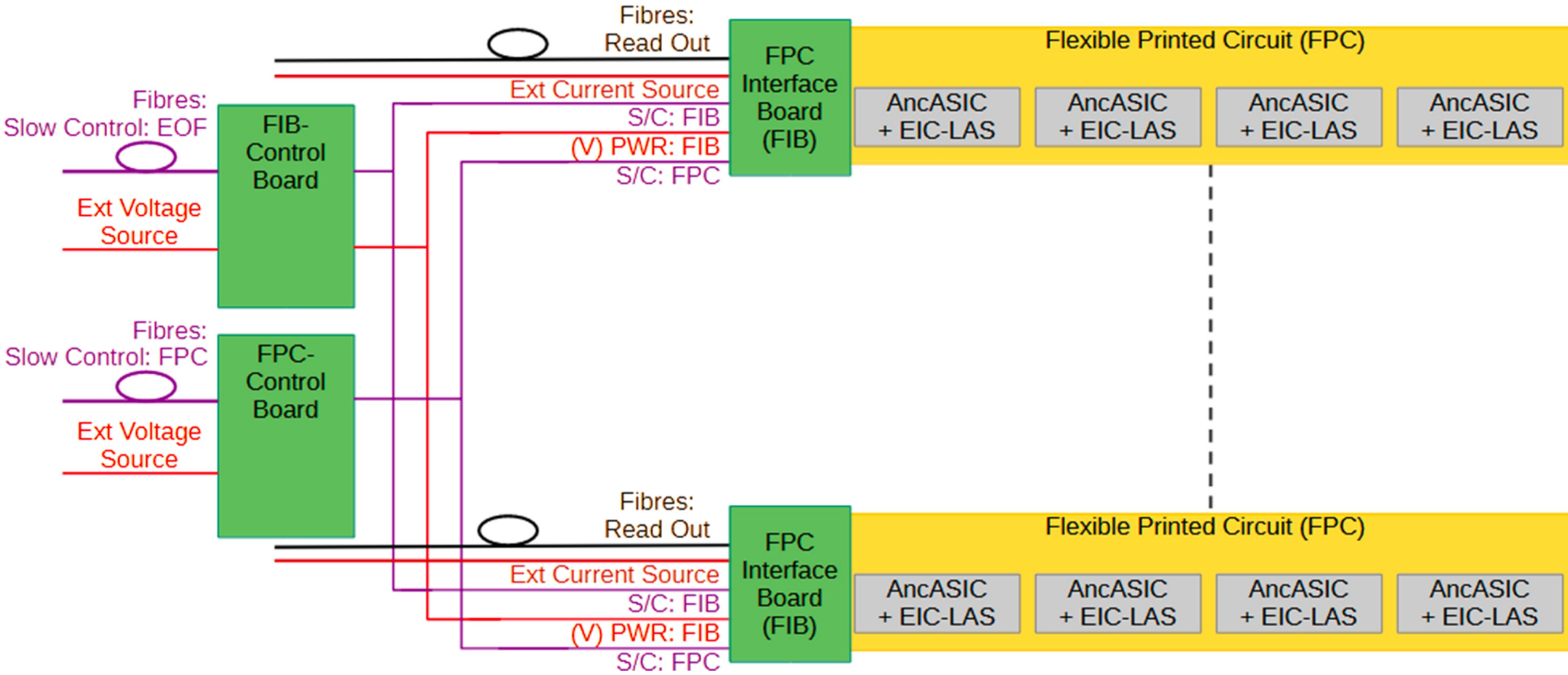

```
GSVDD/GSVSS  : Global Services domain (1.2V/0V), always-on, used for on-chip services
GAVDD/GAVSS  : Global Analog domain (1.2V/0V)
GDVDD/GDVSS  : Global Digital domain (1.2V/0V)
TXVDD/TXVSS  : Serializer domain (1.8V/0V), only used for serializers
PSUB         : Substrate bias (-1.2V .. 0V), used for substrate biasing
Control pads : Powered by the services domain
```

AncASIC

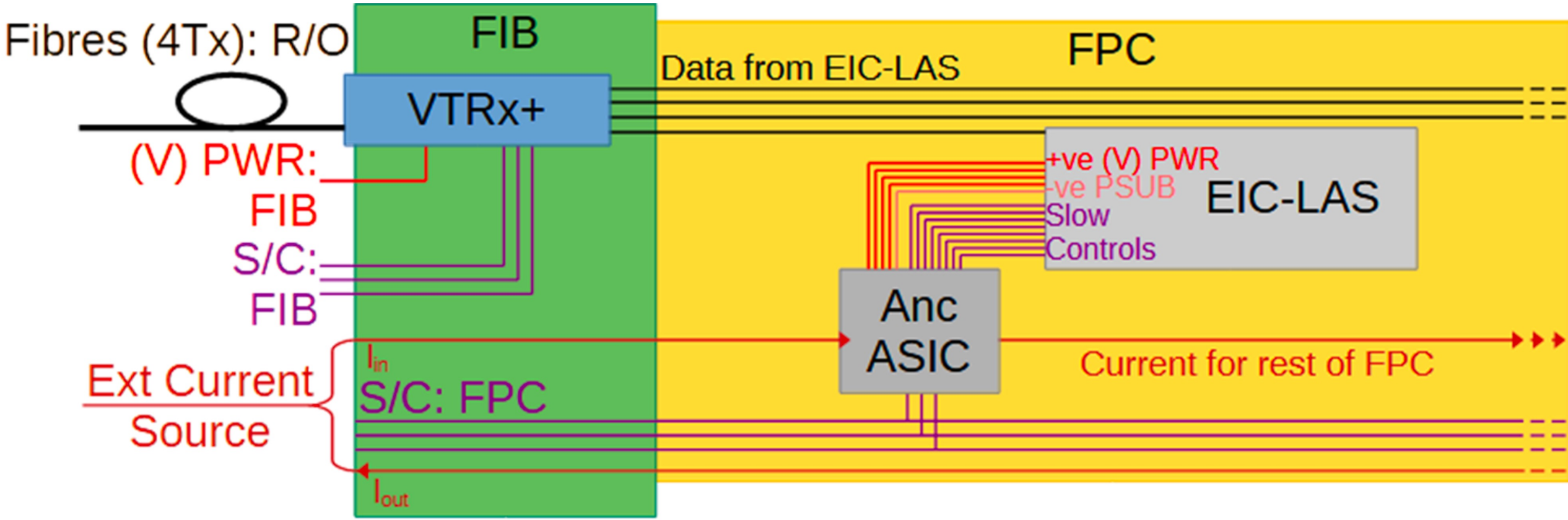


Preliminary – Treat as fully subject to change

SVT OB/Disk with EIC-LAS+AncASIC



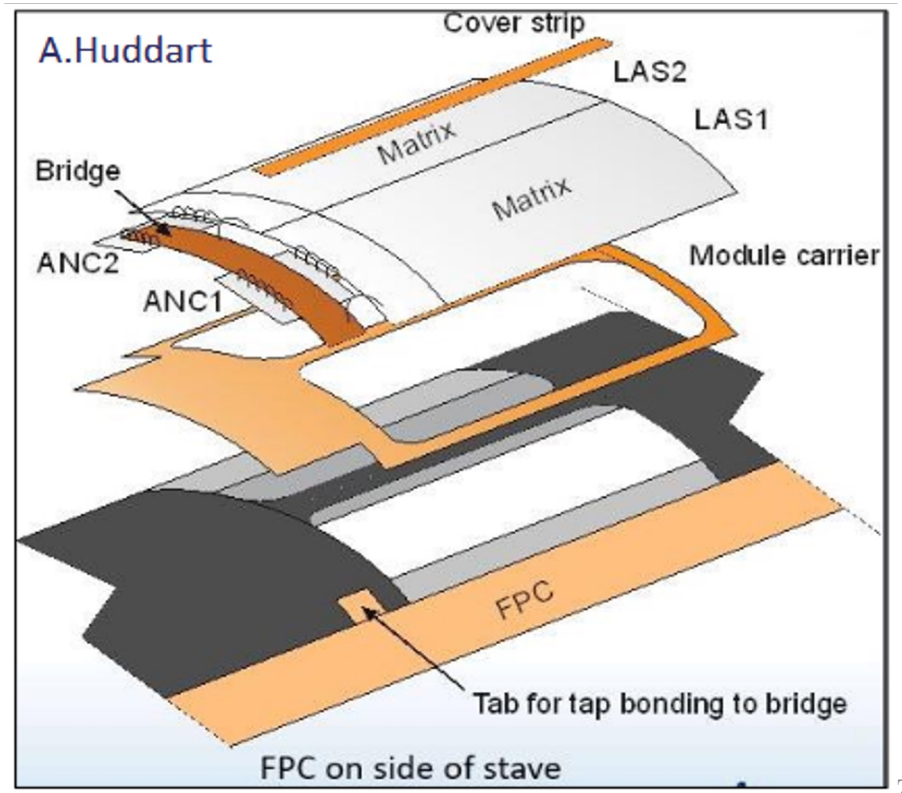
SVT OB/Disk with EIC-LAS+AncASIC

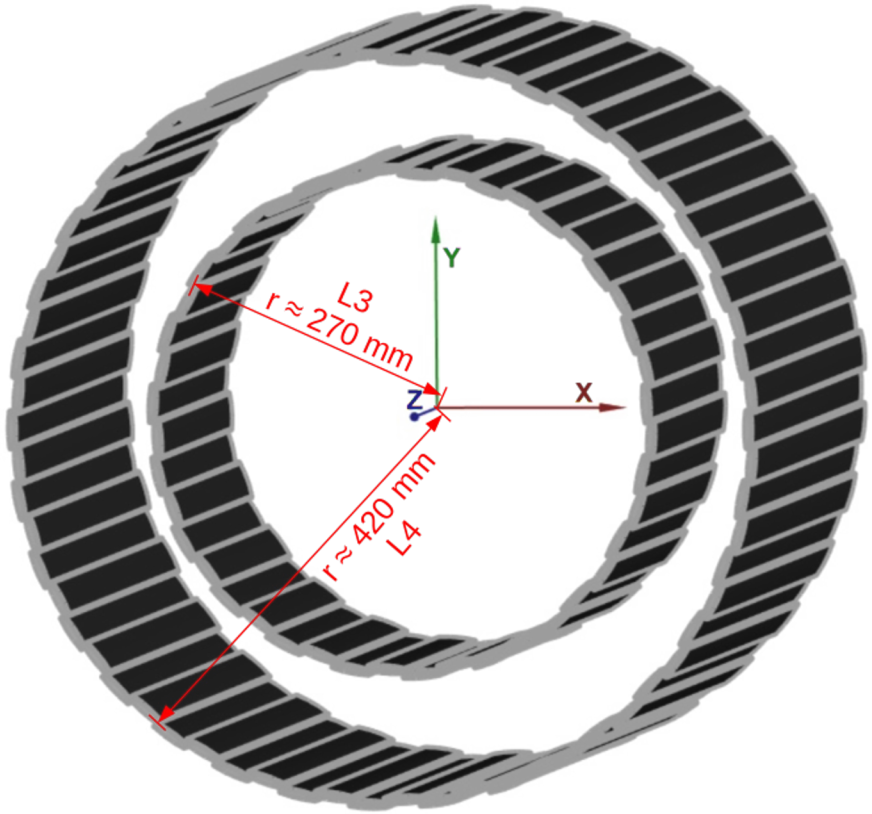


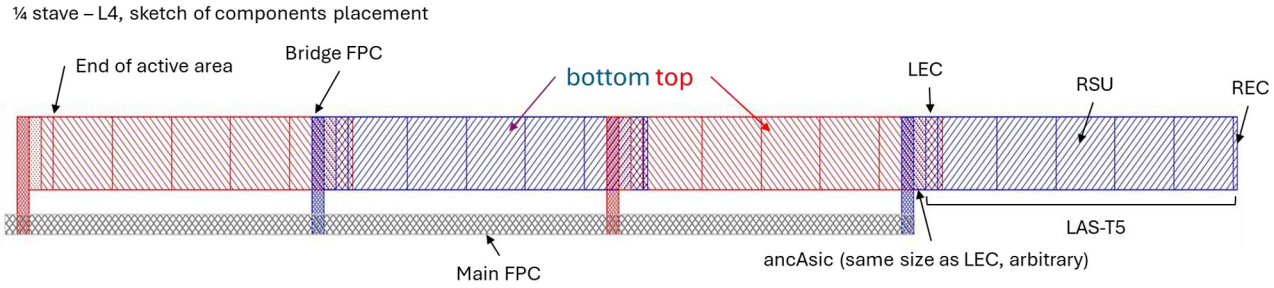
SVT Outer Barrel (L3/L4)

Outer barrels (L3, L4)

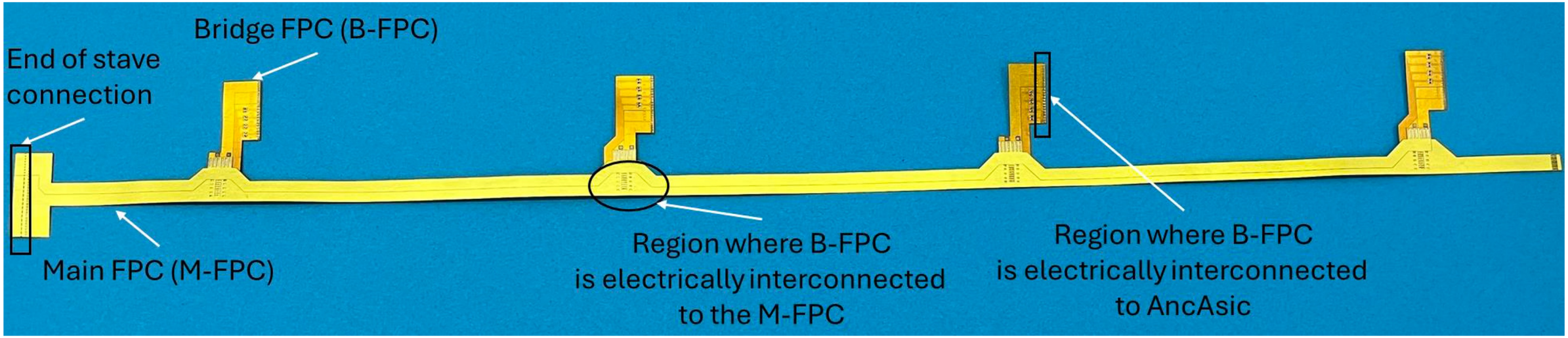
- **EIC large area sensors (EIC-LAS)** with design modified based on ITS3, mounted on more conventional staved structure with CF support and integrated air/water cooling
- **AncASIC** for sensor bias, serial power and slow control
- Radii of 27 and 42 cm; lengths of 42 and 84 cm
- X/X_0 ~0.25% and 0.55%

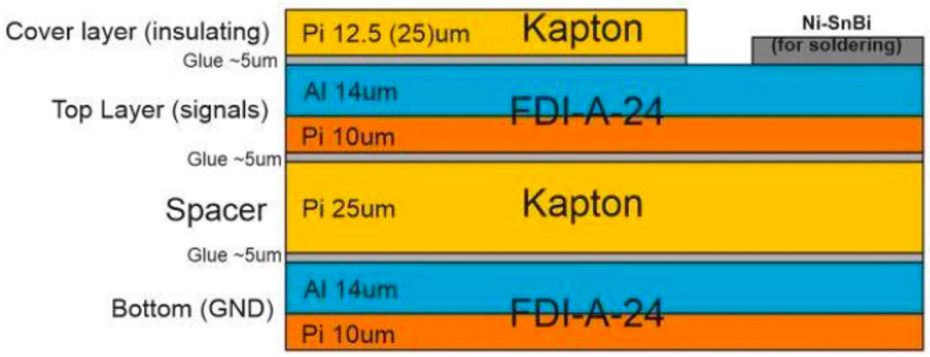






RPE LTU



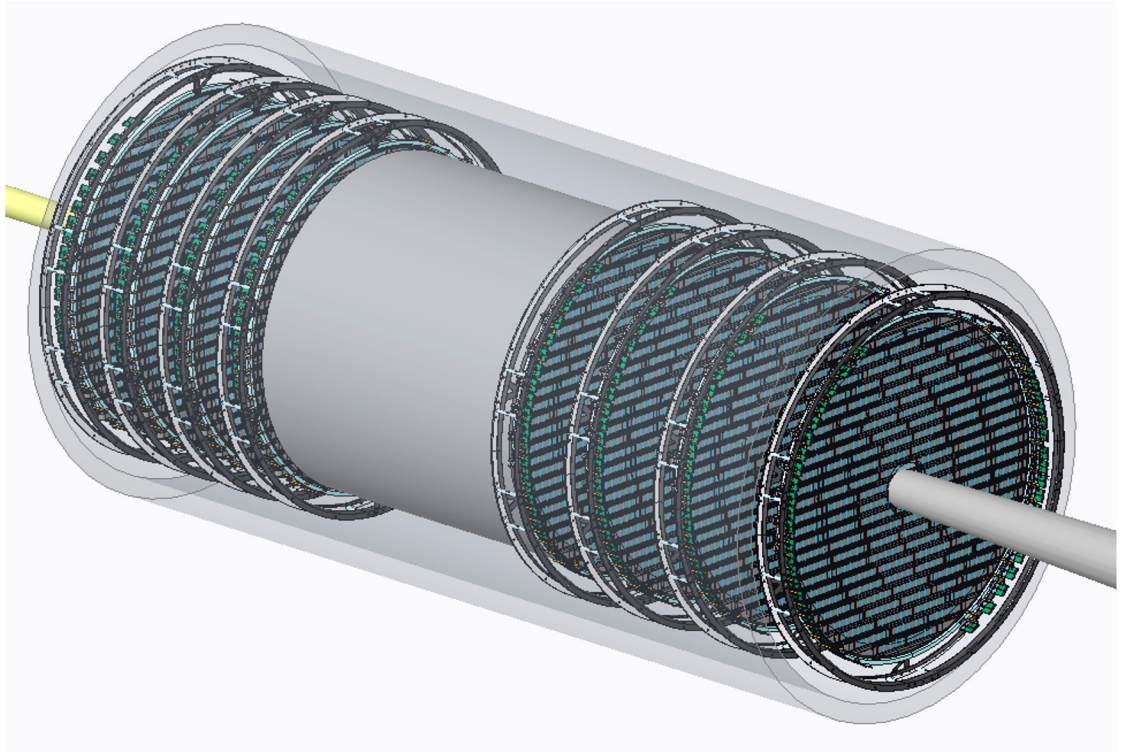


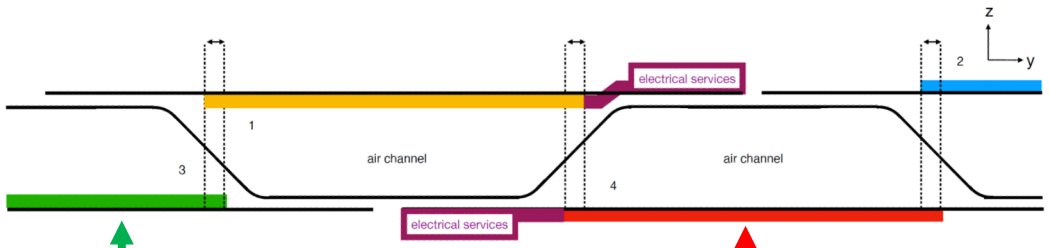
	Components	Thickness	Material	X0 (cm)	X0 (%)	Comment
HIC	FPC metal layers	28	Al	8.897	0.031	14um/layer x 2 layers = 28um (FDI-A-24)
	FPC insulating layers 1	20	polyimide	28.57	0.007	10um/layer x 2 layers = 20um (FDI-A-24)
	FPC insulating layers 2	25	polyimide	28.57	0.009	
	FPC binding glue	5	TBC	39.07	0.001	real glue unknown, assuming Araldite 2011
	Pixel Chip	50	Si	9.37	0.053	To change to 66um thickness, to read ITS3 TDR
Total (FPC + Pixel chip)					0.102	
Total FPC only					0.049	Note FPC material budget closer to Pixel chip (0.053%X))

SVT Disks (ED/HD0-4)

Disks (5 electron + 5 hadron going direction):

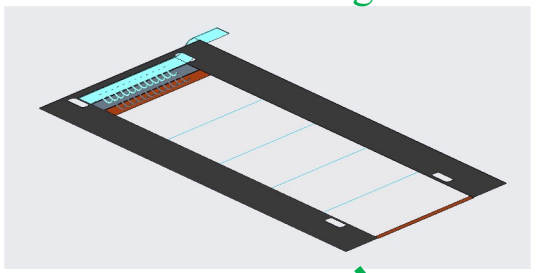
- **EIC large area sensors (EIC-LAS)** with design modified based on ITS3, mounted on conventional structure with CF support and integrated air cooling
- **AncASIC** for sensor bias, serial power and slow control
- Outer radii of 25 and 40 cm
- X/X_0 ~0.25%

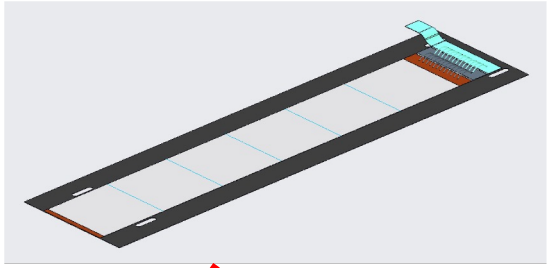


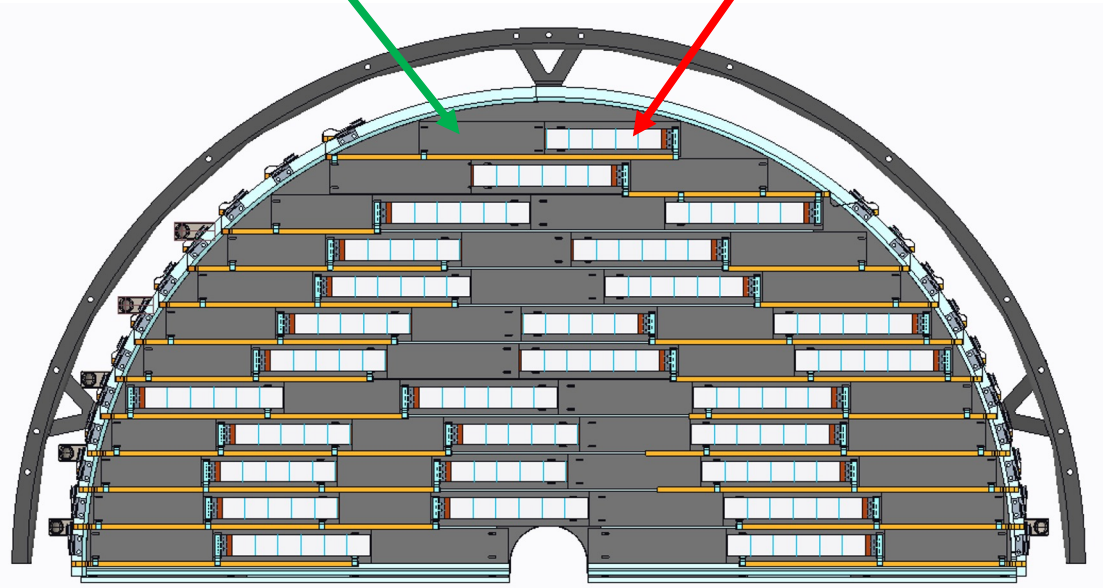


Sensor Inward Facing Module

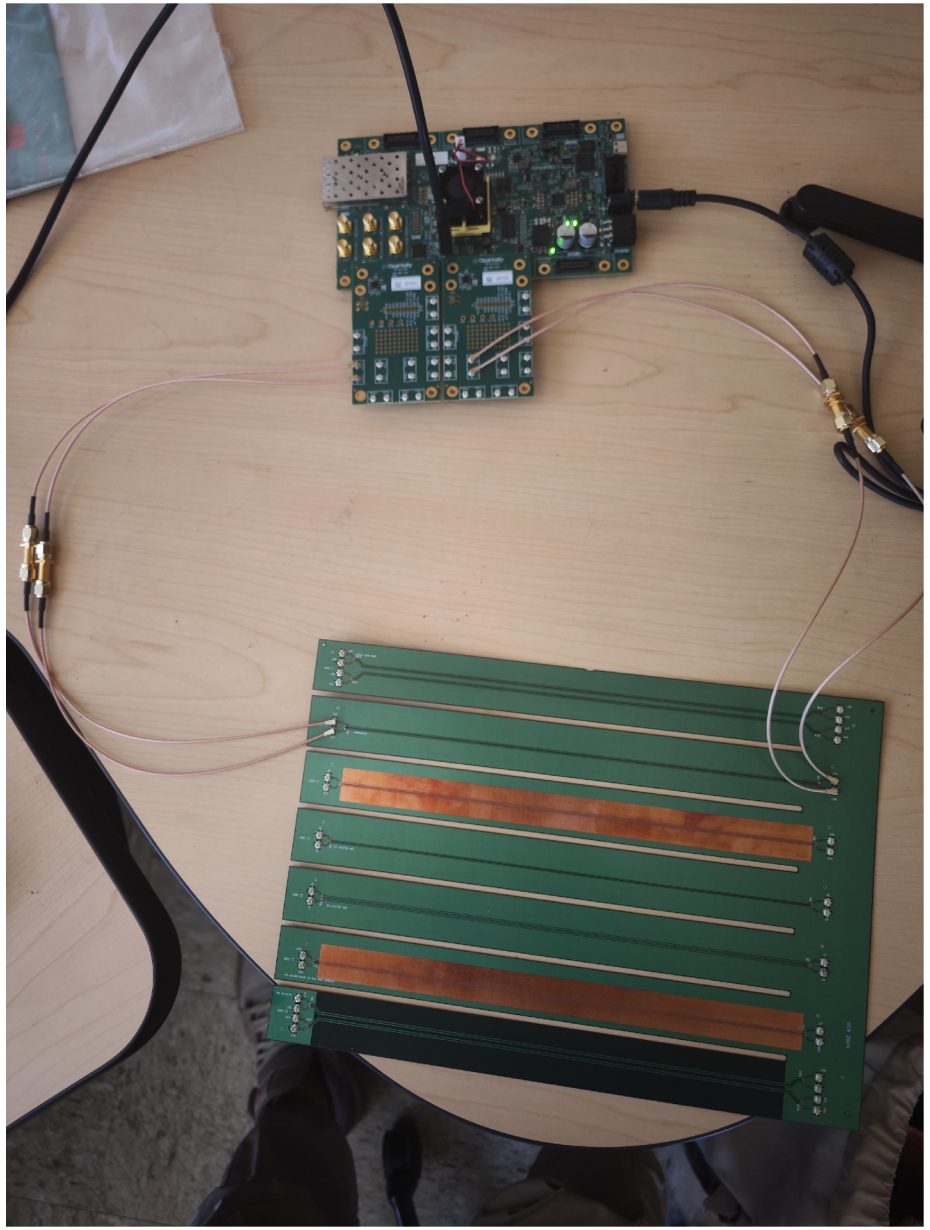
Sensor Outward Facing Module







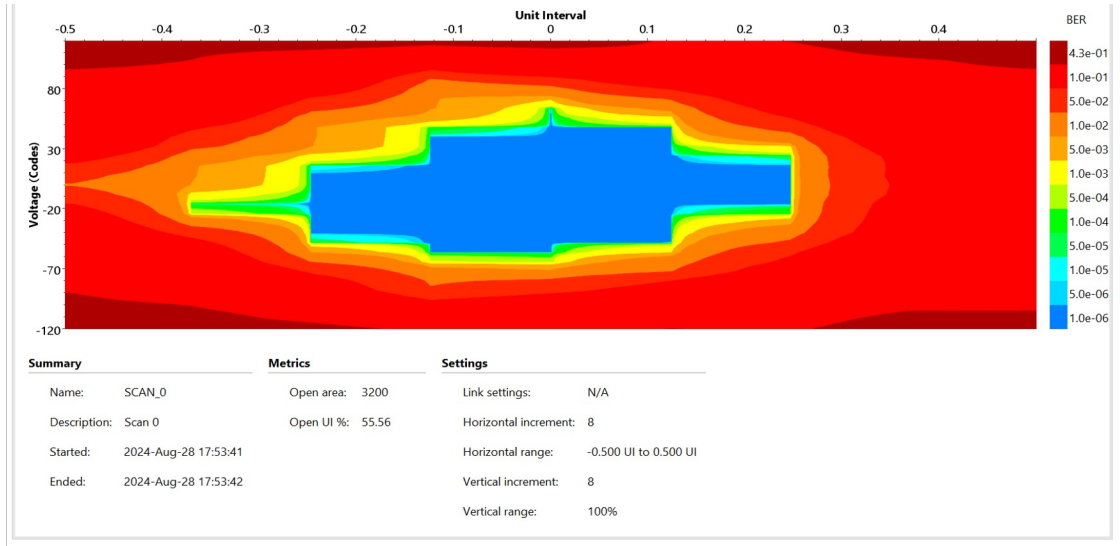
IBERT Test on OMNI

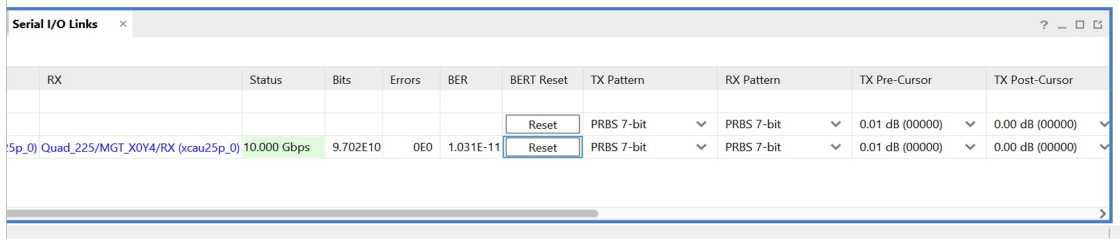


Based on XEM8320 FPGA evaluation boards with Artix Ultrascale+ AU25P FPGA;

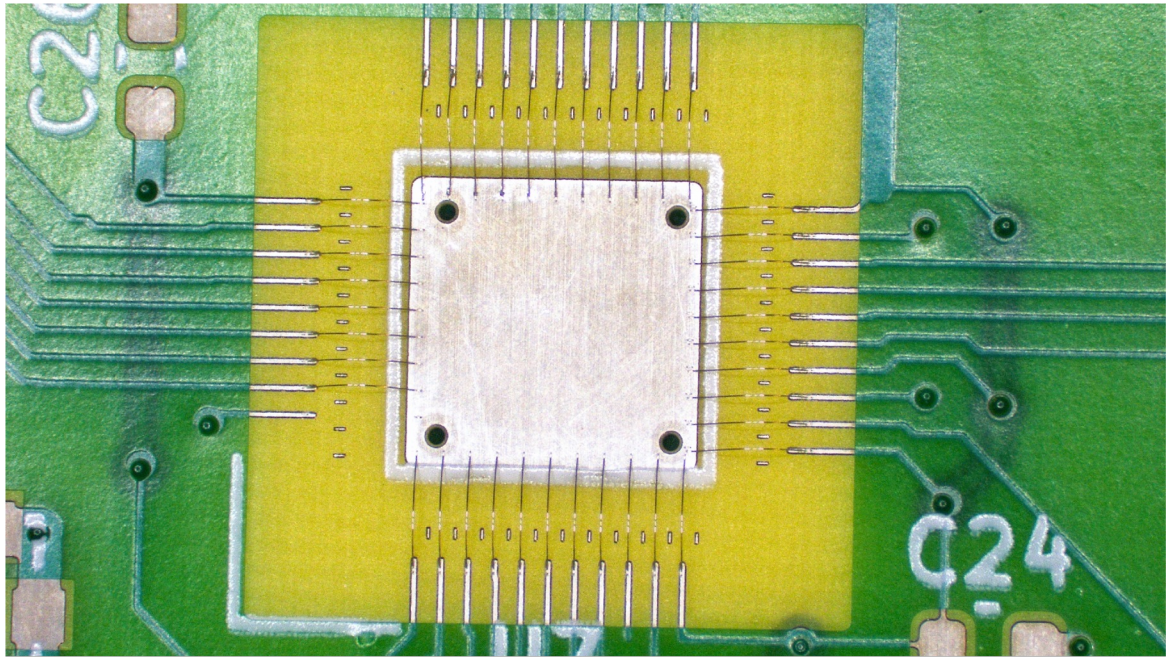
Scan eye plot for each differential lines @10Gbps:

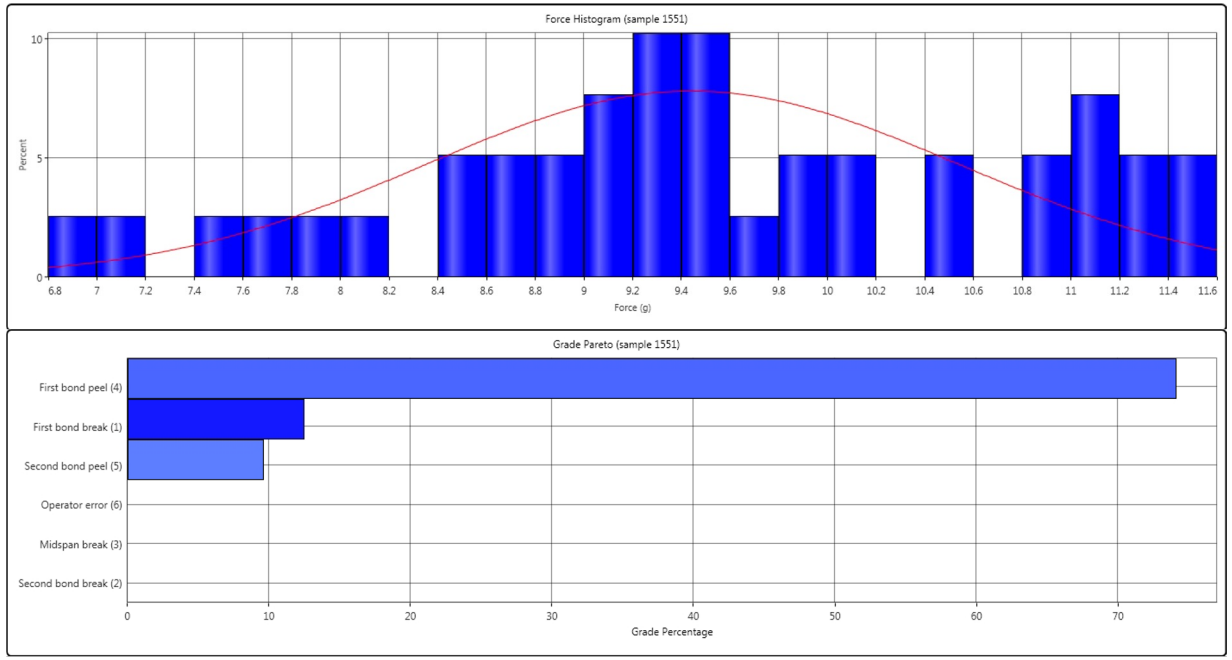
- Open area
- Bit error ratio





Wire-bonding and Pull Tests on OMNI





- Number of tests: 39
- Mean - 3 * standard deviation: 5.7782 g
- Minimum load: 6.9011 g
- Maximum load: 11.570 g
- Mean: 9.5195 g
- Standard Deviation: 1.2471 g

FPC Summary and Plan

- UK colleagues have been working with LTU to produce FPC prototypes for OB
  - LTU: provided main and bridge FPC (took ~9 months to design/produce). SMD soldering through flex-mounts (page 14)
  - UK: issue with spTAB under investigation; issue with wire-bonding on Al+polyimide foil, improved after bonder tuning; no signal test yet
  - Goal at LBL with LTU: check soldering to connect main and bridge FPCs; develop tooling and assembly procedure; validate power/signal integrity
- LBL has been working with OMNI to produce Al FPC prototypes (two iterations already)
  - First iteration:
    - good wire-bonding results
  - Second iteration:
    - Implemented Cu-plated soldering pads
    - Implemented through-vias to connect two Al layers
    - Improved signal transmission with Erlon528k, 12/14 mils traces over 25 cm: ~60%@4 GHz, passed IBERT@10Gbps
  - Third iteration to check:
    - Power (DC current) transmission
    - Signal transmission integrity and cross-talk with 6/6, 7/7, 8/8 mil traces and different grounding
    - Flexibility