



U.S. MAGNET
DEVELOPMENT
PROGRAM

Test Facility Improvements – LBNL

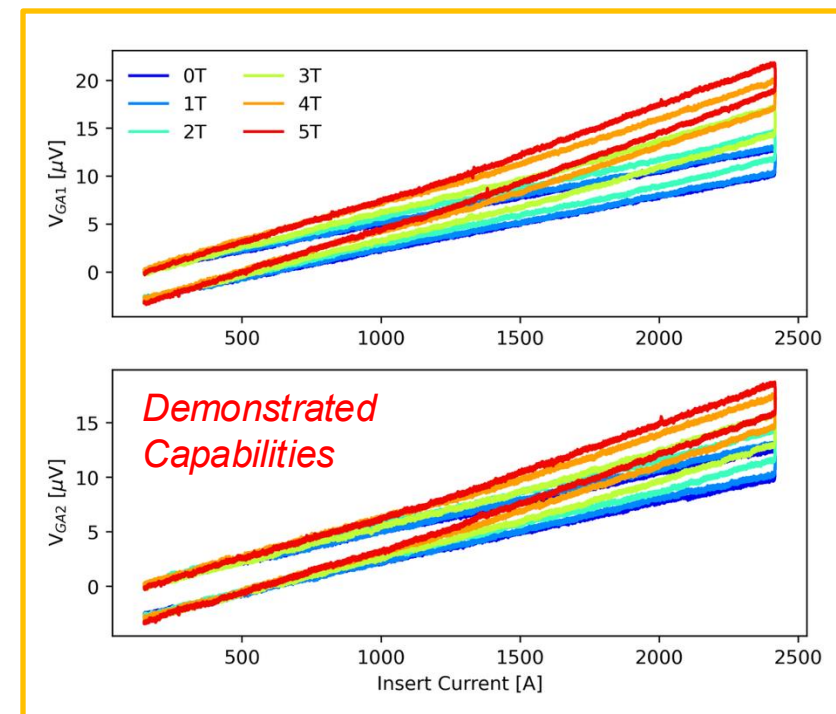
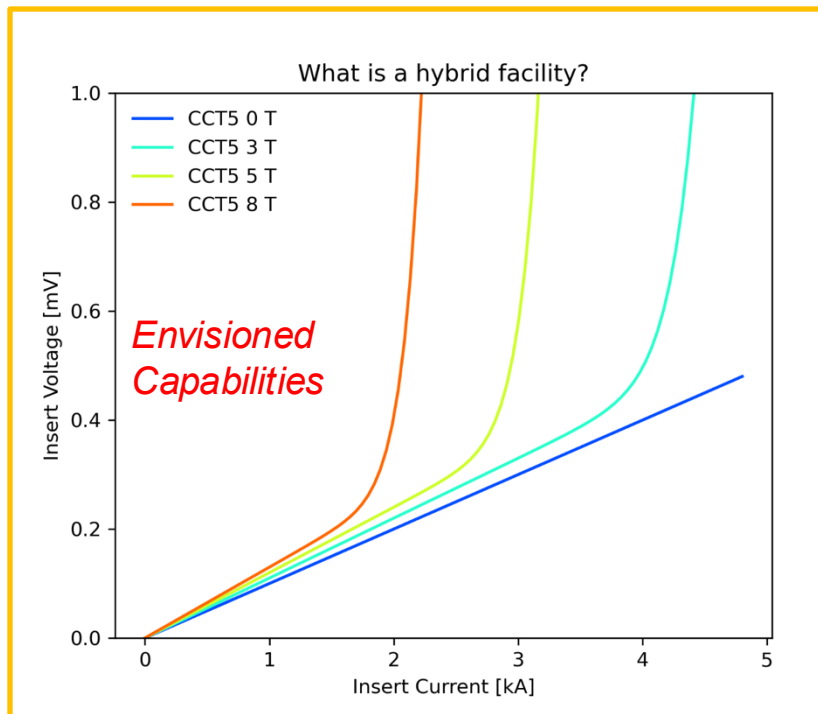
Reed Teyber, Diego Arbelaez, Chet Spencer, Anjana Saravanan, Philip Mallon and MTF-U Team

Introductory Remarks

- MDP collaboration meeting - gave overview of LBNL test facility
 - Due to budget, no real progress since then
- Today's slides serve to
 - Outline where we are today
 - Comments on first hybrid test
 - Comments on performance limiting issues
 - Key projects underway

Demonstrated Capabilities

- First LBNL dual powering test performed successfully up to 6 Tesla
 - From a facility point of view, this is an LTS-HTS hybrid test with a single turn insert dipole
 - Encouraging, clean insert data, very positive outcome despite challenges



Facility – Dual Powering Circuits

IGBT temp & flow
monitoring and
interlock



cRIO PS control,
quench detection,
DAQ

IGBT bus bars

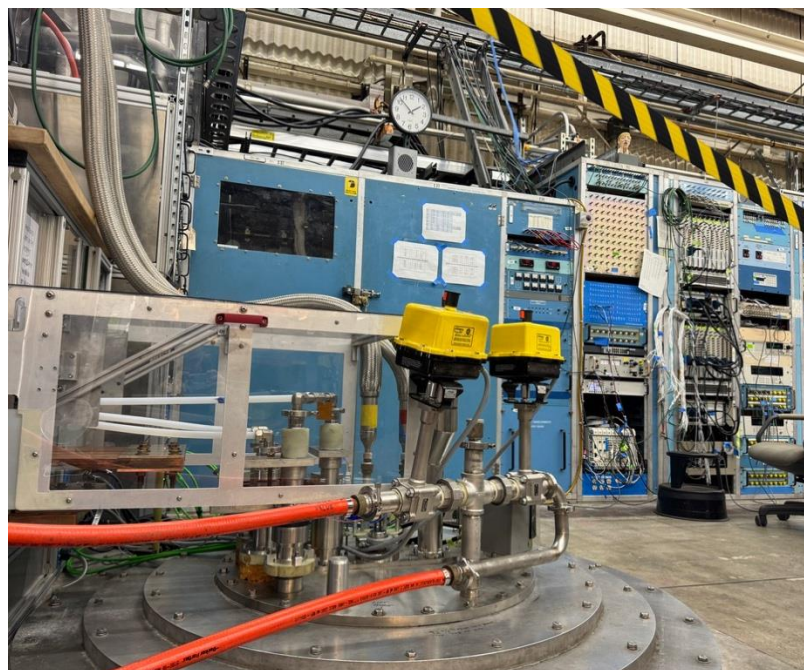
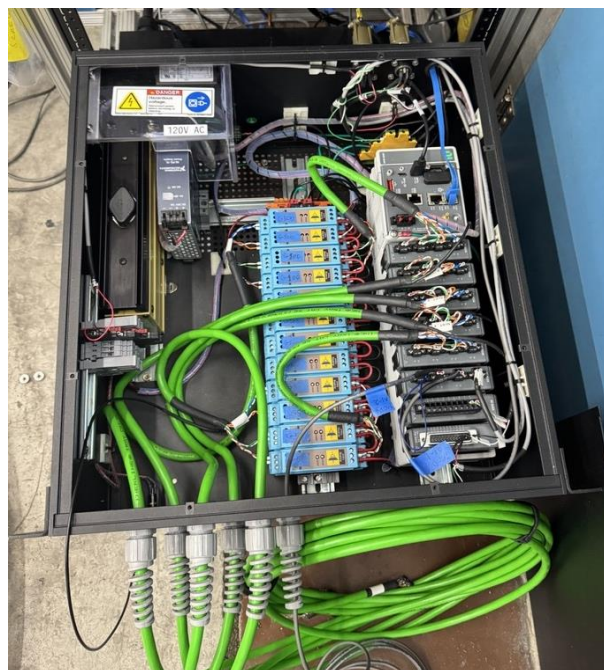


Facility, main
extraction rack /
DAQ

CCT5 + GA Joint

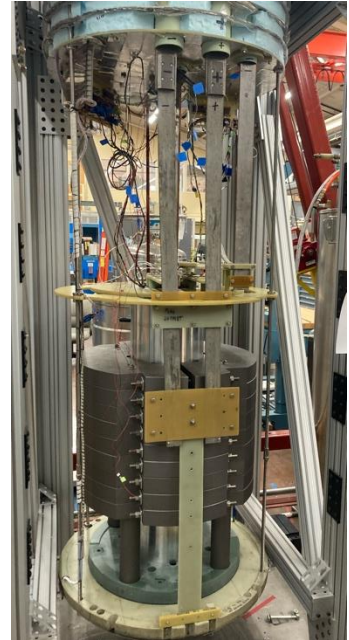


Header buildup,
Insert power circuit



HM1 Test Prep

- HM1 is now on header, hope to test within ~2 months of access to funding
 - Still some controls / software / wiring to dial in for test
- Facility will limit background field
 - The HM1 test experience – both the good and the inevitable bad – is the best feedback to adjust our engineering direction
- Next slides will touch on this



Bundle Name	Bundle Source	Name	Tap	Iso?	Module	Channel	Card	Measured Range (+/-)	Gain	Amp in range V	Amp out range V	DIP sw1	DIP sw2
Vtaps	Green + PCB Feed	Half +	VCI 10 Pos-00	Adam	Mod 1	AI 0	9238	0.05	10	0.5	5	10100001	*00100000
Vtaps	Green + PCB Feed	Half -	00-VCI 10 Neg	Adam	Mod 1	AI 1	9238	0.05	10	0.5	5	10100001	*00010000
Vtaps	Green + PCB Feed	full mag	10 Pos - VCI 10	Adam	Mod 1	AI 2	9238	0.05	10	0.5	5	10100001	*00010000
Vtaps	Green + PCB Feed	x	x	x	x	x	x	x	x	x	x	x	x
Vtaps	Green + PCB Feed	I0-I8		Adam	Mod 2	AI 0	9238	0.01	50	0.1	5	10100001	*00100000
Vtaps	Green + PCB Feed	I8-I15		Adam	Mod 2	AI 1	9238	0.01	50	0.1	5	10100001	*00100000
Vtaps	Green + PCB Feed	I15-I22		Adam	Mod 2	AI 2	9238	0.01	50	0.1	5	10100001	*00100000
Vtaps	Green + PCB Feed	I22-O2	splice	Adam	Mod 2	AI 3	9238	0.01	50	0.1	5	10100001	*00100000
Vtaps	Green + PCB Feed	O0-O4		Adam	Mod 3	AI 0	9238	0.01	50	0.1	5	10100001	*00100000
Vtaps	Green + PCB Feed	O4-O10		Adam	Mod 3	AI 1	9238	0.01	50	0.1	5	10100001	*00100000
Vtaps	Green + PCB Feed	O10-O13		Adam	Mod 3	AI 2	9238	0.01	50	0.1	5	10100001	*00100000
Vtaps	crow fly	B lakeshore		NO	Mod 3	AI 3	9238	NC	NC	NC	NC	NC	NC
Vtaps	crow fly	I Insert		NO	Mod 6	AI 0	9239	10	NC	NC	NC	NC	NC
Vtaps	crow fly	I Outsert		NO	Mod 6	AI 1	9239	10	NC	NC	NC	NC	NC
Vtaps	crow fly	CCT5 full scale full mag		Verivolt	Mod 6	AI 2	9239	500	0.02	500	10	Verivolt 500	Verivolt 500
Vtaps	crow fly	Insert full scale full mag		Verivolt	Mod 6	AI 3		500	0.02	500	10	Verivolt 500	Verivolt 500

PCB 1	C1	C2	C3	C4	DAQ + DAQ -
1	VCL10_PLUS	I0	O0	VCL13_PLUS_COLD	
2	O0	I8	O4	VCL13_NEG_COLD	
3	O0	I8	O4	X	
4	VCL10_NEG	I15	O10	X	
5	VCL10_PLUS	I15	O10	X	
6	VCL10_NEG	I22	O13	X	
7	X	I22	Lakeshore +Vh	VCL10_PLUS_COLD	
8	X	O0	Lakeshore -Vh	VCL10_NEG_COLD	
8	X	O0	Lakeshore +Vh	VCL10_NEG_COLD	
7	X	I22	Lakeshore +Vh	VCL10_PLUS_COLD	
6	VCL10_NEG	I22	O13	X	
5	VCL10_PLUS	I15 (Yellow-black stripe)	O10 (blue)	X	
4	VCL10_NEG	I15 (Yellow-black stripe)	O10 (blue)	X	
3	O0	I8 (green)	O4 (brown)	X	
2	O0	I8 (green)	O4 (brown)	VCL13_NEG_COLD	
1	VCL10_PLUS	I0	O0	VCL13_PLUS_COLD	

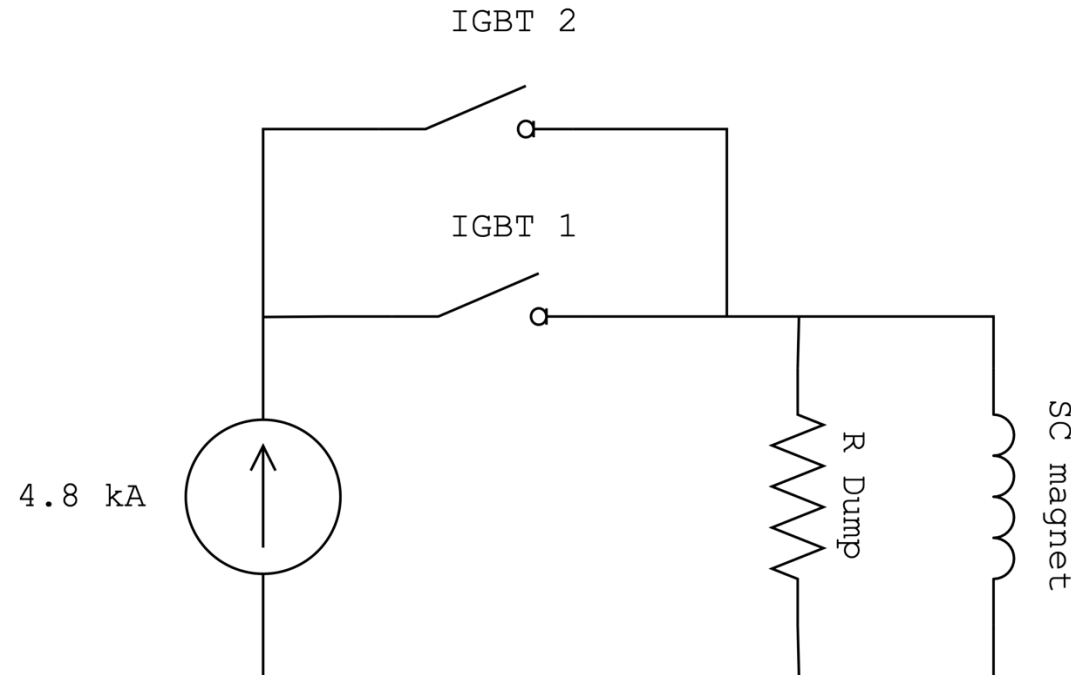
Reed Teyber, May 27 2025

PCB 2	C1	C2	C3	C4	
1	VCL13_PLUS	X	X	Lakeshore +100mA	
2	(crow fly to warm flag)	X	X	Lakeshore -100mA	
3	VCL13_NEG	X	X	X	
4	(crow fly to warm flag)	X	X	X	
5	VCL10_PLUS	X	X	X	
6	(crow fly to warm flag)	X	X	X	
7	VCL10_NEG	X	X	X	
8	(crow fly to warm flag)	X	X	X	
8	X	X	X	X	
7	VCL10_NEG_COLD	X	X	X	
6	X	X	X	X	
5	VCL10_PLUS_COLD	X	X	X	
4	X	X	X	X	
3	VCL13_NEG	X	X	X	
2	X	X	X	Lakeshore -100mA	
1	VCL13_PLUS_COLD	X	X	Lakeshore +100mA	

Reed Teyber, May 27 2025

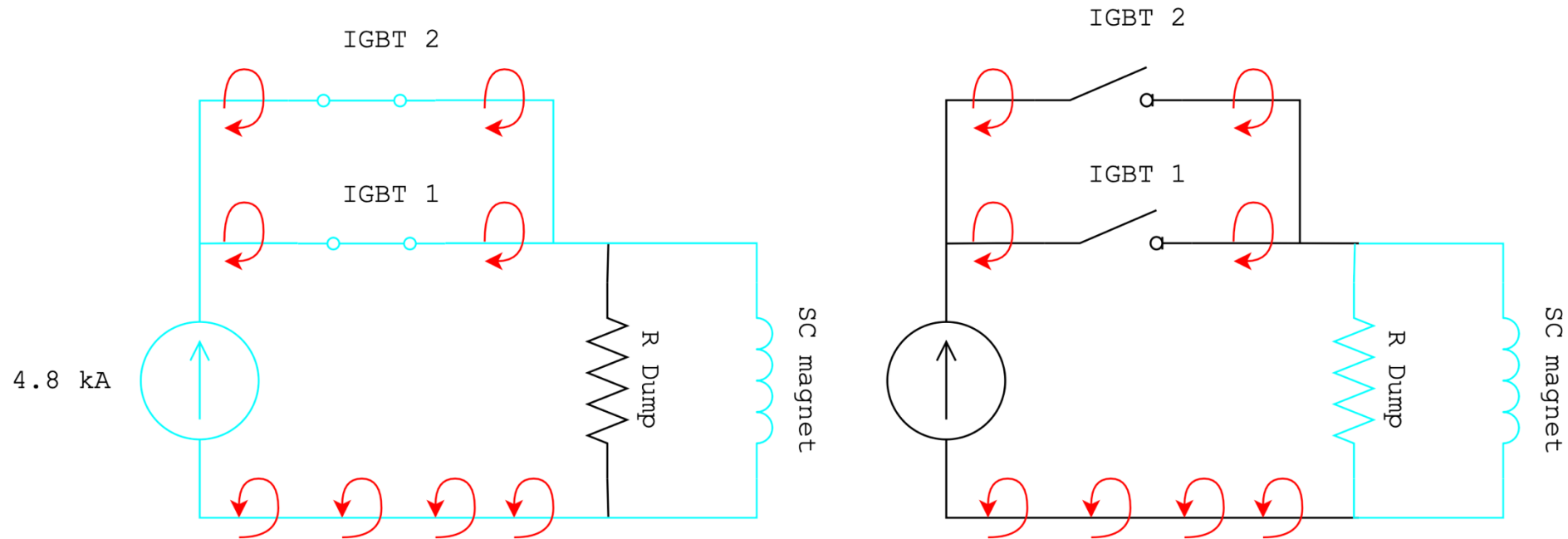
IGBT related issues

- Have had some unresolved issues with IGBT's
 - Consider overly-simplified schematic of Sorensen circuit



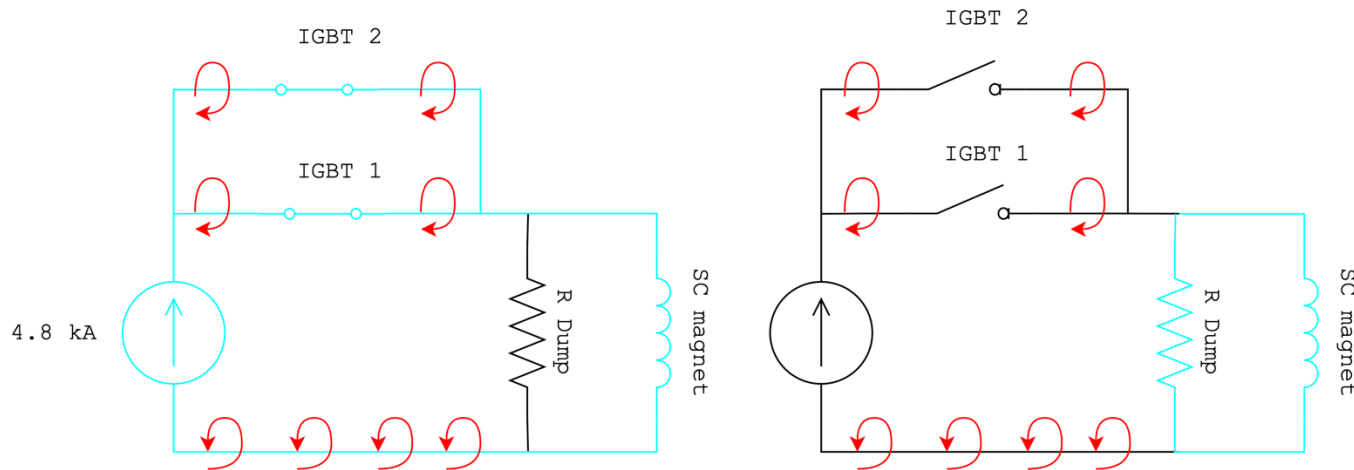
IGBT issue #1

- Fast IGBT switching causes bus bar magnetic field to collapse – voltage spike



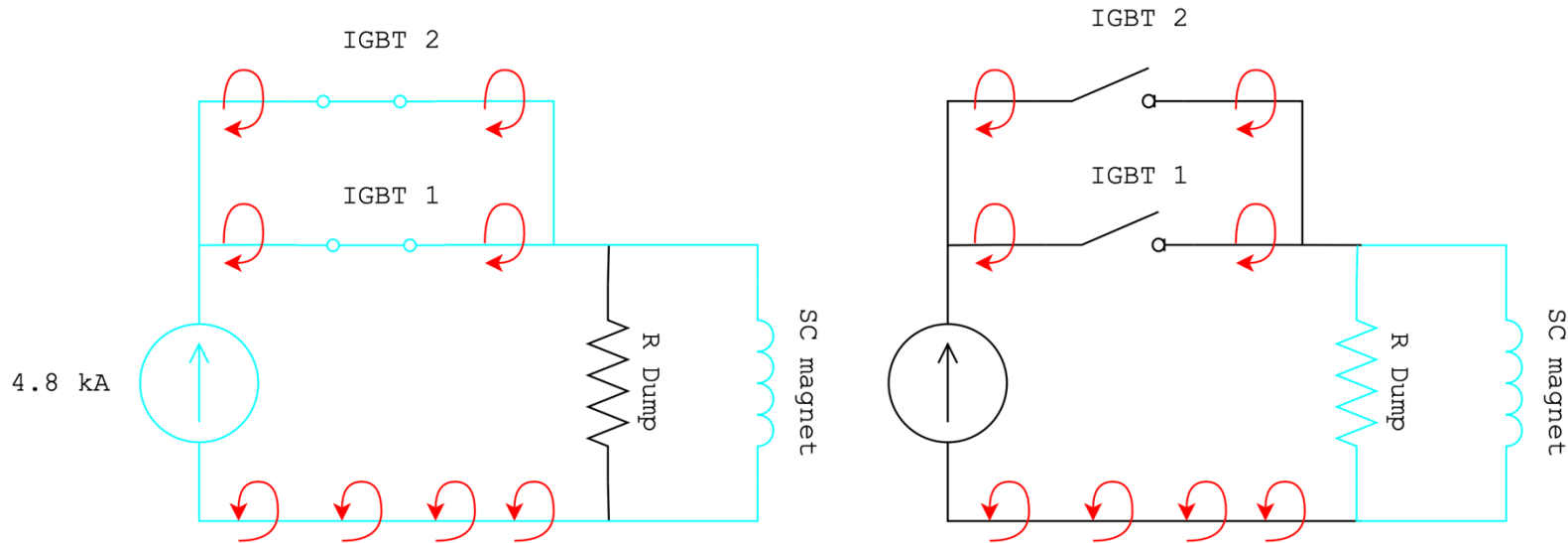
IGBT issue #1

- We have implemented 2 iterations of snubbers -RC high pass filters – but still have significant (short) voltage spike
 - Our comfort levels limit outsert field (should it?)
- Multiple paths forwards identified, should be solvable with sustained engineering effort
 - Most promising approach (capacitor bank) might mean un-winding significant administrative safety effort (WPC)



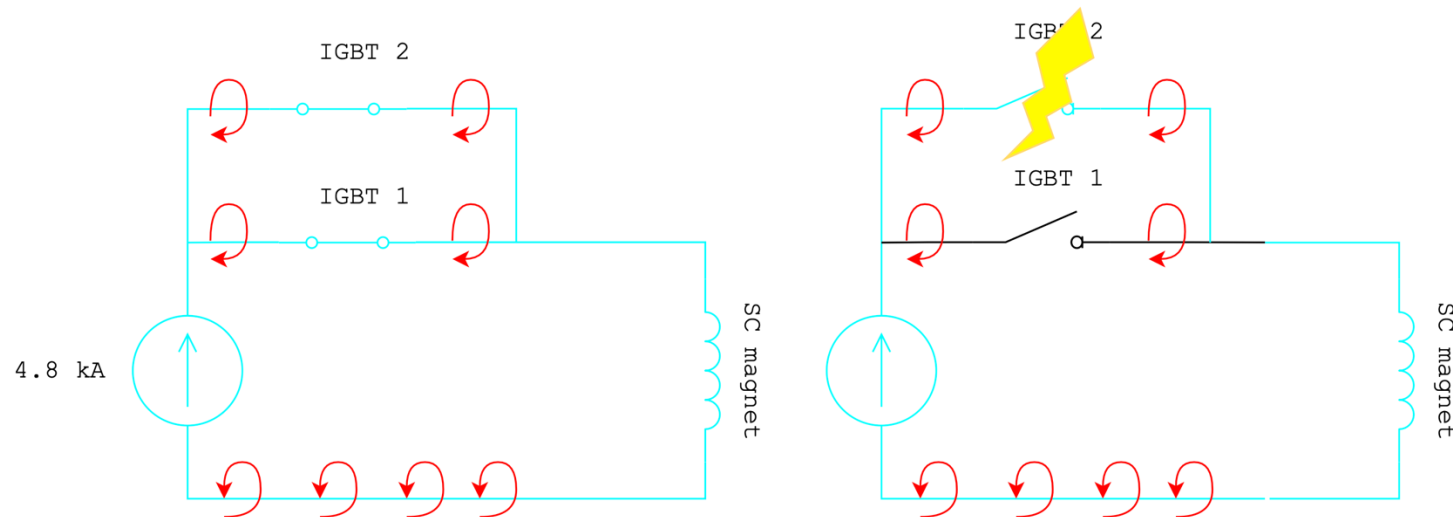
IGBT issue #2

- Insert cRIO control loses communication when outsert extracts
 - More testing required to determine if related to dB/dt during extraction or disturbance of the ground potential
 - Technically this does not limit our ability to characterize inserts, but highly undesirable



IGBT issue #3

- Someone dump resistor removed (visually intact), which was not removed after their testing
- Next test – destroyed IGBT pair (from 10 -> 8 functioning IGBT's), which reduced current below what CCT5W required



Future projects to highlight

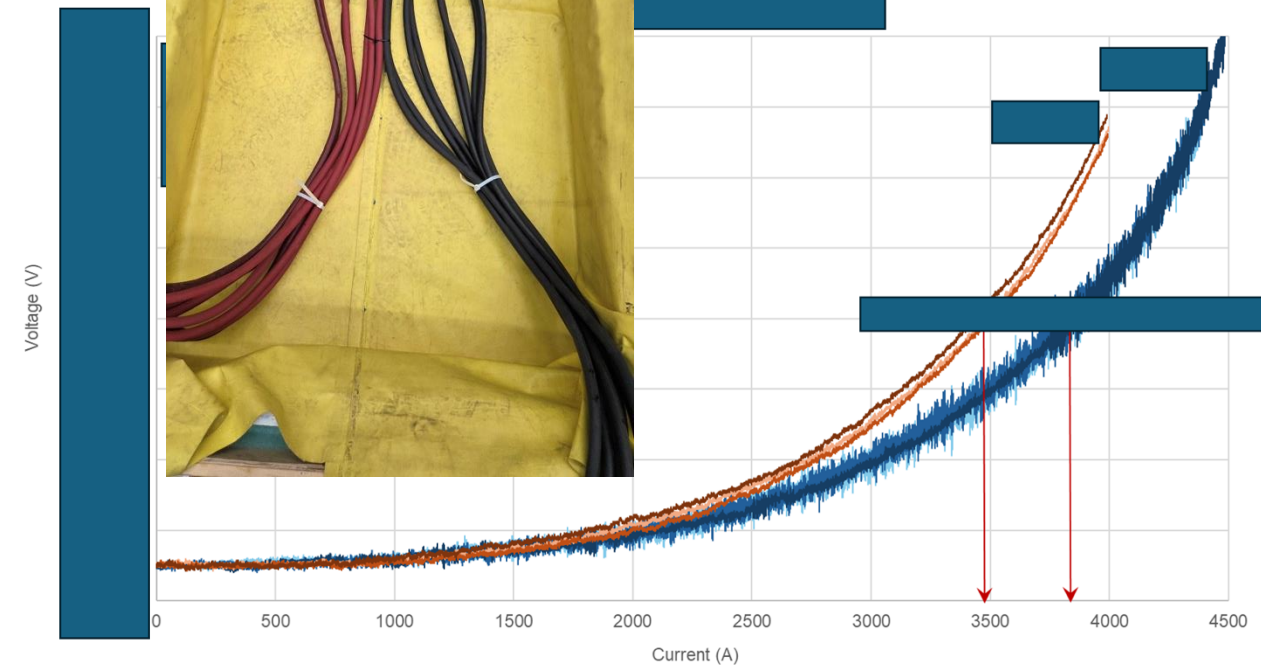
- Following slides highlight priorities after HM1 test is complete
 - Continued cRIO control / quench detection system improvements
 - New 36" hybrid header with 20 kA vapor cooled leads
 - Replacement & engineering improvements of 10 IGBT's
 - Expansion of insert power supply system towards 8 kA
 - New liquefier
- Many more discussed projects (new LTS data acquisition et cetera) but should tackle current challenges before taking on more

Control Improvements

- A significant effort has gone into the insert cRIO FPGA data acquisition + power supply control + HTS quench detection system
- Continued improvements + development + using the system are valuable to hybrid testing effort
- Recently used system for ReBCO fusion cable testing up to 4.5 kA



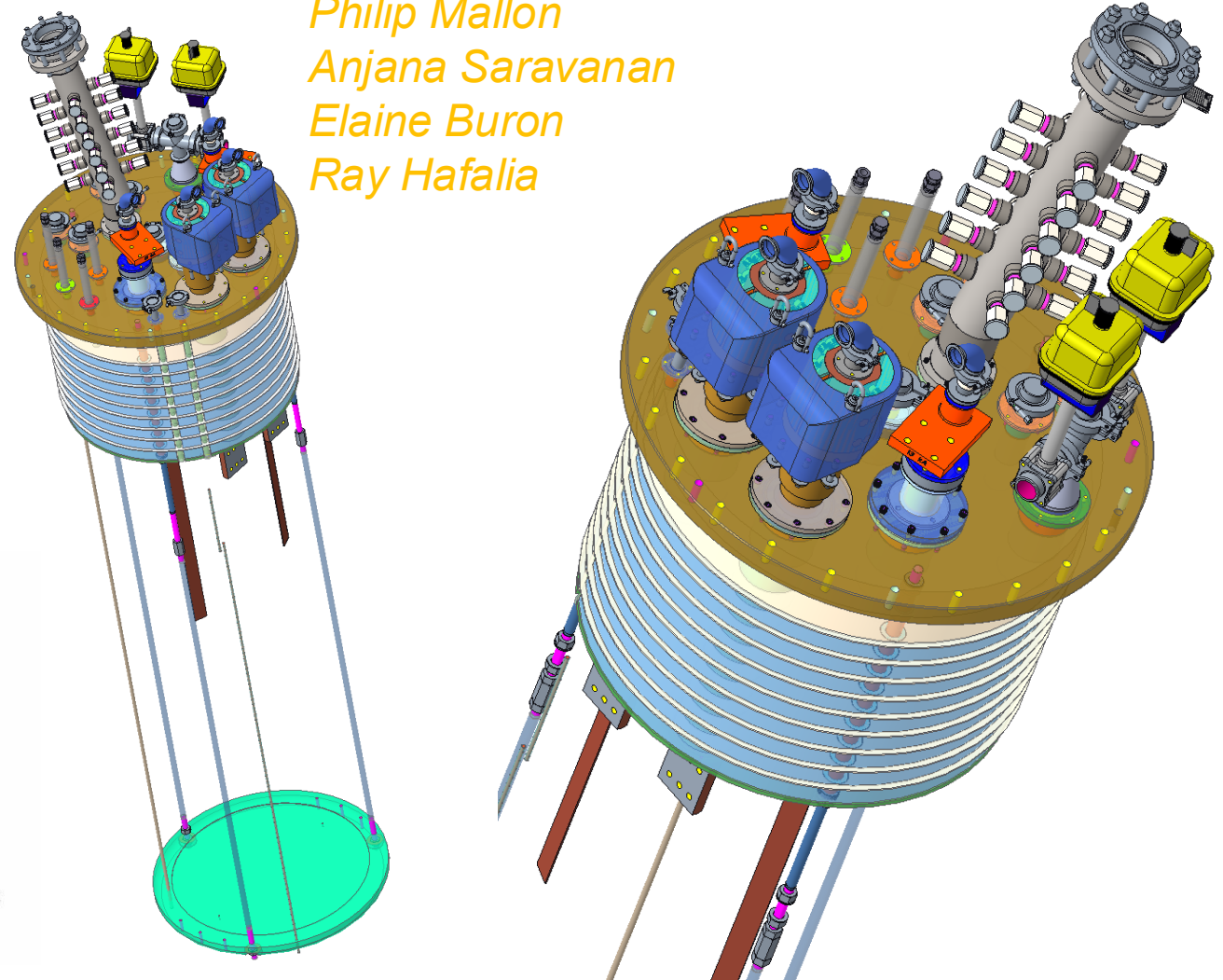
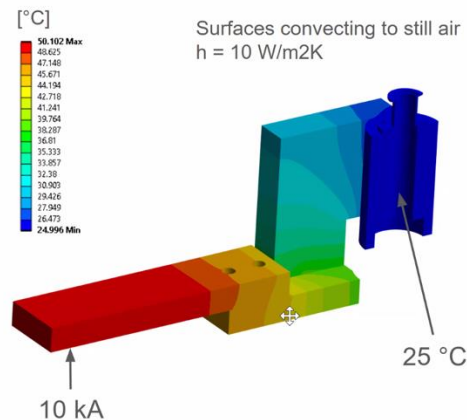
*Facility used for
project by:
Mike Naus
Xiaorong Wang*



36" Header

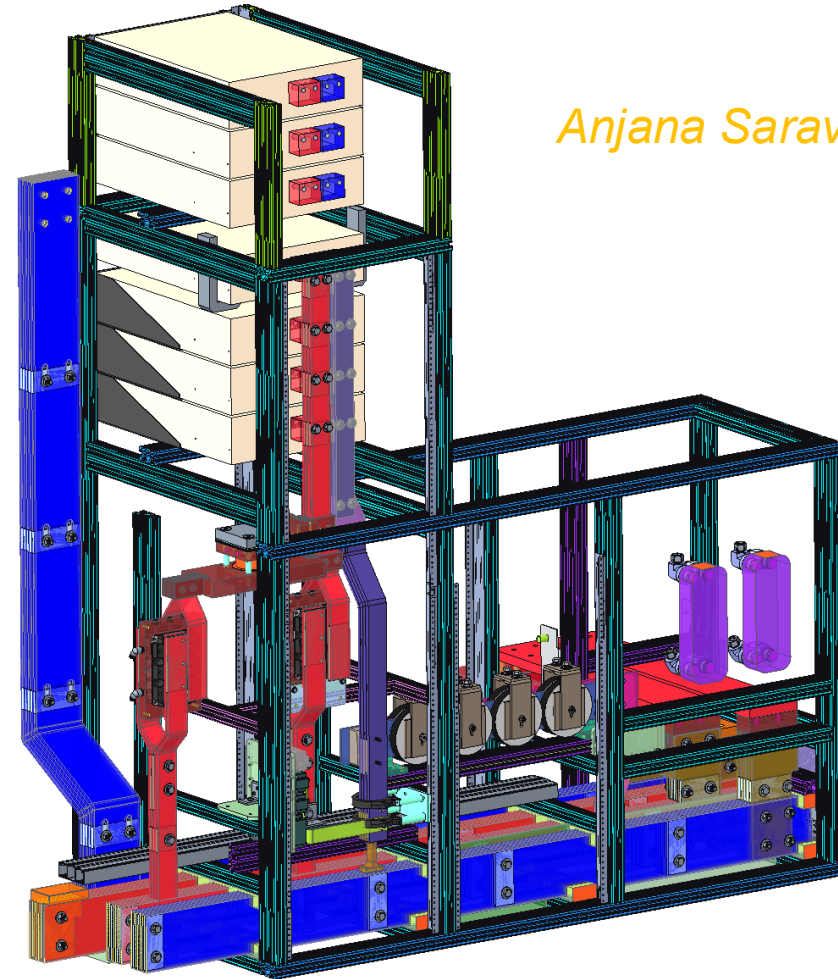
- We “repurposed” ports on our existing 32” header to allow 10 kA + 13.5 kA VCL’s
- New 36” header needed for our new 20 kA VCL’s and CCT6

*Philip Mallon
Anjana Saravanan
Elaine Buron
Ray Hafalia*



Sorensen Expansion

- We have additional power supplies, IGBT's and wall power to increase insert current (towards 8 kA)



Anjana Saravanan

New Liquefier

- We will have a new liquefier

Power Supply Summary

- Main PS

- limited ~ 14 kA
 - VCL's 13.5 kA
 - 8 IGBT's 14 kA
 - Voltage spike (TBD)
- Planned ~ 20 kA
 - VCL's 20 kA
 - 10 upgraded IGBT's 20 kA
 - Improved snubber

- Insert PS

- limited ~ 4.8 kA
 - 4 parallel PSU's
 - VCL's 10 kA
 - 2 upgraded IGBT's 4.8 kA
- Planned ~ 8 kA
 - 7 parallel PSU's
 - VCL's 10 kA
 - 4 upgraded IGBT's kA
 - Series diode-limited

Summary

- Funding has paused progress for many months
- Will test HM1 as quickly as possible, delaying any “invasive” facility projects
- After HM1, prioritize getting to high outsert and high insert current
 - New IGBT’s to replace destroyed units
 - Engineering effort to mitigate switching voltage
 - New header to accommodate 20 kA VCL’s (and CCT 6)
 - Expanded Sorensen power supplies for higher insert current
 - Continued development and integration of facility systems
- On a good trajectory, progress rate depending on available help