AncASIC MPW1 Test at LBL

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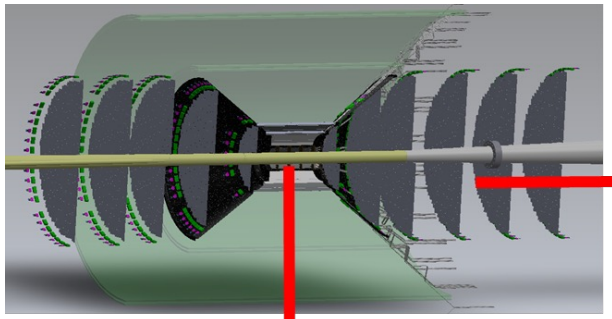
Introduction

ITS3 to ePIC

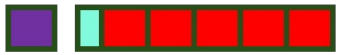
- ALICE are currently developing a chip (MOSAIX) to be used in the ITS3 upgrade.
- Since performance is similar, ePIC (the EIC detector) would like to use this chip for its inner layers.
- For the outer layers a smaller version is needed (yield and coverage)

AncASIC

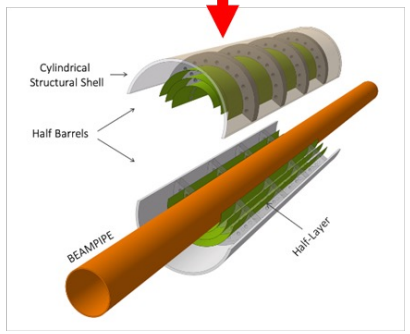
- Since MOSAIX was designed for inner layers, it has features which make it unsuitable for the outer layers:
  - Point-to-point powering
  - Point-to-point slow control
- Idea is to design an Ancillary ASIC (AncASIC) to interface to MOSAIX
  - Serial powering
  - Slow control multiplexing
  - Negative Voltage Generation



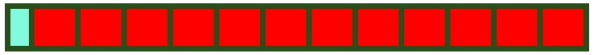
Outer Barrel and Discs



- Smaller Verion of MOSAIX with minimal changes (EIC-LAS)
- Supporting AncASIC

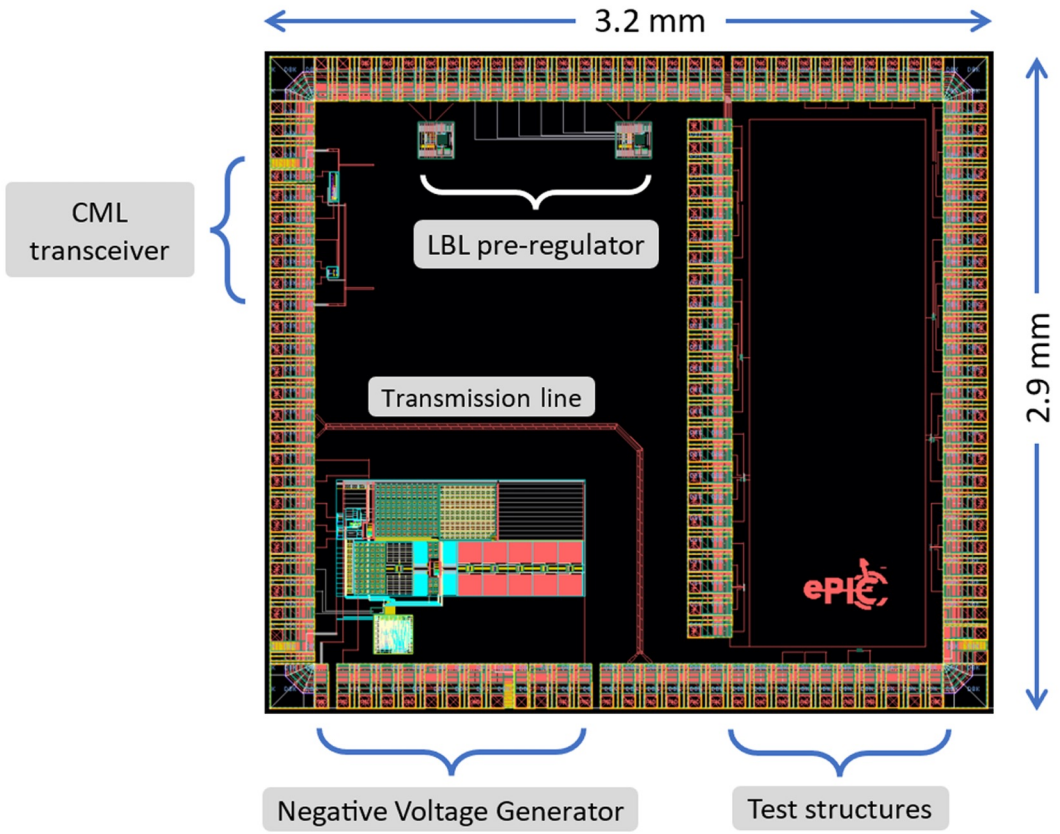


Inner Barrel



- Thinned silicon bent around beampipe
- USE MOSAIX from ITS3

AncASIC MPW1



The AncASIC MPW ASIC includes the following components:

- An I2C controller (programming interface for configuring individual configuration registers)
- Negative voltage bias generator (NVBG)
- Current-mode logic (CML) transmitter and receiver
- A passthrough, differential transmission line
- Test devices (MOSFET, BJT, resistor, etc.)
- Pre-regulator designed by LBNL ASIC group

MWP1 Carrier Board

VREF

Pre_REG

SC_CLK

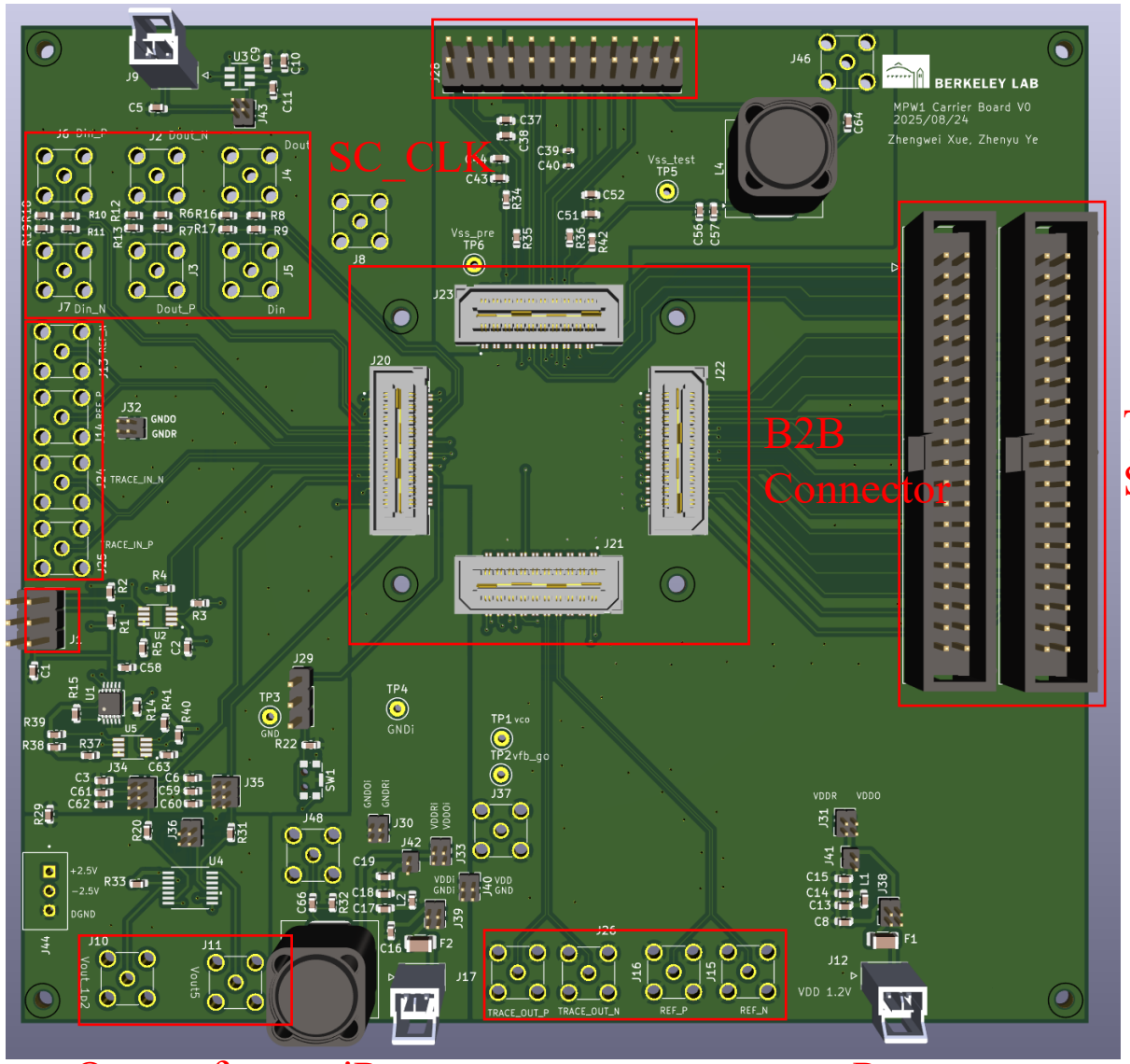
CML transceiver

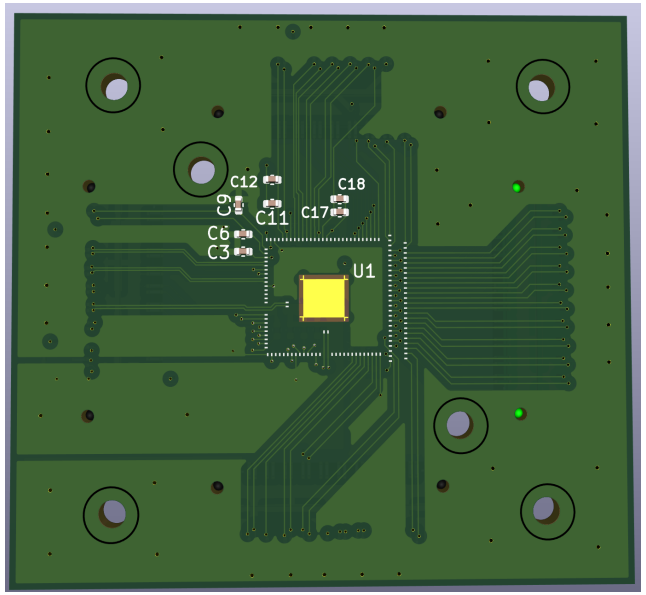
Input for passthrough trace and reference

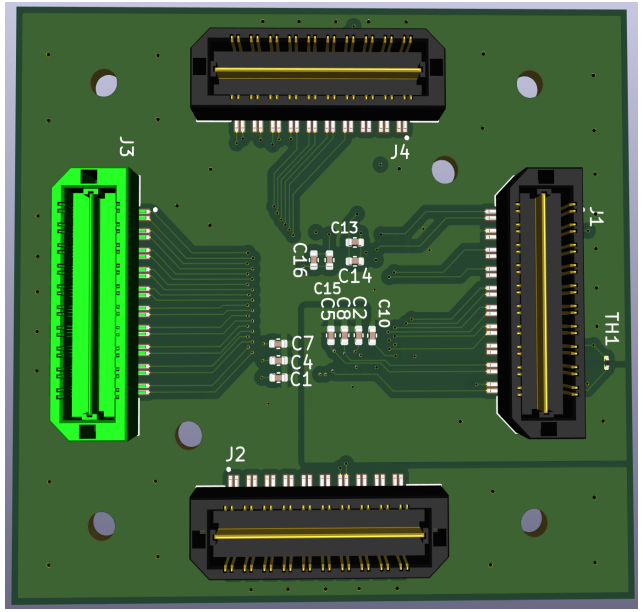
I2C

B2B Connector

Test Structure







Output for NBVG

iPower

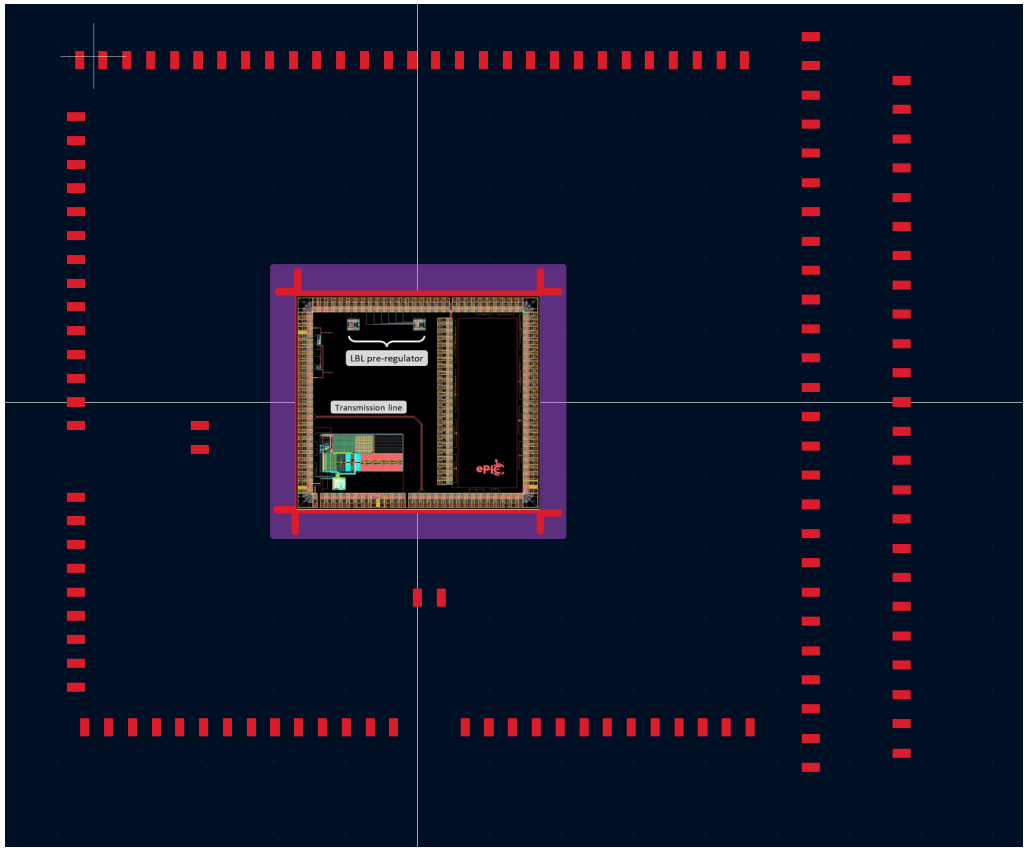
Output for passthrough trace and reference

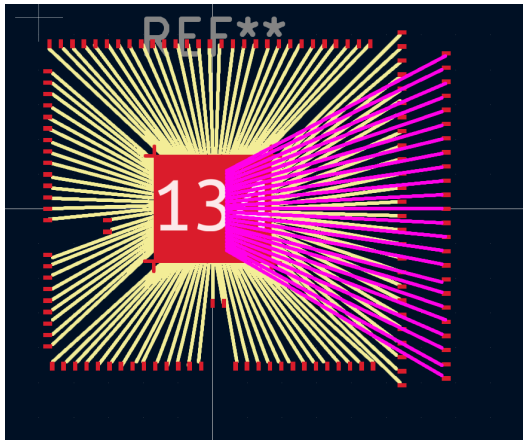
Power

Mother board

Daughter board

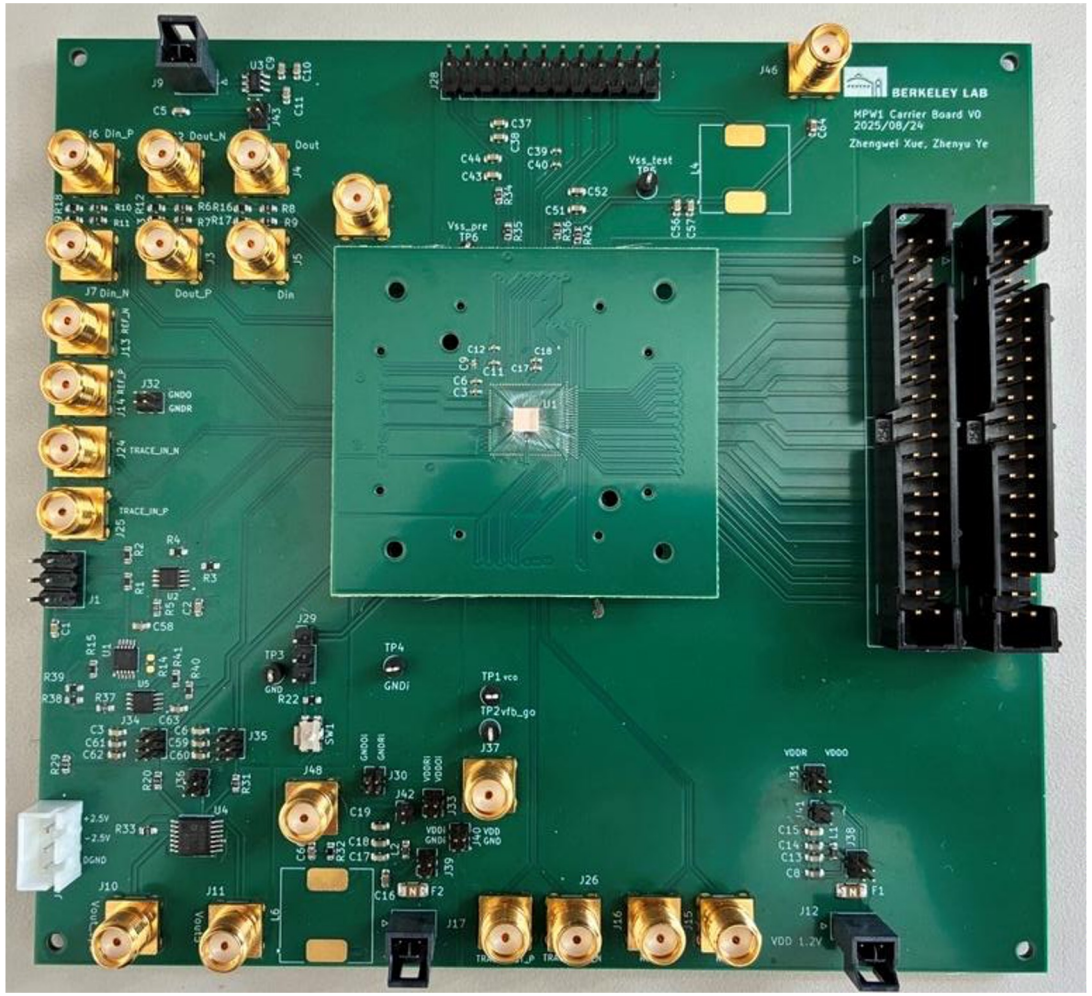
Wire-Bonding

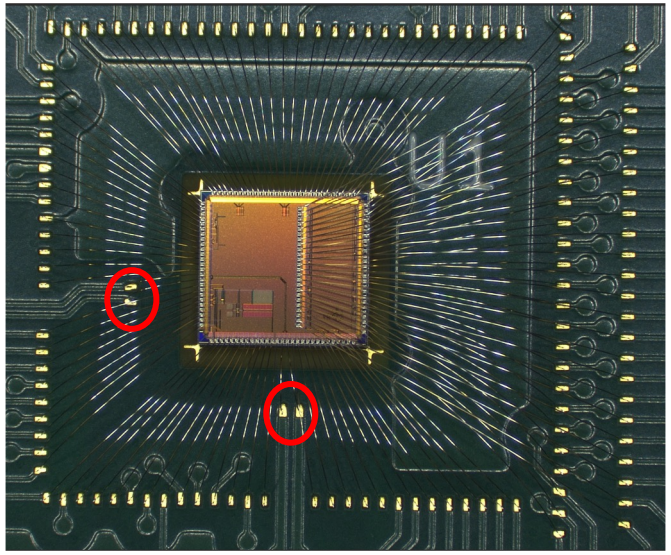




- Bonding pad size: 5 mil *10 mil. Pitch 11 or 18 mil (right side). 1 mil ~ 25 um
- Based on the limitations of the PCB manufacturer. It's hard to reduce the pad size and pitch.

MPW1 carrier board

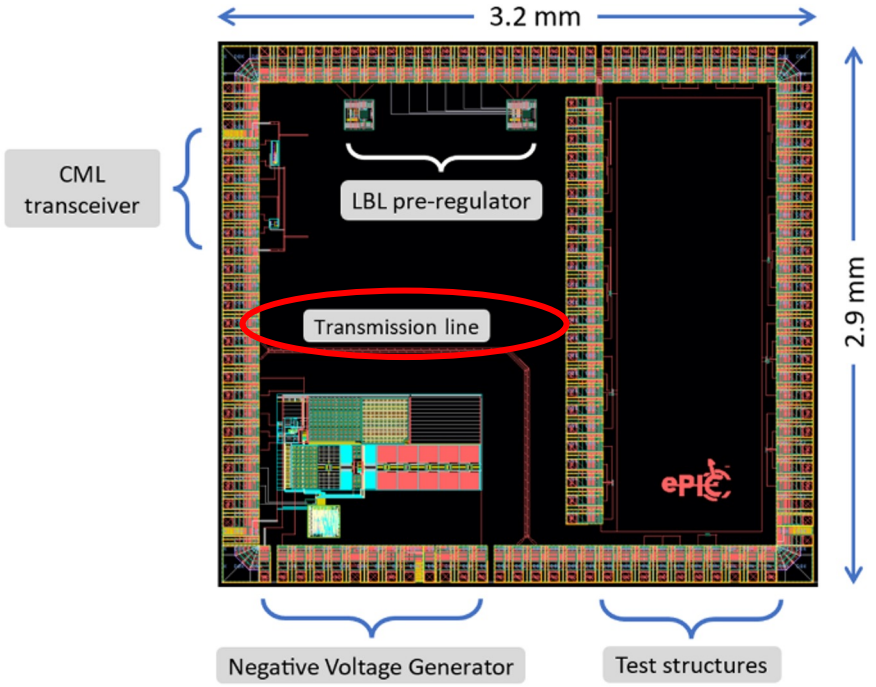




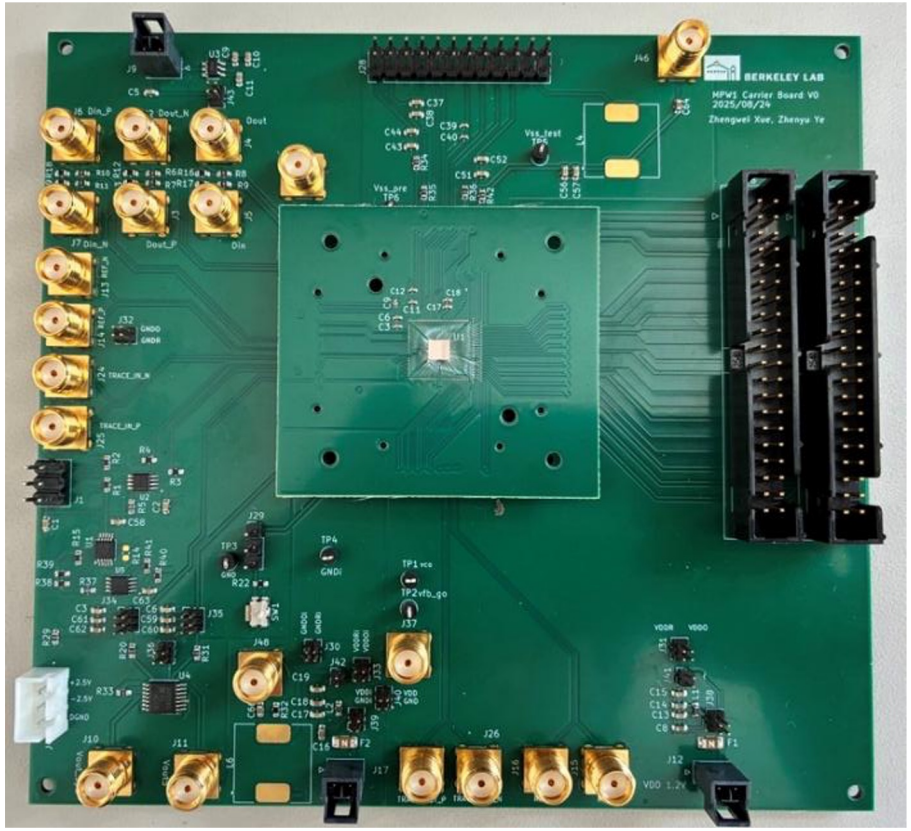
LBL MPW1 carrier boards (3 mother and 5 daughter boards) were delivered to LBNL on October 24th.

A MPW1 has been bonded to the daughter board.

Transmission line test



Rx of transmission line

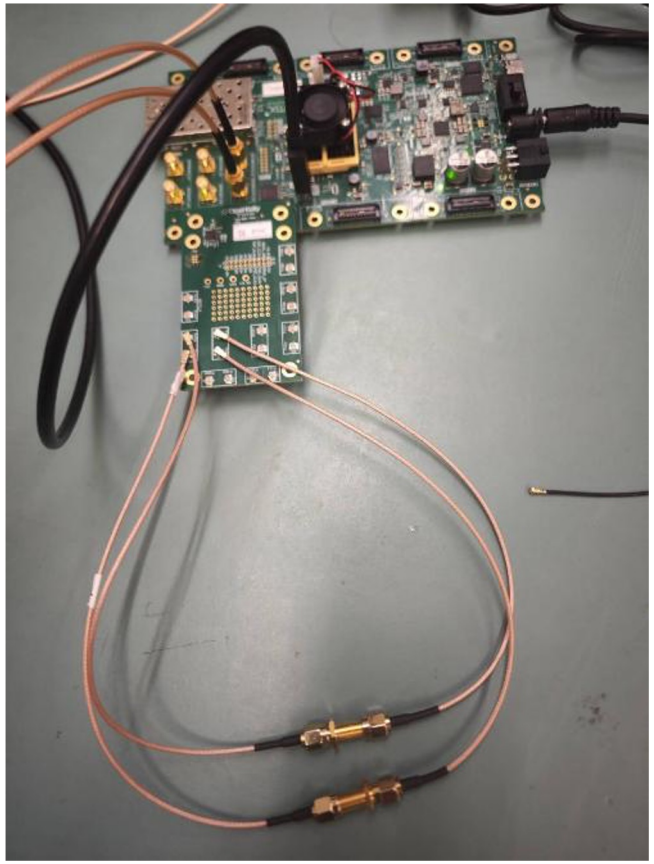


Tx of transmission line

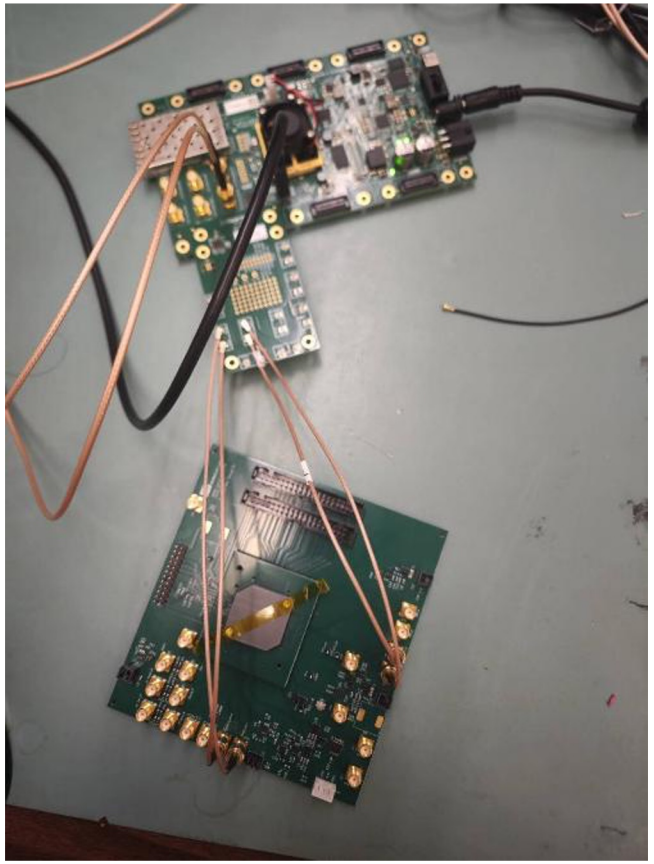
The is a pair of differential trace (Named "**Ref**") close to the trace of transmission line on PCB.

Their characteristic differential impedance (Z_{diff}) are controlled to 100 Ω.

Transmission line test

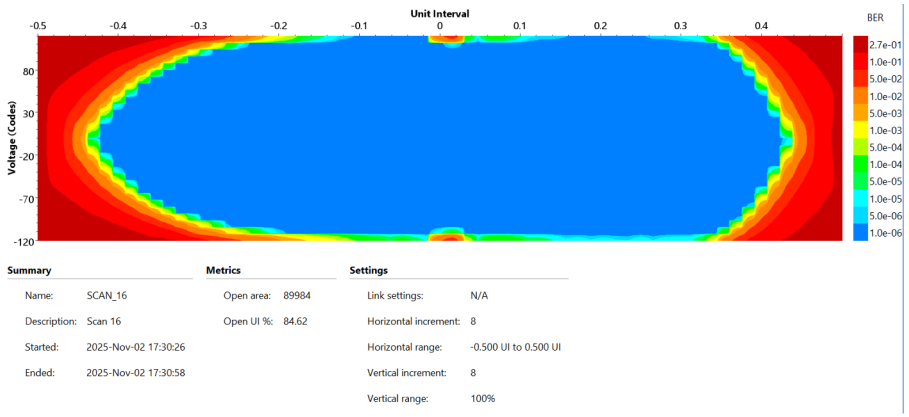


Directly connected

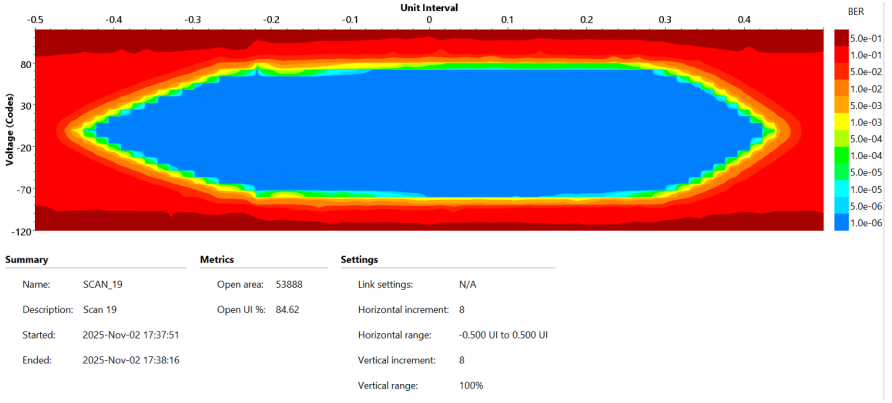


The signal travels along the traces on the PCB (and MPW1).

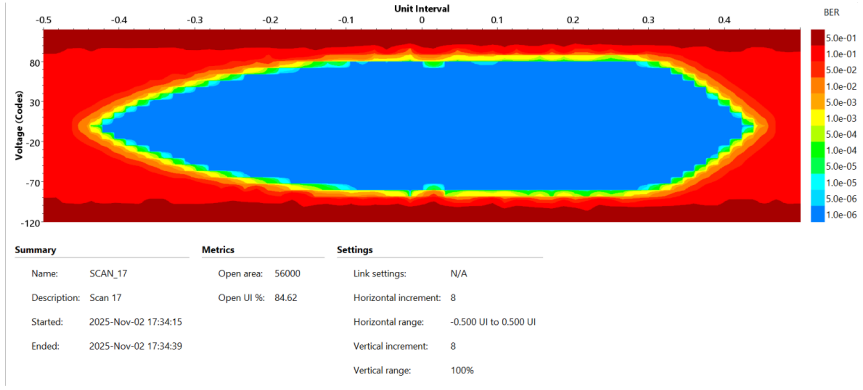
IBERT @ 1.28Gbps



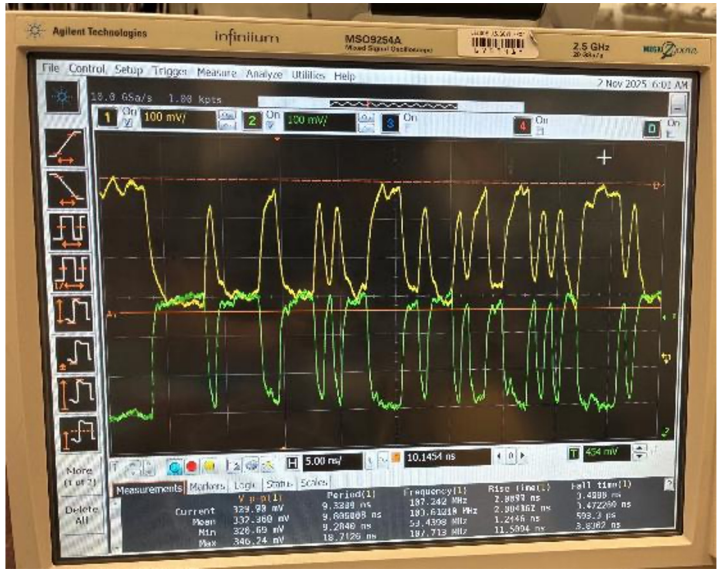
Directly connected: Open area 89984



Signal via PCB and MPW1: Open area 53888



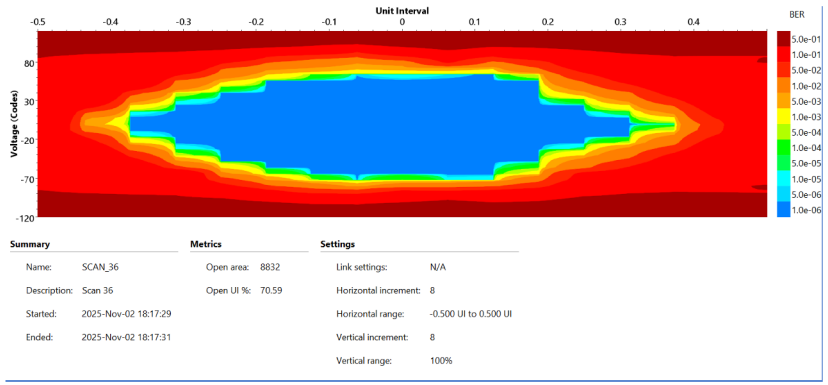
Signal on PCB only(Ref): Open area 56000



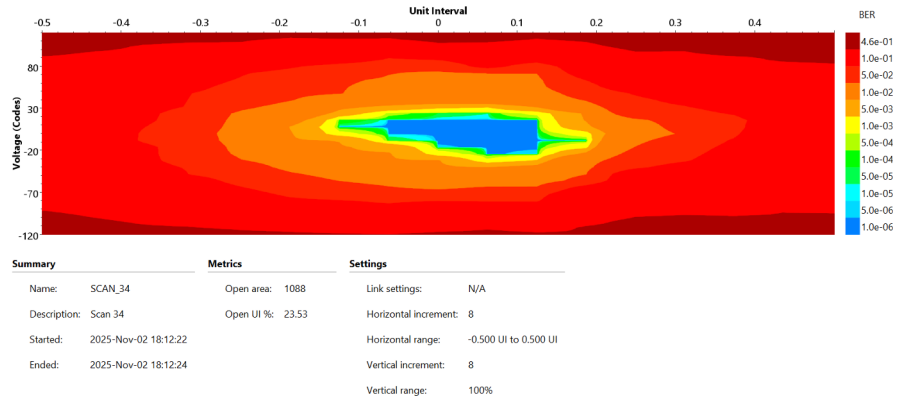
Yellow: Trace in MPW1
Green: Ref

Very good signal quality on both traces.

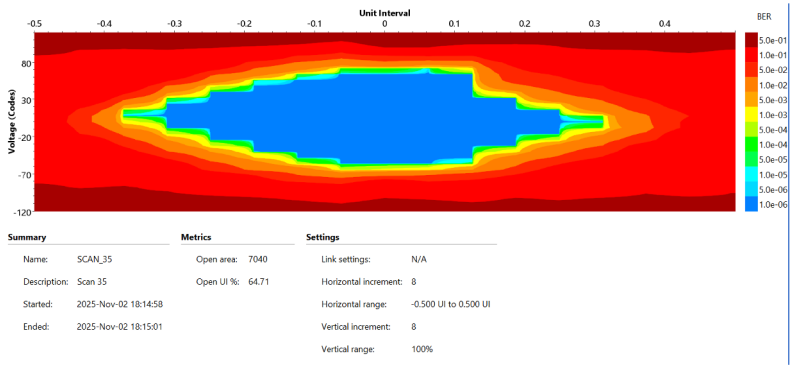
IBERT @ 5.12Gbps



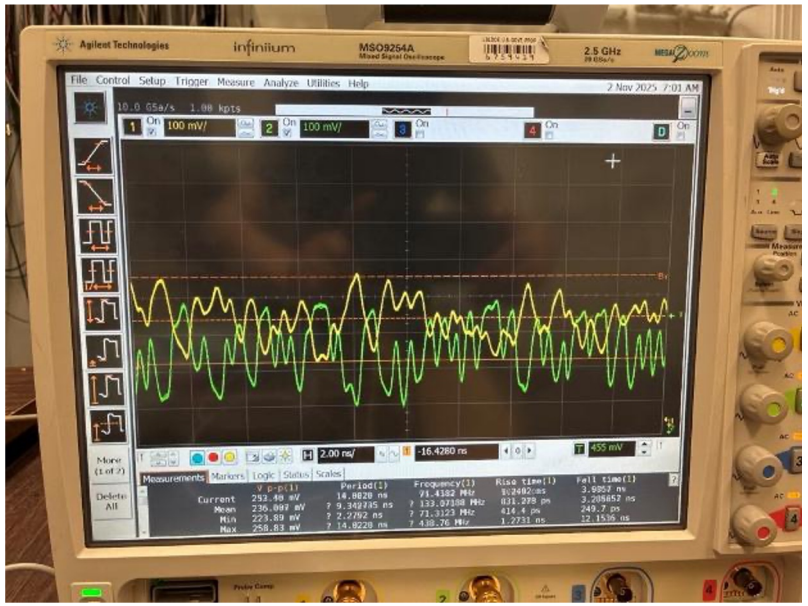
Directly connected: Open area 8832



Signal via PCB and MPW1: Open area 1088

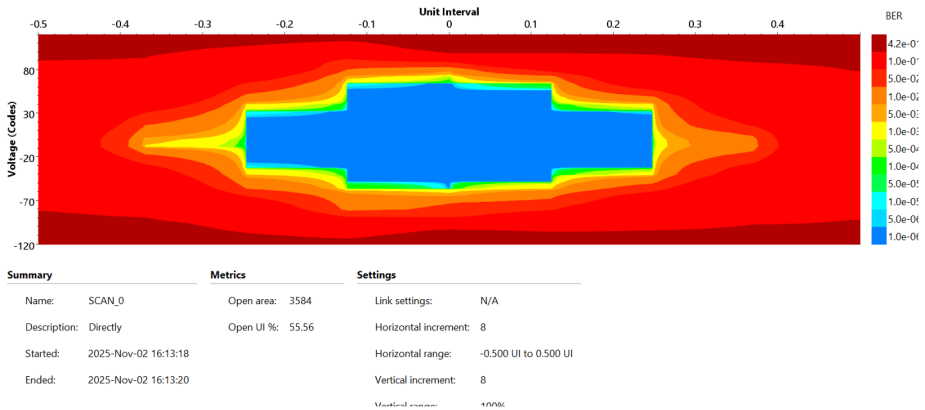


Signal on PCB only(Ref): Open area 7040

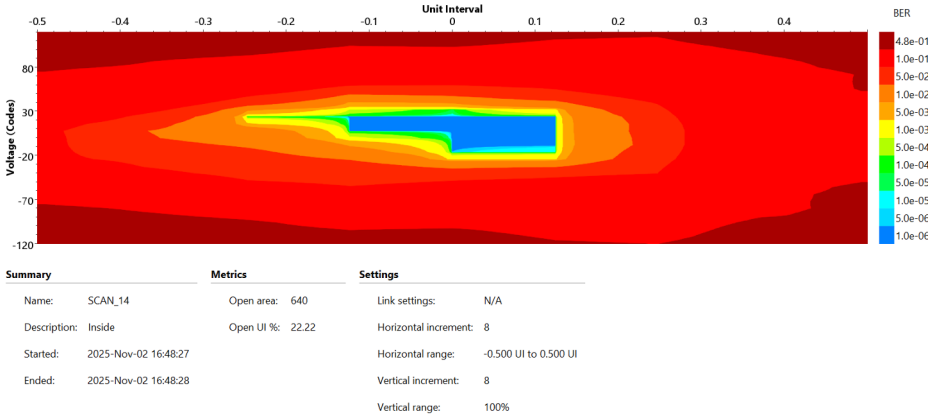


Yellow: Trace in MPW1
Green: Ref

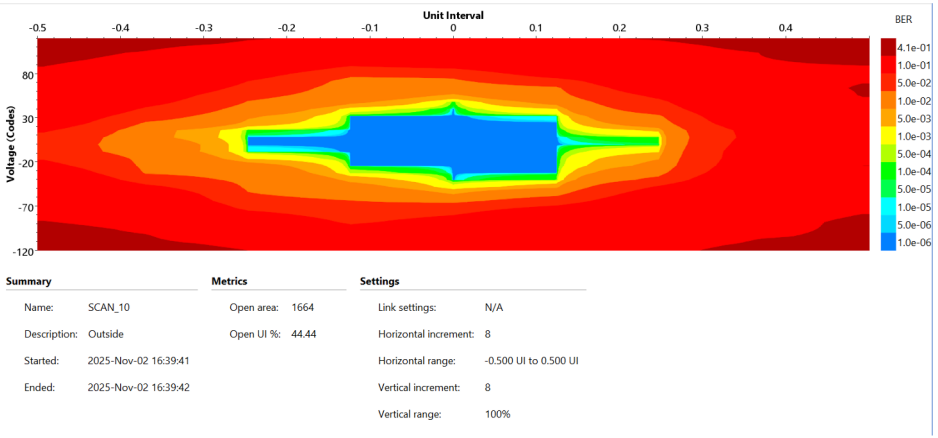
IBERT @ 10.24Gbps



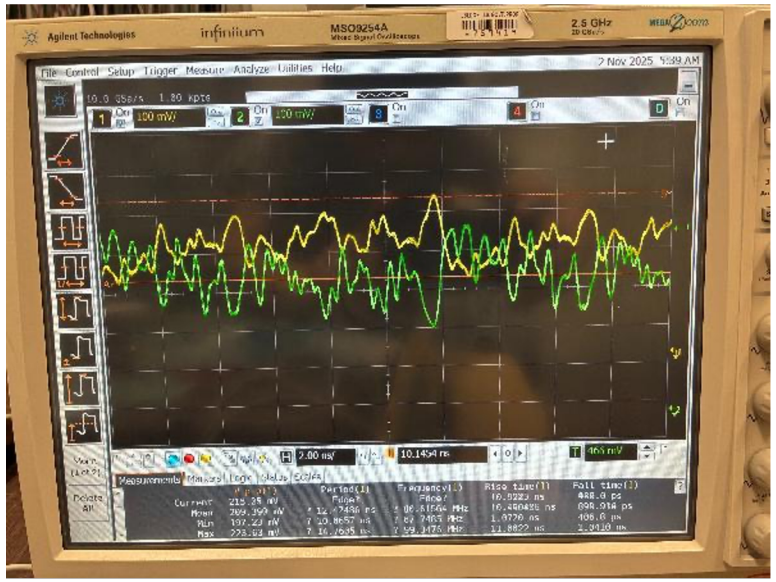
Directly connected: Open area 3584



Signal via PCB and MPW1: Open area 640

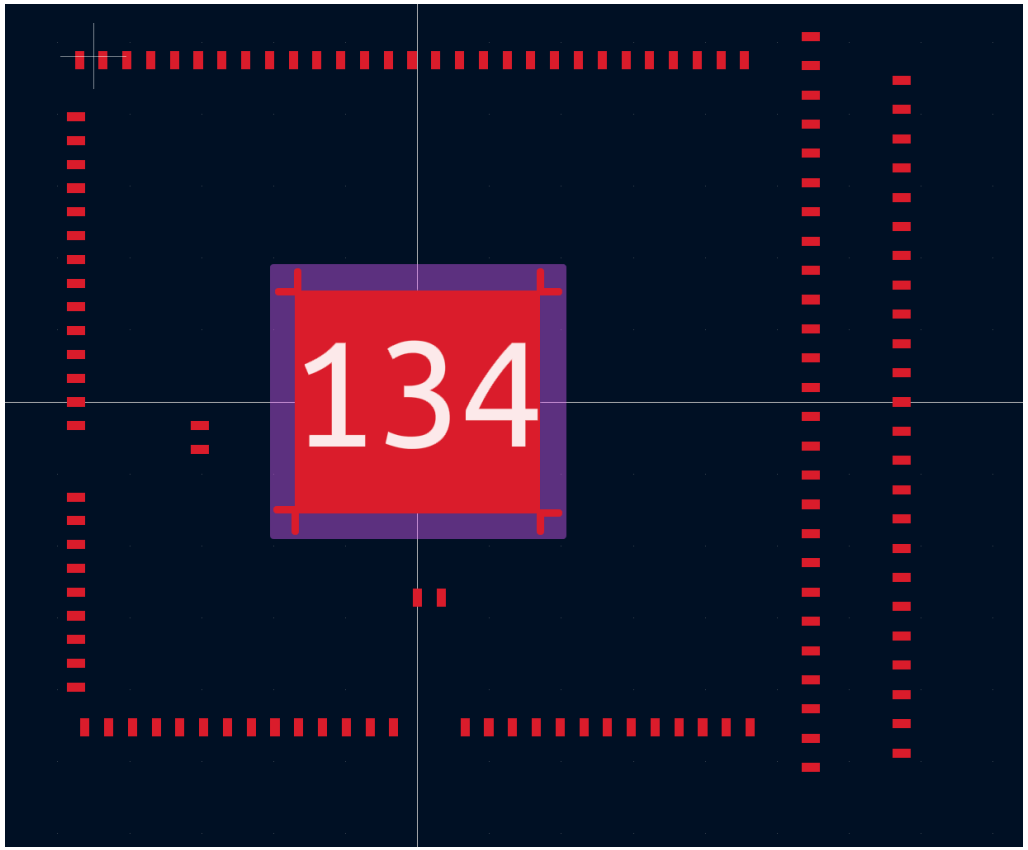


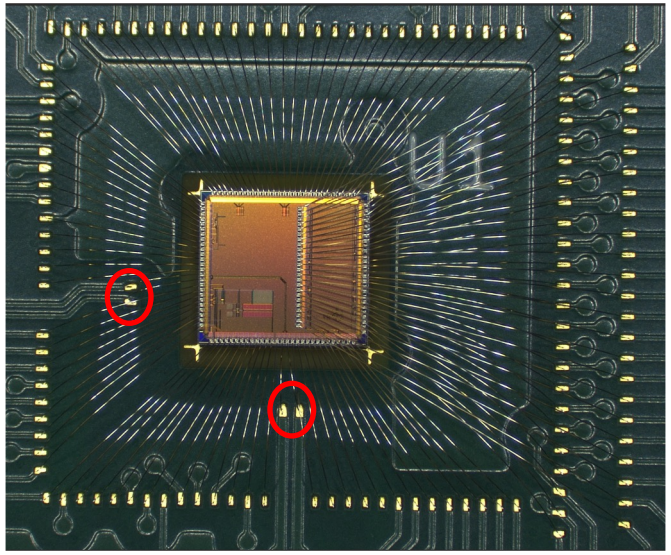
Signal on PCB only (Ref): Open area 1664



Yellow: Trace in MPW1
Green: Ref

Transmission line test (next step)

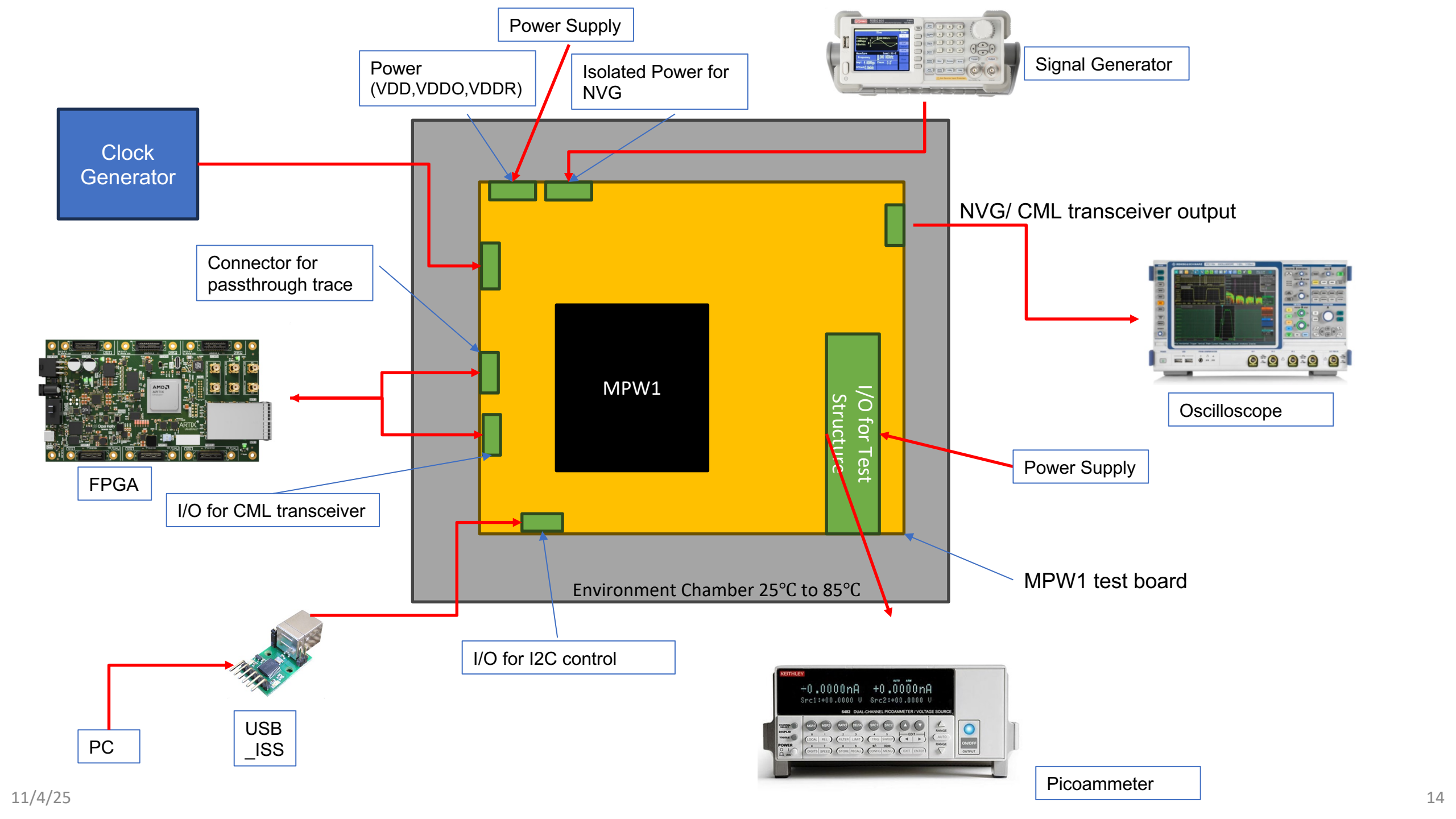




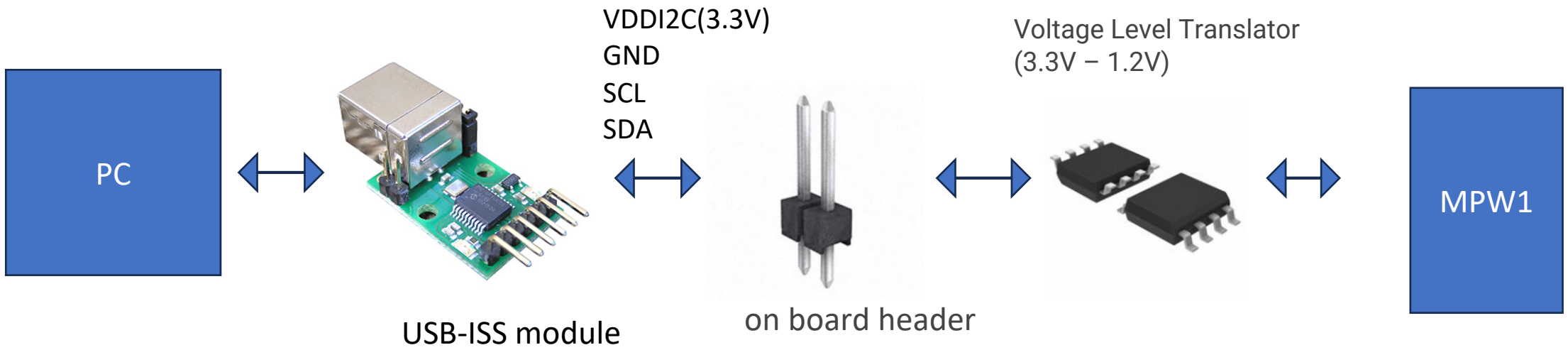
- Requested to direct wire bond between the pair of pads
- Repeat the Eye scan for this configuration and compared with Ref and MPW1 results

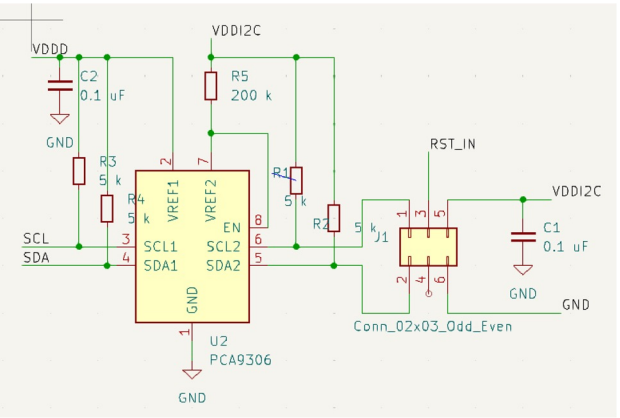
Summary and Outlook

- LBL MPW1 carrier boards were delivered, one MPW1 chip bonded
- Testing of MPW1 in progress.
  - Preliminary results suggest that the signal quality of the on-chip transmission lines may be suboptimal/compromised @ high data rate (5.12/10.24 Gbps).
  - Work on testing the other components also planned


Power Supply
Power
(VDD,VDDO,VDDR)
Isolated Power for
NVG
Signal Generator
Clock
Generator
Connector for
passthrough trace
NVG/ CML transceiver output
MPW1
I/O for Test
Structure
Oscilloscope
FPGA
I/O for CML transceiver
Power Supply
MPW1 test board
Environment Chamber 25°C to 85°C
I/O for I2C control
PC
USB
_ISS
Picoammeter

I2C Controller





Voltage Level Translator

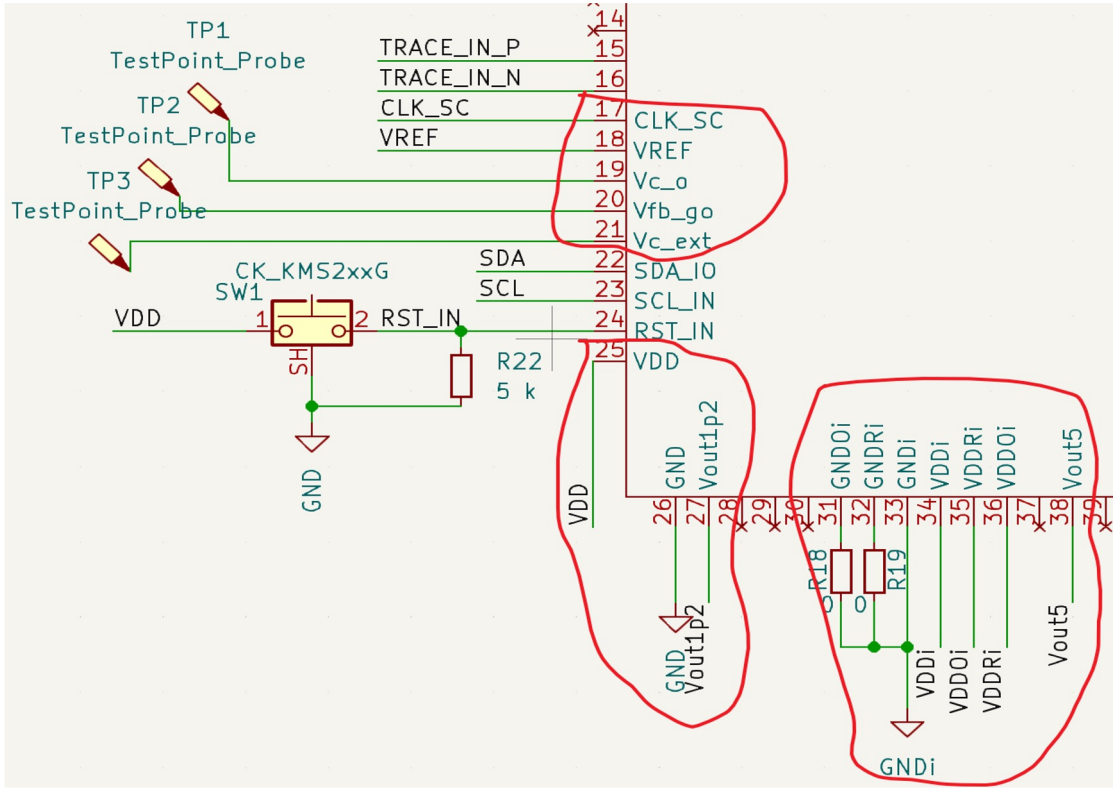
I2C register	AncASIC parameter
Register[0] <2:0>	EN <2:0>
Register[1] <7:0>	EN_{CP} <15:8>
Register[2] <7:0>	EN_{CP} <7:0>
Register[3] <7:0>	I_{integ} <15:8>
Register[4] <7:0>	I_{integ} <7:0>
Register[5] <7:0>	I_{vco} <15:8>
Register[6] <7:0>	I_{vco} <7:0>
Register[7] <7:0>	I_{off} <15:8>
Register[8] <7:0>	I_{off} <7:0>

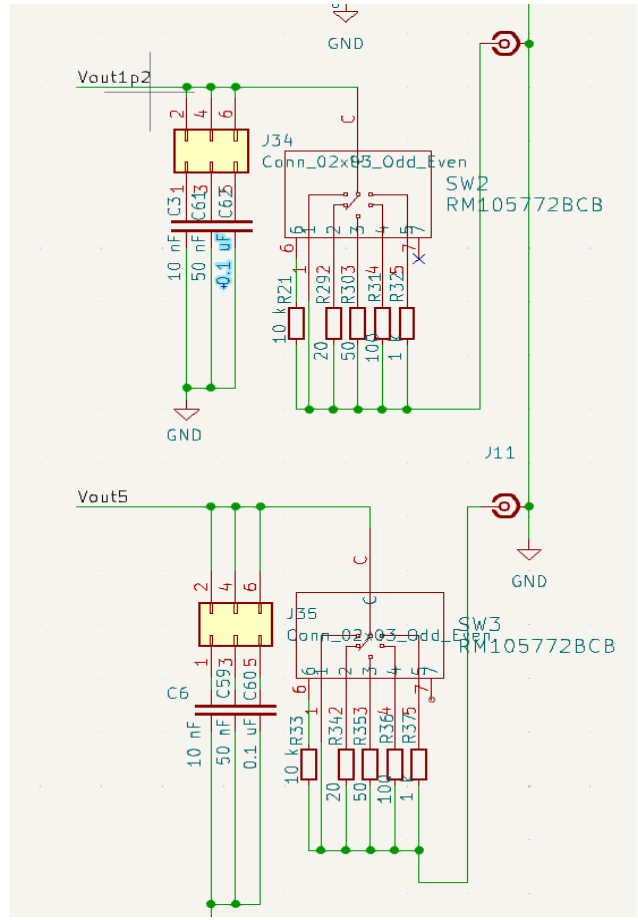
Parameter	Description
Iinteg	bias current for the SC integrator
Ivco	bias current for the VCO
Ioff	bias current for the offset generator
EN_{CP}	enable branches of the main charge pump and RF driver
EN<2>	selects VCO control voltage (Vc) - 0 = external control voltage - 1 = output of the SC integrator
EN<1>	Enable RF clock for main charge pump
EN<0>	Enable RF clock for aux. charge pump

Register map and Description

Test plan: Register Write/Read;
Single event upset(SET) test.

Negative Voltage Bias Generator





- R_load: use rotary switch with resistors as R_load to measure step response.
- C_load: have a few capacitors 10 nF – 100 nF which are selectable through jumpers.

Negative Voltage Bias Generator

Test Plan:

1.Output range

Change Verf, verify:
$V_{OUT} = -(20/3)V_{REF}$.

2.Line regulation

Change VDD (1-1.4V), get the curve between VDD&Vout;

3.Transient response

Catch the waveform of Vout & Vdd. estimate the rise time, settling time, and peak overshoot as a function of VREF. Repeat for different values of the load current, I_load.

4.Loop bandwidth

Repeat test 3 in different f_sc. Verify loop stability.

5.Power supply rejection ratio (PSRR):

Inject sinusoidal ripple on the power VDD, measure the ripple on Vout

6.Output noise and ripple:

Use oscilloscope record Vout in different Vref & I_load, Analyze the output histogram, peak, rms and frequency spectrum.

7.Temperature:

Repeat the above tests from 25℃ to 85℃

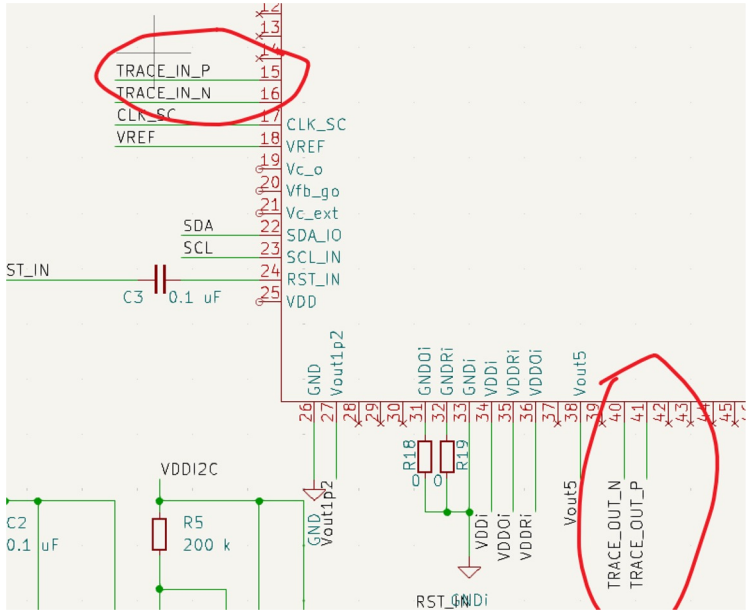
Necessary Instrument:

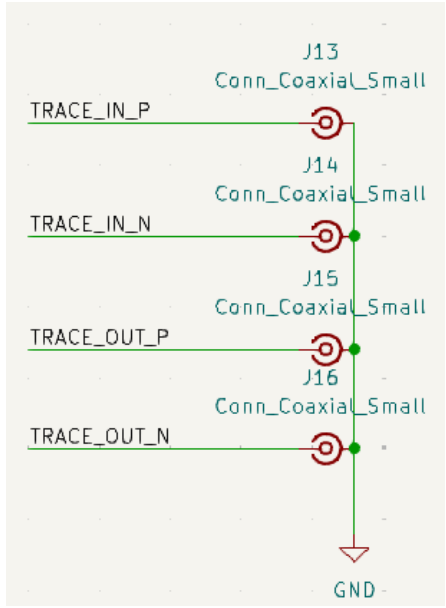
- **Power supply for VDD**
- **Power supply for Vref**
- **Oscilloscope**
- **Clock generator for CLK_SC**
- **Signal generator for power VDD with ripple**
- **environmental chamber for temperature test**

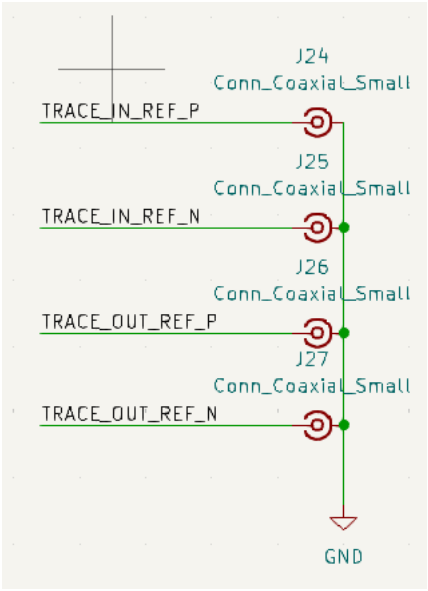
HS Data Transmission

3.4 Transmission line (passthrough)

The high-speed data coming from the sensor will be collected by a transceiver ASIC (lpGBT) and sent to the control room. Several options for the hardware implementation are under consideration and one of the options is to route this data through the AncASIC. In order to test and understand the effects of sending high-speed data through the AncASIC, a passthrough differential transmission line is implemented in this prototype using the thick top metal. Fig. 12 summarizes the layout of this structure, which is designed to have a characteristic impedance of $Z_0 \approx 100\,\Omega$.







Connected to High Frequency connector (e.g. SMA). An on-board differential trace is placed on PCB as the reference group.

Test Plan: Eye diagram @10.24Gbps

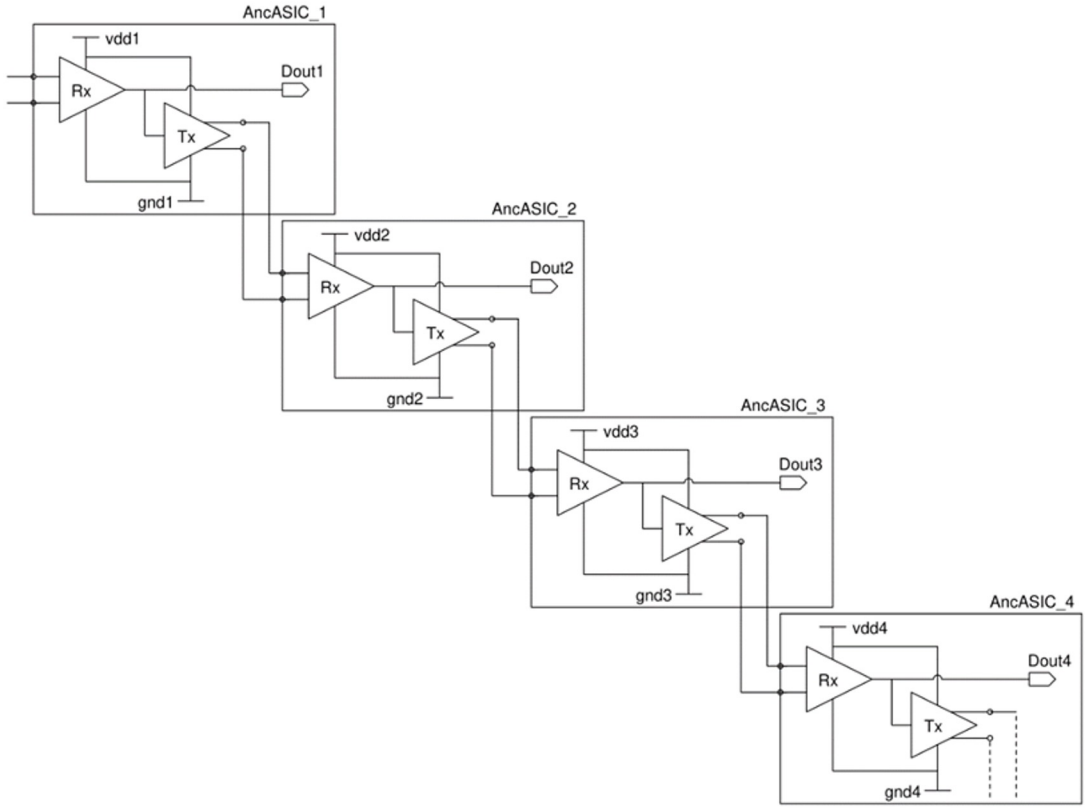
Necessary Instrument:

- FPGA for High-speed data generate and eye diagram

CML transceiver

Test plan:

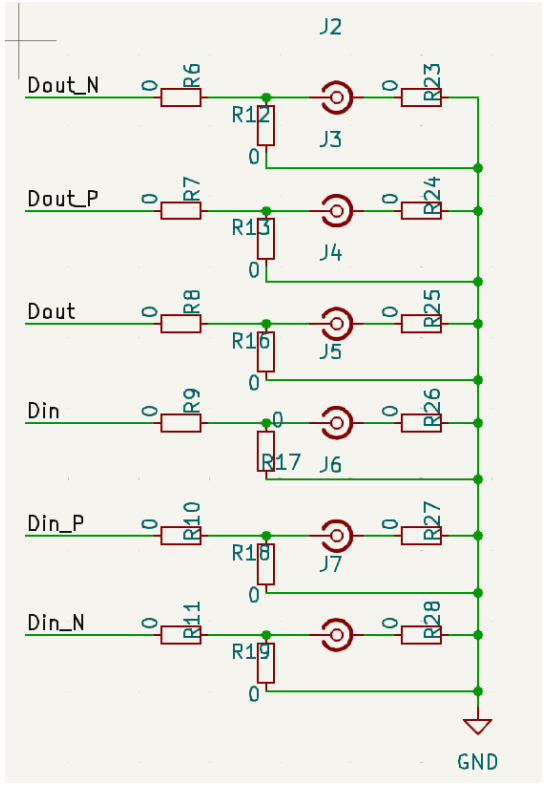
- Transmission loss, time delay, and eye diagram for **Single chip tests** and **Daisy-chain tests;**
- Do Daisy-chain test when the Tx and Rx are working in different common voltage.



Daisy-chain test structure

Necessary instruments:

- Oscilloscope
- FPGA
- Power supplies for set different common voltage



- Include footprints for AC/DC coupling selection;
- the connectors for the CML transceiver are connected to ground via a resistor (or resistors) instead of direct connection.

Test structure for irradiation tolerance

- **Standard V_T NMOS transistors:**

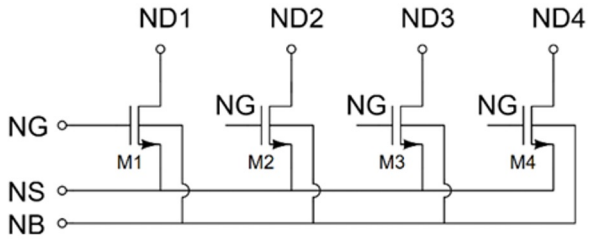


Figure 7: Standard V_T NMOS devices.

- **Standard V_T PMOS transistors:**

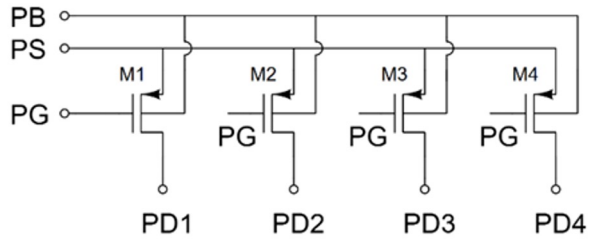


Figure 8: Standard V_T PMOS devices.

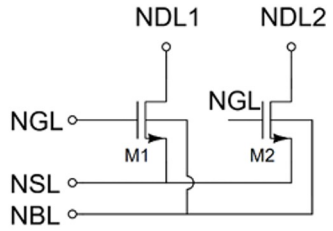


Figure 9: Standard V_T NMOS (large).

- **Standard V_T PMOS transistors:**
  - Large transistors for leakage measurements.
  - Two devices with different Deep Trench Isolatio

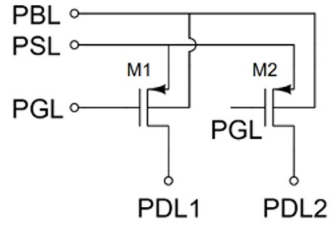


Figure 10: Standard V_T PMOS (large).

- **Additional devices:**

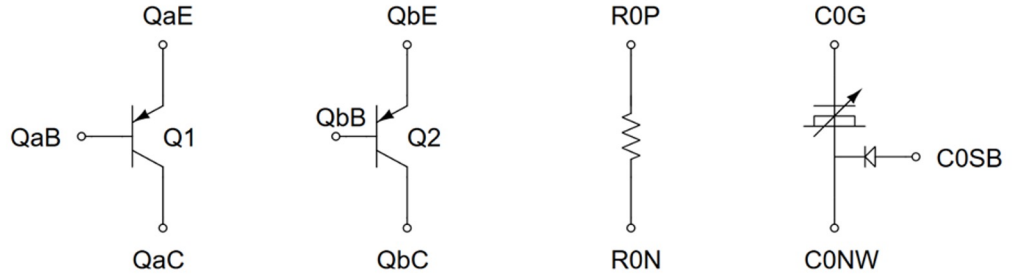


Figure 11: Additional test devices: BJTs, polysilicon resistor, and MOS capacitor.

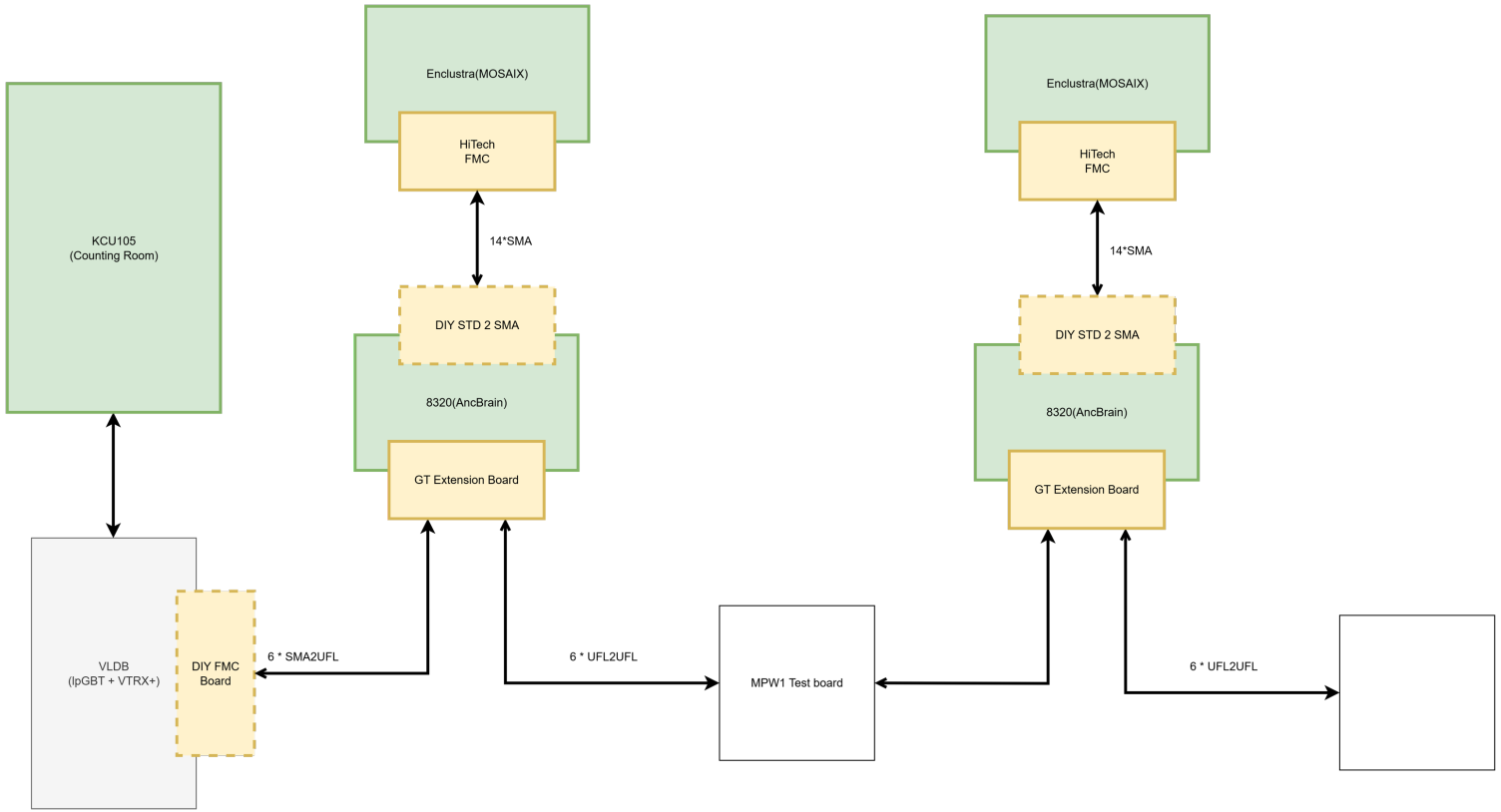
Test performance:

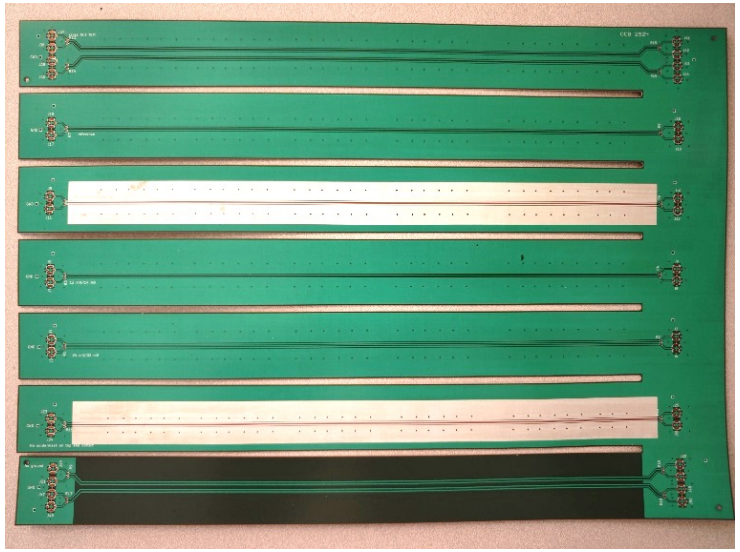
- Power consumption
- Threshold Voltage shift
- Leakage current

Necessary Instrument:

- Power Supply
- Picoammeter

Future test plan





1. Transmit CML slow control signals in full readout chain, including AncBrain emulator, MOSAIX sensor, lpGBT and counting room FPGA)

2. Transmit CML signals through FPCs instead of cables. The design of mother board will be modified.