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Wir schaffen Wissen – heute für morgen


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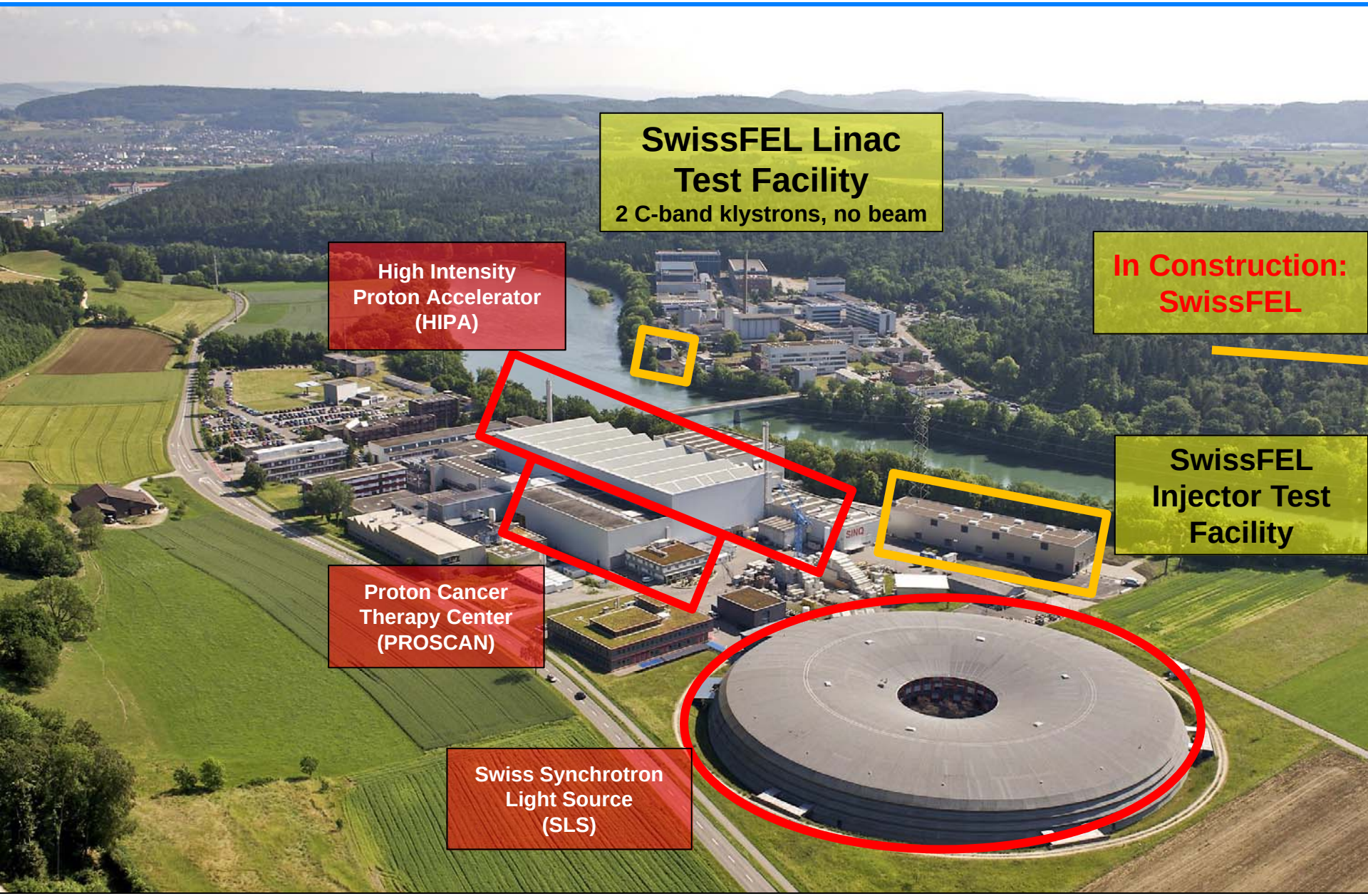
# The SwissFEL LLRF System - Concept and Realization

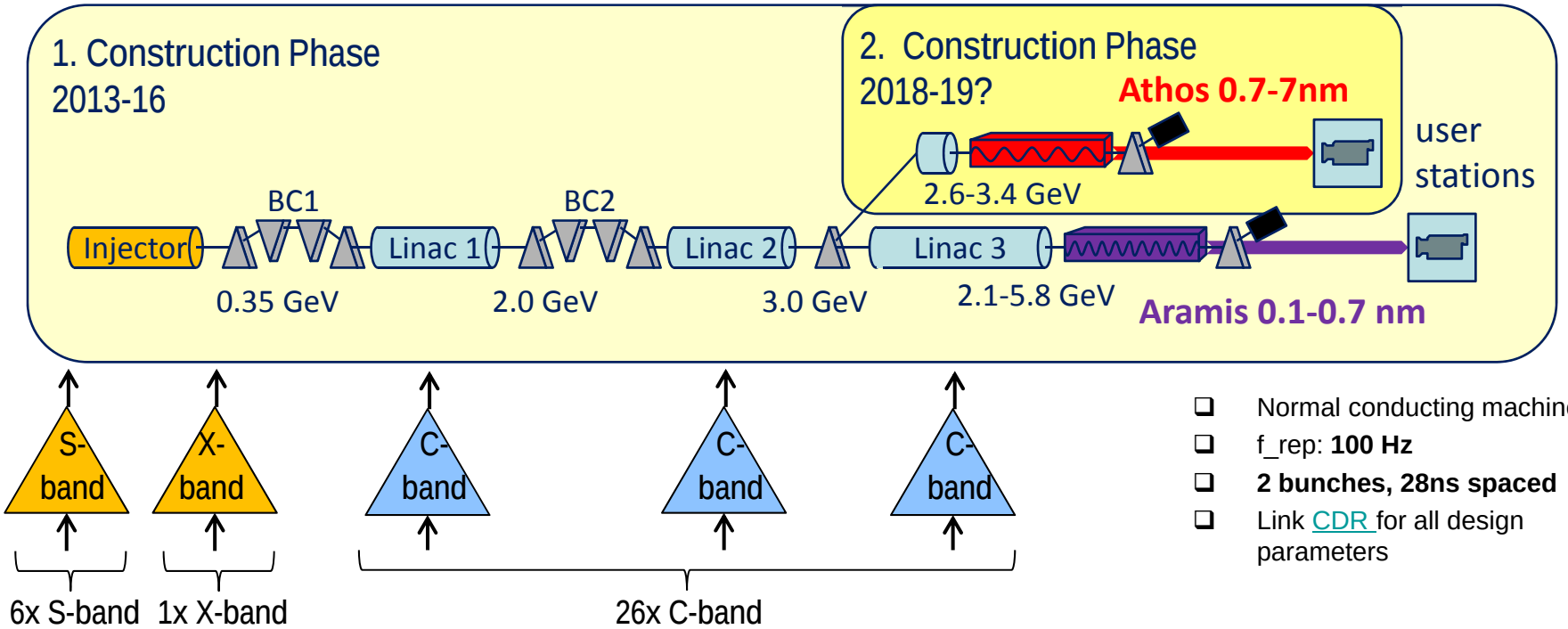
# Large Research Facilities @ PSI



# Outline

1. SwissFEL Project Intro
   1. Machine Requirements & Performance
   2. RF Stability Requirements for Subsystems
   3. SwissFEL Tunnel & Gallery Cross-Section
2. LLRF Concept
3. LLRF Realization
4. Conclusion & Outlook

# Machine Requirements & Performance




- Normal conducting machine
- f_rep: **100 Hz**
- **2 bunches, 28ns spaced**
- Link CDR for all design parameters

## SwissFEL performance calculations based on "expected performance" of RF stations:

| | Pulse-to-pulse stab. |
|---|---|
| S-band Phase* | 0.018° rms |
| S-band Voltage* | 1.8e-4 rms |
| X-band Phase | 0.072° rms |
| X-band Voltage | 1.8e-4 rms |
| Linac 1/2/3 Phase | 0.036° rms |
| Linac 1/2/3 Voltage | 1.8e-4 rms |

## SwissFEL beam performance calculations:

| electron beam parameters | stability |
|---|---|
| arrival time jitter | <20 fs |
| intensity jitter | <9% |
| energy stability | <1.6e-4 |

# RF Tolerances – Subsystem Requirements



## phase noise assumptions:

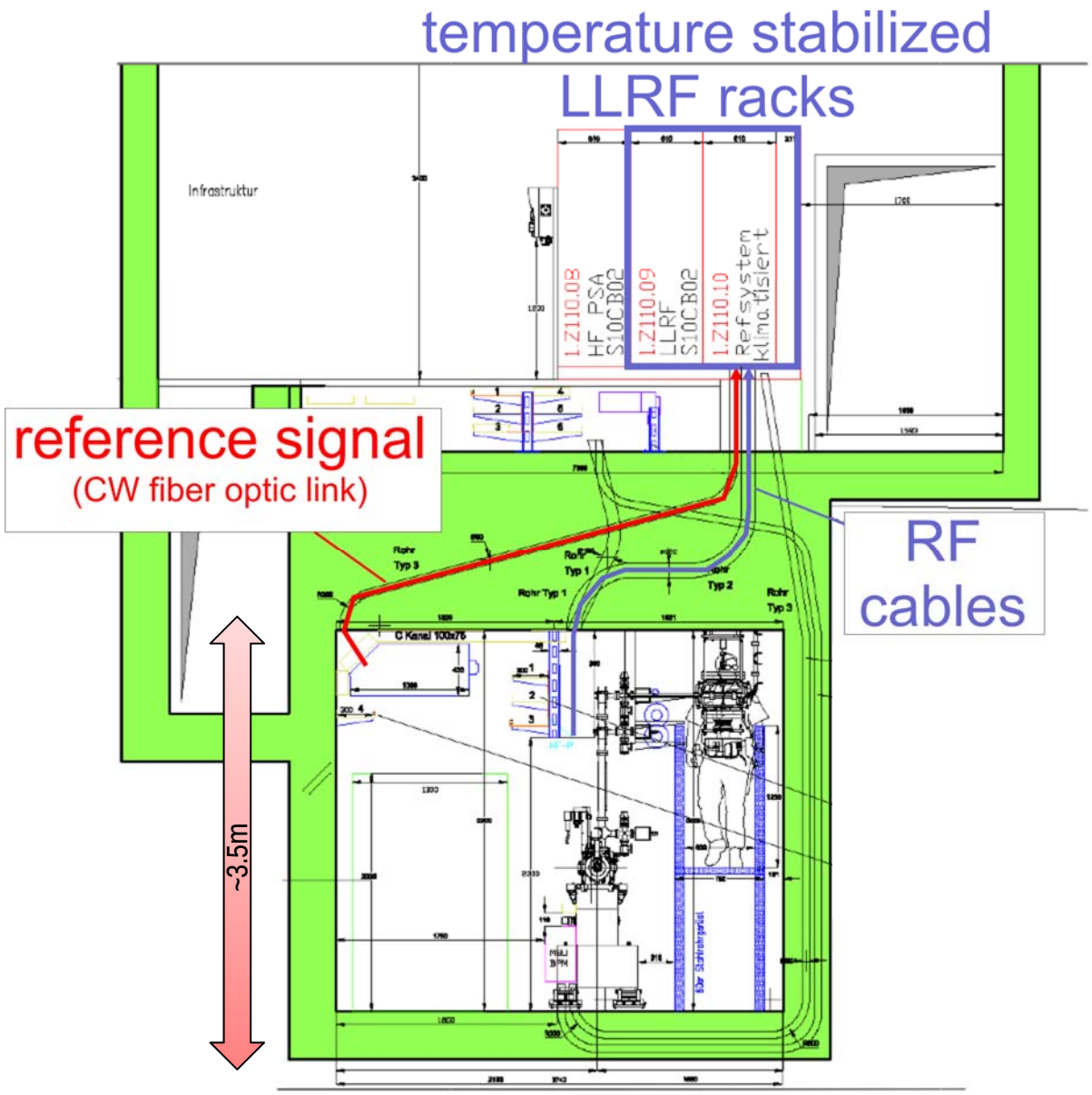
- uncorrelated contributions

$$\sigma_\phi = \sqrt{(\sigma_\phi)^2_{MO} + (\sigma_\phi)^2_{vec.\,mod.} + (\sigma_\phi)^2_{pre-amp.} + (\sigma_\phi)^2_{kly}}$$

- guaranteed max. phase noise contribution from master oscillator / phase locked oscillator (PLO) (10 Hz – 10 MHz)
- equal contributions (!?) of vector modulator, pre-amplifier, klystron (HV mod.) (10 Hz – 10 MHz)

| Frequency [MHz] | RF tolerance / phase noise (rms) [fs] / [°] | PLO guaranteed phase noise performance (rms) [fs] / [°] | max. added phase noise vec. mod. / pre-amplifier / klystron/HV mod. (rms) [fs] / [°] |
|---|---|---|---|
| 2998.8 | 17 fs / 0.018° | 9.3 fs / 0.01° | 8.3 fs / 0.009° |
| 5712.0 | 17 fs / 0.036° | 9.3 fs / 0.02° | 8.3 fs / 0.017° |
| 11995.2 | 17 fs / 0.072° | 7 fs / 0.03° | 8.8 fs / 0.038° |

# SwissFEL Tunnel & Gallery Cross-Section




- tunnel temperature: (24±0.1) ºC
- LLRF rack temp.: (24±0.1) ºC (2x air conditioned racks)
- technical gallery ambient temperature: (26±2) ºC
- Structures use a dedicated temperature stabilization system (25..35 ±0.01) ºC
- reference signal fiber optic links: Phase locked oscillator (PLO) in each temperature stabilized LLRF rack
- Emphasis on short RF measurement cables to the racks

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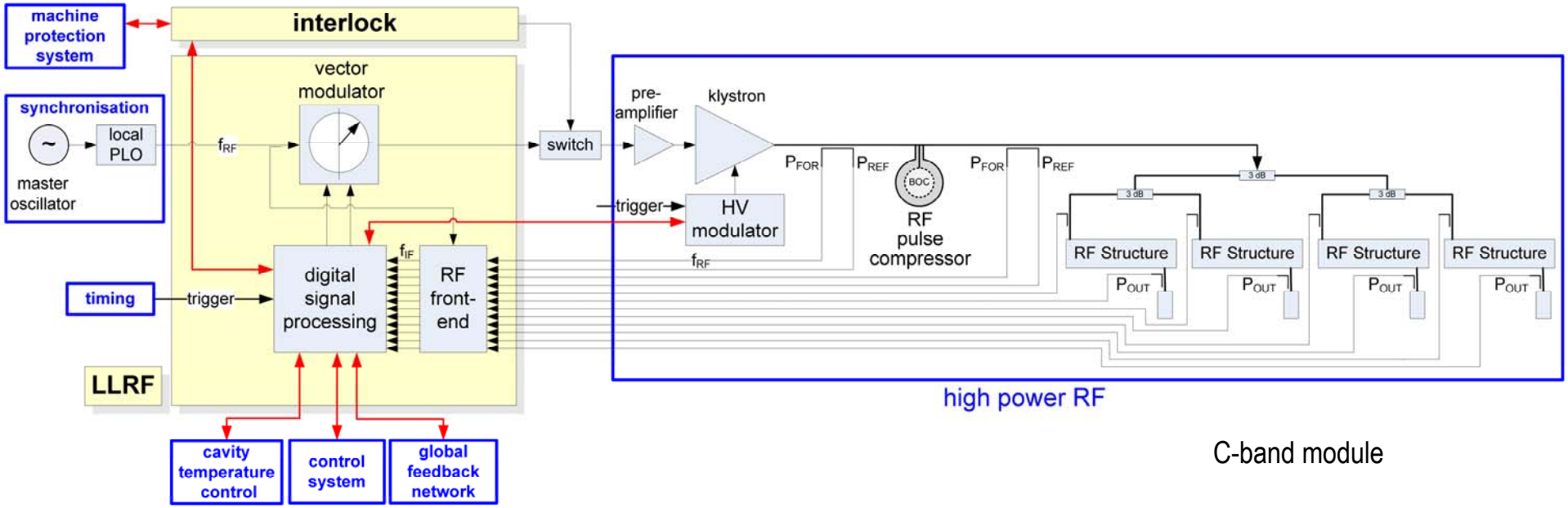
1. SwissFEL Project Intro
2. LLRF Concept
   1. LLRF Overview & Stability Strategy
   2. Frequency Choices
   3. Digital Hardware: Modular Unit
3. LLRF Realization
4. Conclusion & Outlook

# LLRF Overview / Stability Strategy




C-band module

## RF Stability Strategy:

- pulse-to-pulse stability:
  depends on MO/PLO, vector modulator, pre-amp., klystron/HV modulator, and structure temperature stability
- drift calibration (reference injection) to compensate drifts of LLRF measurement system
- RF pulse-to-pulse feedbacks (vector sum control)
- beam based feedbacks

## Consequence:

- **100 Hz repetition rate**: feedbacks can only suppress disturbances up to ~10 Hz
- **pulse-to-pulse / intra-pulse stability**: mainly determined by actuator chain (10 Hz-10 MHz)

# LLRF Design Concept / Frequency Choices



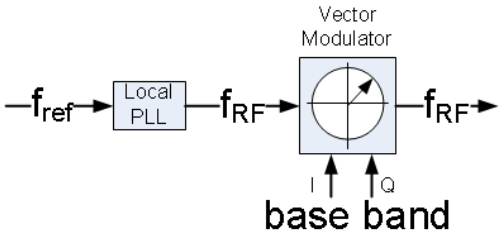
- number of RF channels: up to 24 channels per RF station ➔ ~800 channels for SwissFEL
- analog front-end: down-conversion to common IF frequency
- S-/C-band: single down-conversion to IF
- X-band: two stage down-conversion to IF

  (In-house S-band system with commercial 12/3 GHz RF front-end)
- common digital processing back-end

| RF freq. | IF freq. | ADC sampling freq. |
|---|---|---|
| S-band: $f_{SB}$= 2998.8 MHz | $f_{IF}= f_{SB}/72$ = 41.65 MHz | $f_S= f_{SB}/12$ = 249.9 MHz |
| X-band: $f_{XB}=4\times f_{SB}$= 11995.2 MHz | $f_{IF1}$= 2998.8 MHz<br>$f_{IF2}=f_{SB}/72$ = 41.65 MHz | $f_S= f_{SB}/12$ = 249.9 MHz |
| C-band: $f_{CB}=40/21\times f_{SB}$= 5712 MHz | $f_{IF}= f_{CB}/144$ = 39.667 MHz | $f_S= f_{CB}/24$ = 238.0 MHz* |

*compliant with TIARA / INFN Frascati requirements

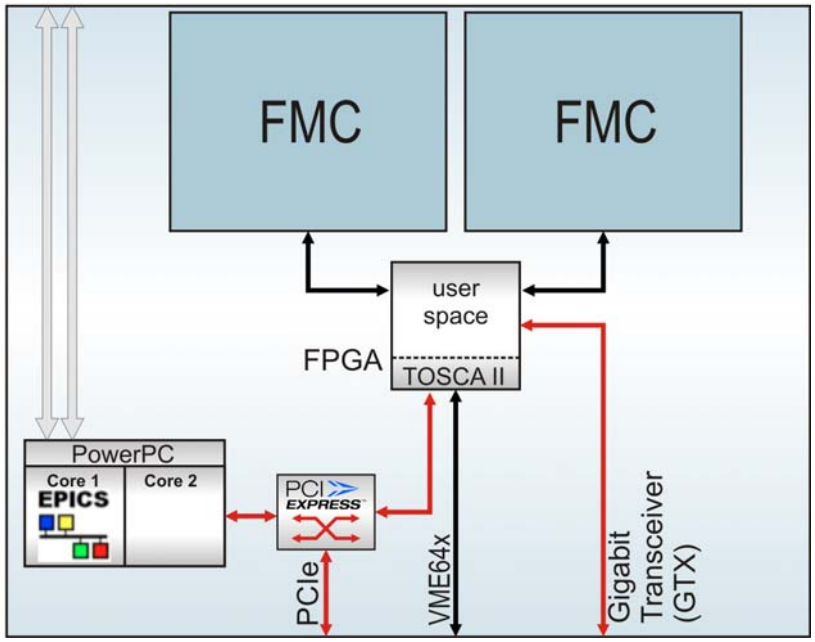
- non-IQ sampling: $f_{IF}/f_S$ = 1/6 (→ measurement bandwidth (FWHM): >34 MHz)
- baseband vector modulator



# Digital Hardware: FMC carrier as modular unit

ctrl. sys. interface

LAN
EPICS / EtherCAT




LLRF board-to-board communication

interface to global feedback network or LLRF board-to-board communication

## design issues:

- maximize synergy with other PSI facilities
  →VME64x processing board
  → joint venture with controls group
- digital processing board: collaboration with company IOxOS
  (board supplier, TOSCA II network on chip IP-core)
- ADC/DAC piggyback: 2x FMC
  (**F**PGA **M**ezzanine **C**ard, ANSI/VITA 57.1 HPC (High Pin Count))
- Dual-Core P2020 CPU } RT-Linux
- fast data processing in one FPGA Virtex-6 130LXT (smallest)
- scalable system (PCIe, VME64x)

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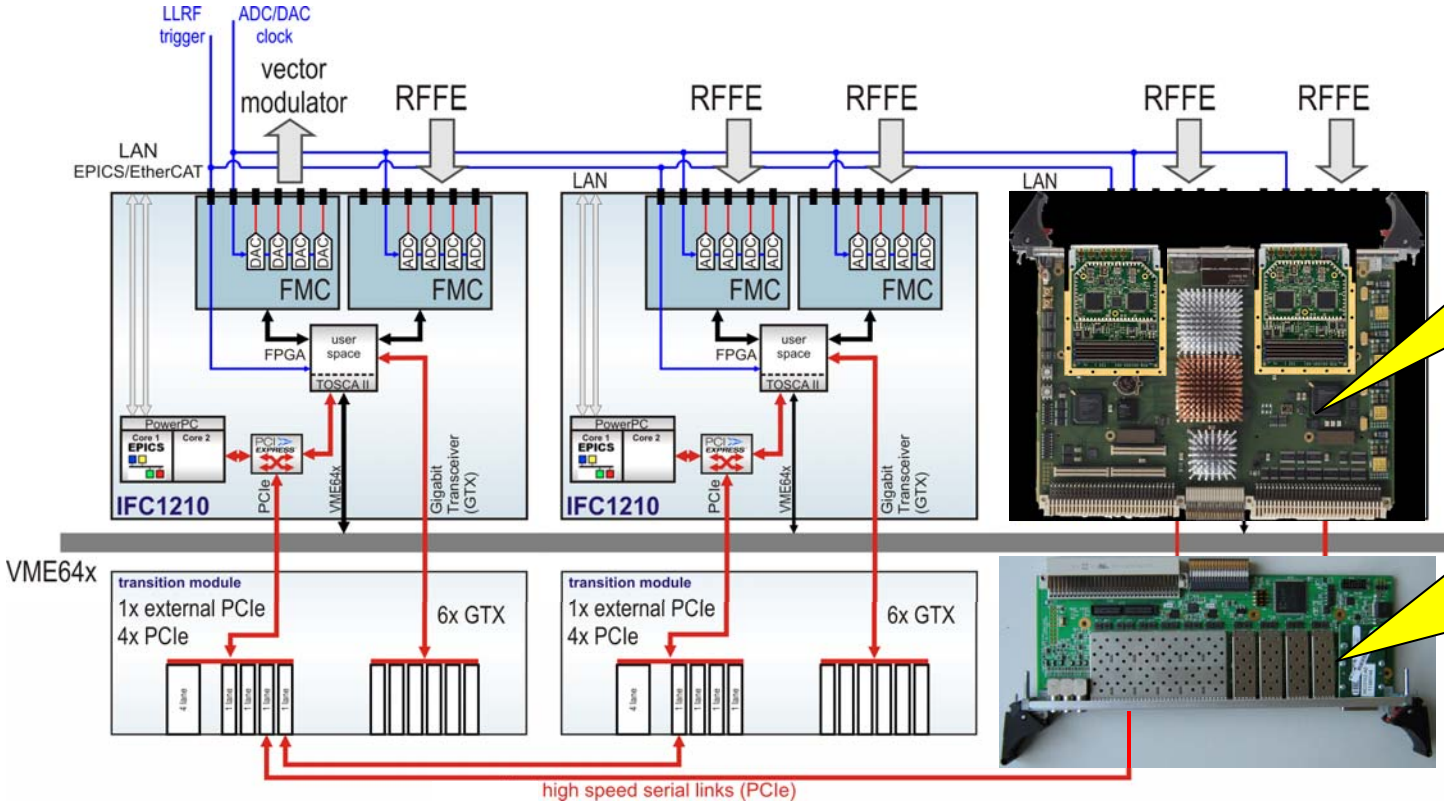
3. LLRF Realization
   1. Digital Platform: Building Block Status
   2. C-Band Prototype System, Lab Setup
   3. Software Stack Architecture
4. Conclusion & Outlook

# Digital Platform: Building Blocks Status




See poster #35: FMC ADC/DAC experiences for SwissFEL

See poster #56: PCIe and VME low latency data transfer in scalable LLRF systems

**status:**

- IFC1210 boards developed in collaboration with company IOxOS SA is commercially available
  - Several FMC ADC and DAC mezzanines tested
  - Inhouse developed transition module prototype available
  - PREEMPT_RT Linux + EPICS environment was set up together with Controls group, based on Denx.de ELDK (Embedded Linux Development Kit)

# C-band Prototype System, Lab Setup

For performance figures, see poster #57:
SwissFEL C-band LLRF Prototype System

## digital processing

VME:
1x MRF EVR-230RF
3x IFC_1210 carrier
3x transition card

FMC:
4x FMC-516 ADC
1x FMC-250 DAC

4U / 7 slot crate

C-Band Receiver:
4x 4 ch modules
16 channels total

RF receiver

2U

C-Band LO Unit:
Clock & LO Gen.
Baseband Vec. Mod.

LO generation

vector modulator

1U

# Software Stack Architecture Prototype System

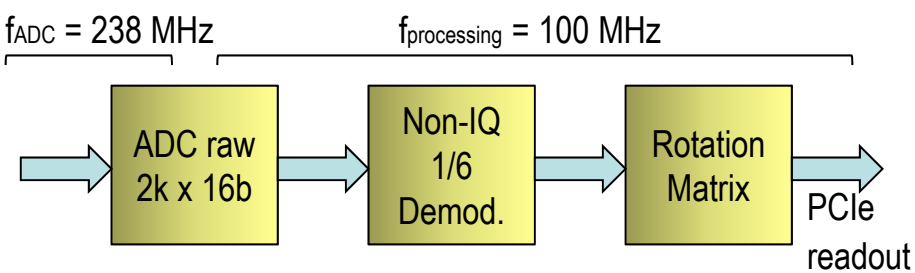
Subject to be optimized

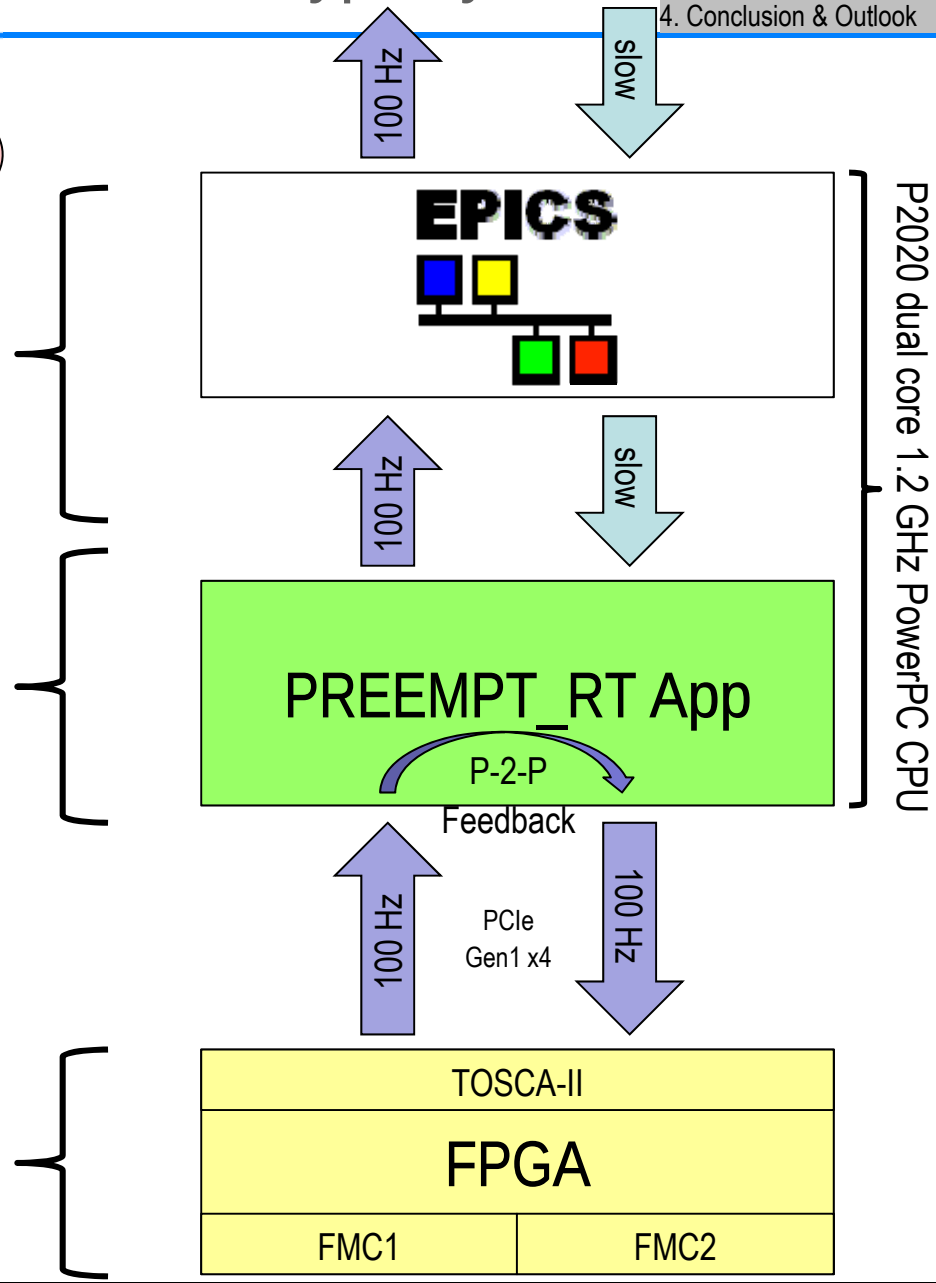
**EPICS** used only for control system interfacing

- 100 Hz archiving (data throughput rate ↑)
- Beam-synchronous data aquisition

Standalone PREEMPT_RT application

- Data forward to EPICS (data throughput rate ↑)
- Pulse-to-pulse feedback (latency ↓)



# Outline

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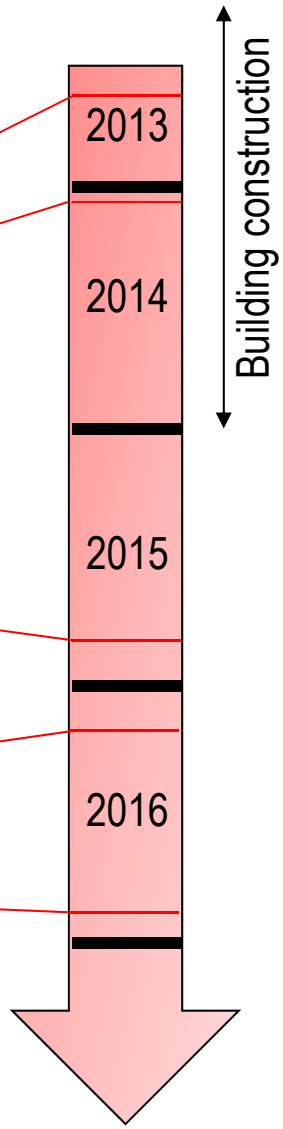
# Conclusion

- Having the ADC and DAC as modular unit such as FMC mezzanine gives predefined upgrade path.
- The use of synergies with Controls group was essential – at least for the EPICS / Linux software parts. Do not undervalue this part.
- Tests on a real environment test facility helps a lot for early debugging the system.

# Outlook (LLRF Milestones)

- LLRF read at C-band test facility
  - RF station 1: 1xBOC / 1x structure
  - RF station 2: 1xBOC / 4x structure
- 1st LLRF for injector ready
- 1st LLRF for linac ready
- First FEL beam



# http://www.psi.ch/swissfel-bauinfo/webcams

Picture G. Janzi, August 2013

# Outline

Reserve

# High Speed Communication Transition Module IFC_TC1

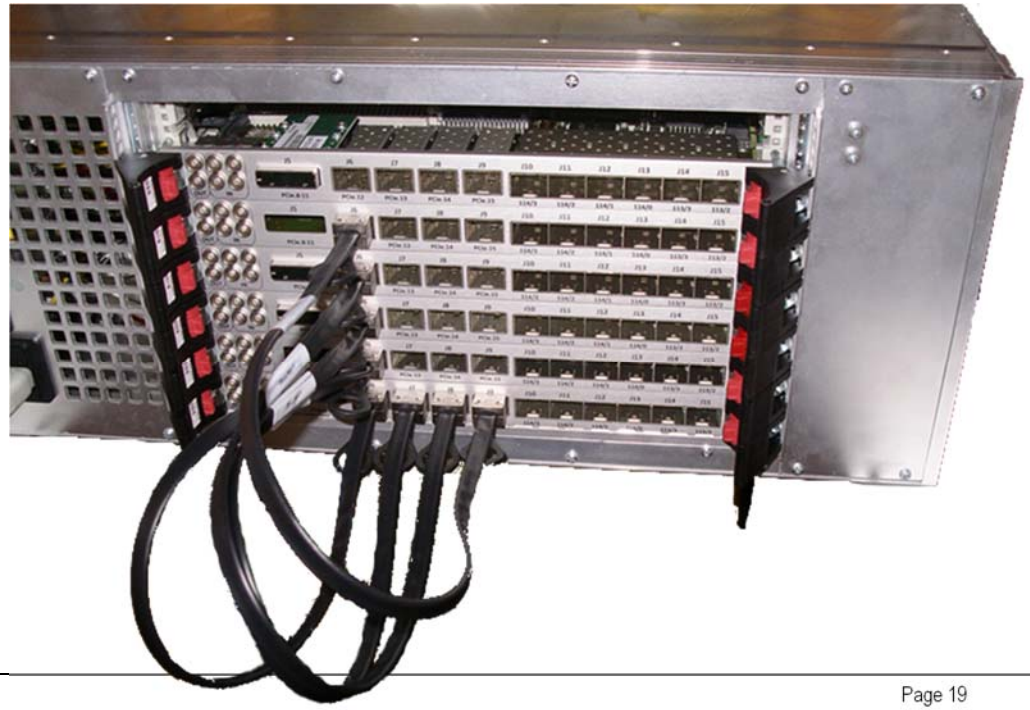
| GPIO | PCIe 4 lanes | 4 x SFP+ PCIe 1 lane | 6 x SFP+ up to 5 GBPS |
|---|---|---|---|

## High Speed Interconnection

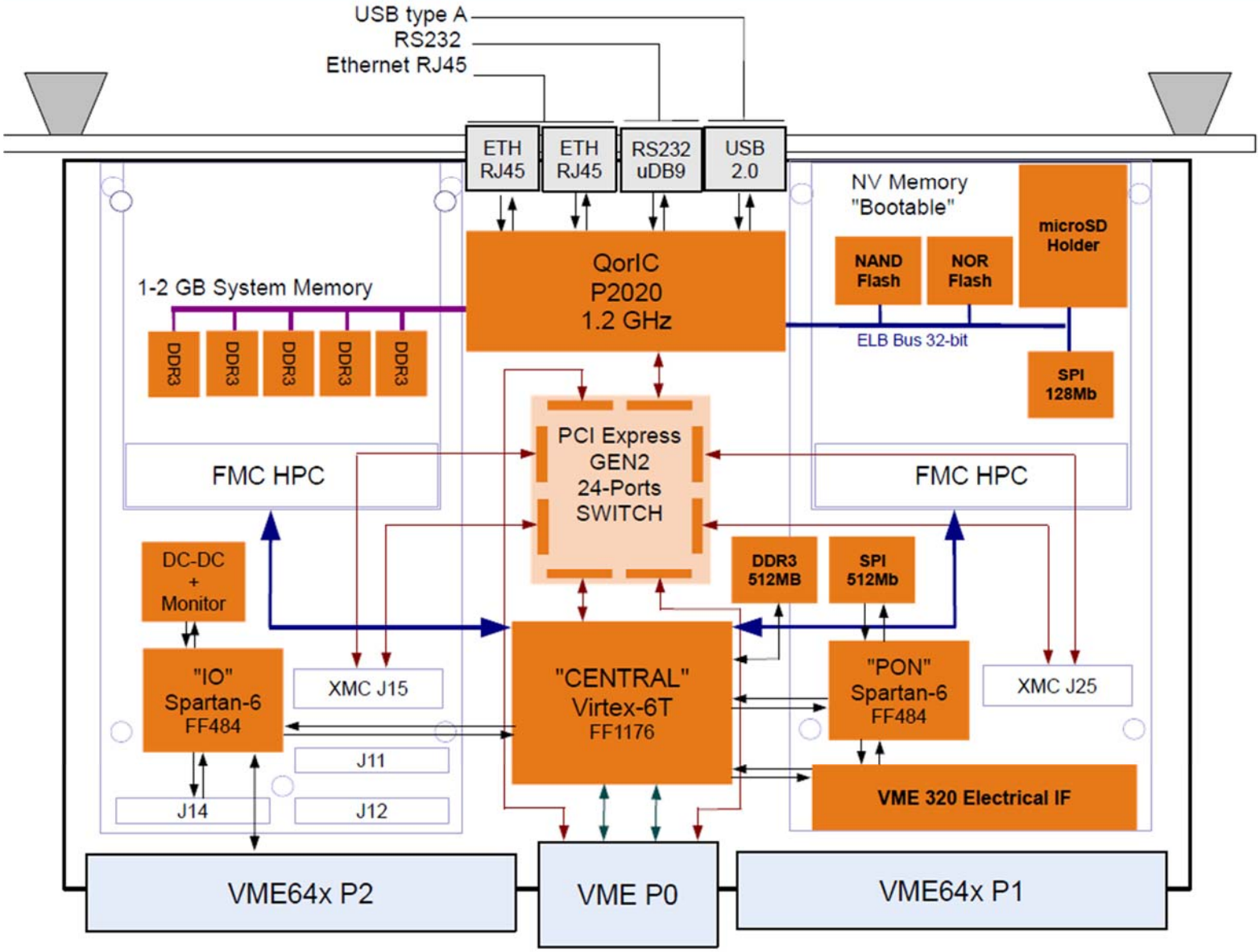
- **Parallel to VME bus**
- **4 x 500 MByte/s**
- **(VME 2eSST320: max 1 x 320 MByte/s)**

## "Best of Two Worlds"

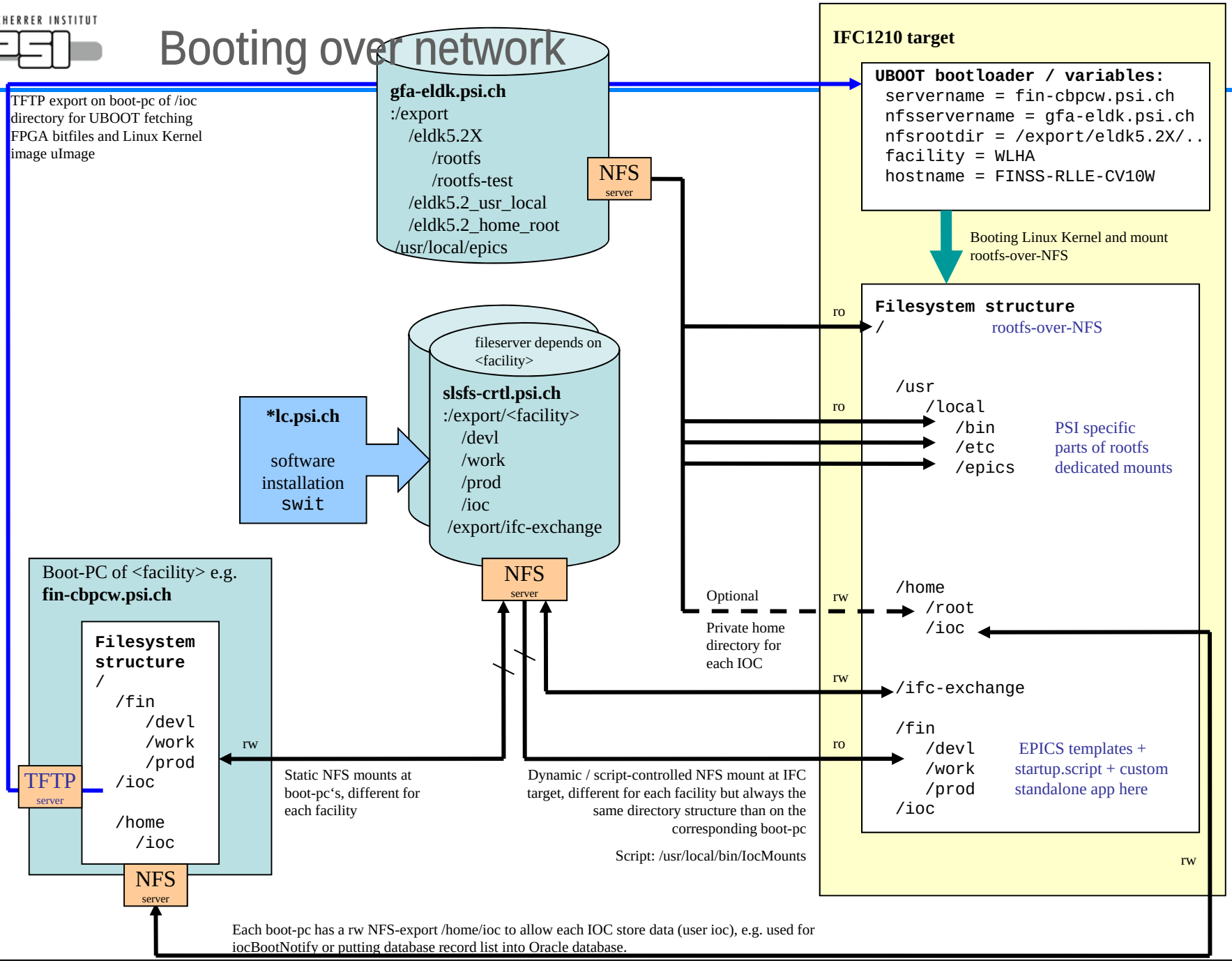
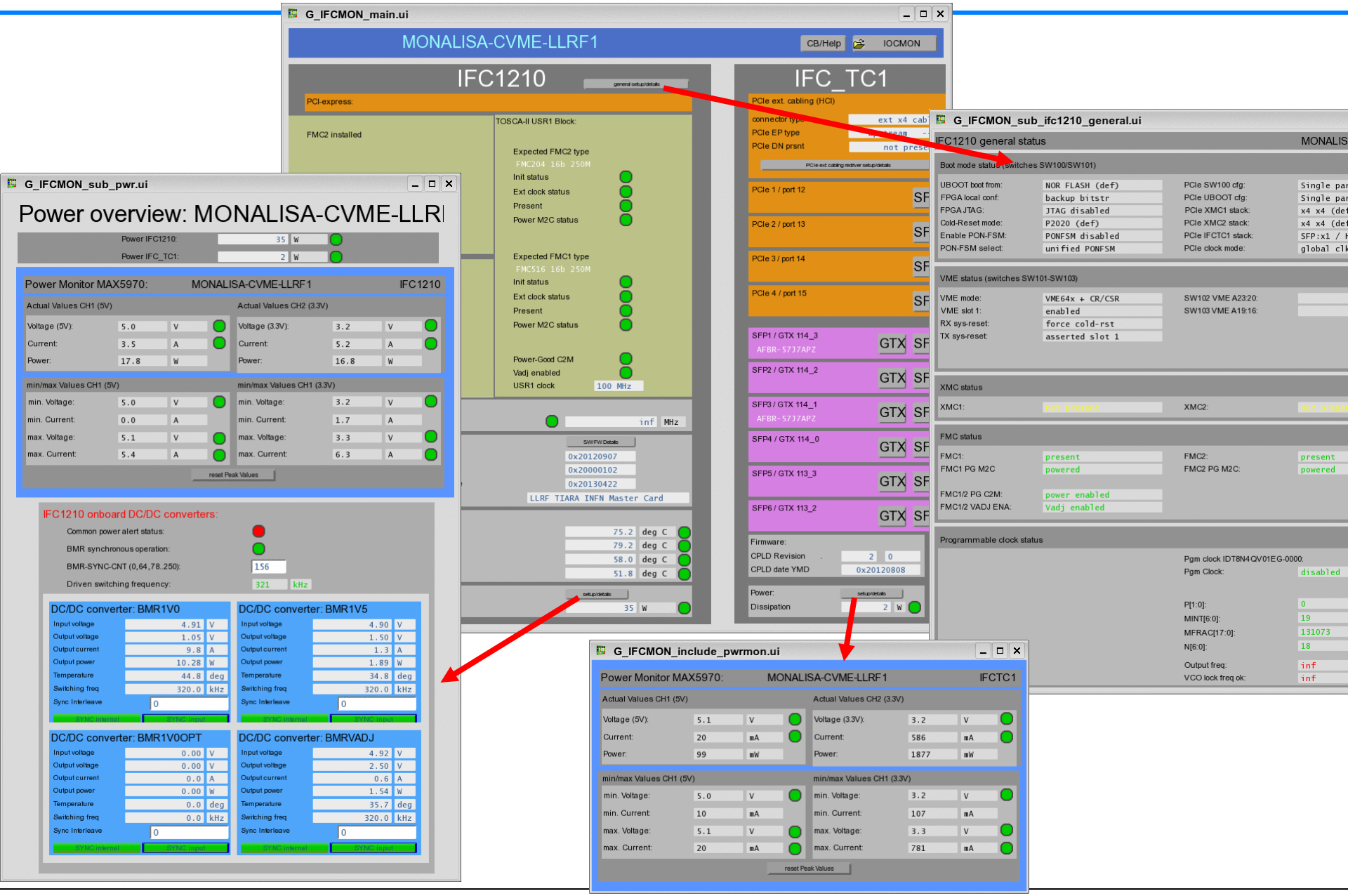
- **Fast dedicated links like in µTCA**
- **Traditional VME64x form factor for legacy I/O cards and crates**



# IFC_1210 Block Diagram



# Booting over network



# IFC1210 Carrier: Status and Monitoring Screens