

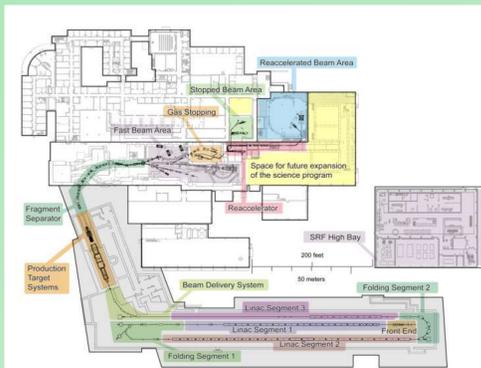
FRIB LLRF Controller

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Introduction

The heart of FRIB is a high-power CW superconducting linear accelerator that contains approximately 350 RF systems. The majority of the systems are either 80.5 MHz QWR cavities or 322 MHz HWR cavities with control requirements listed in the table below. This poster contains details of the 2nd FRIB prototype currently being tested on cavities.



FRIB RF Requirements for SRF Cavities

| Operating Mode | Frequency (MHz) | Dynamic Amplitude Error (s,%) | Dynamic Phase Error (s,deg) | Dynamic Amplitude Error (RMS,%) | Dynamic Phase Error (RMS,deg) | P_{avg} (W) | P_{nom} (W) | Qty |
|------------------|-----------------|-------------------------------|-----------------------------|---------------------------------|-------------------------------|---------------|---------------|-----|
| $\beta=0.041$ CW | 80.5 | 1.00 | 1.00 | 0.25 | 0.25 | 672 | 444 | 12 |
| $\beta=0.085$ CW | 80.5 | 1.00 | 1.00 | 0.25 | 0.25 | 2487 | 1469 | 94 |
| $\beta=0.285$ CW | 322 | 1.00 | 1.00 | 0.25 | 0.25 | 2812 | 1945 | 76 |
| $\beta=0.530$ CW | 322 | 1.00 | 1.00 | 0.25 | 0.25 | 4974 | 3462 | 148 |

* P_{avg} = P_g : peak power, P_{nom} : nominal power with beam and no disturbance

Signal Digitization and Control

RF Inputs

The LLRF controller digitizes the RF input signals using direct sampling and non-IQ sampling techniques. All filtering is done digitally in the FPGA. Removal of the bandpass filters and mixers improved long term phase drift and crosstalk compared to the previous design, which mixed down to a 50 MHz intermediate frequency. Each LLRF has two 4-channel ADCs. Each ADC samples three input channels and the RF reference for a total of six inputs per LLRF. In testing so far, a sample rate of 38.99 MHz was used. In this configuration, the LLRF controller samples 31 points on the RF signal to produce each I/Q pair. In upcoming testing, other sample frequencies will be tested in an effort to optimize the sample rate.

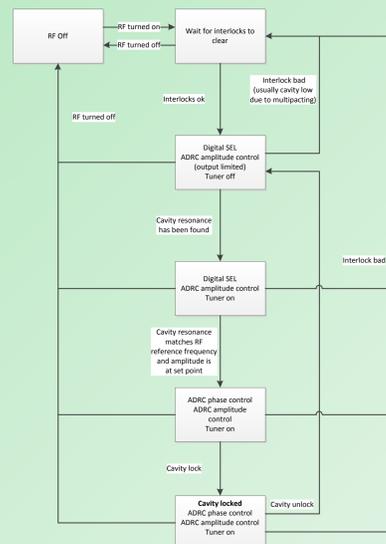
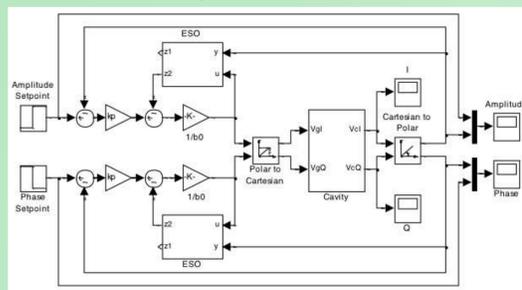
RF Output

Each LLRF controller has one output channel with an RF switch to select between two output DACs and filter frequencies. This allows a controller to be swapped between cavity types without it being necessary to swap the RF front-end board. There is no mixing on the RF output; the DAC produces the RF signal directly and the signal is passed through a pair of bandpass filters to remove the unwanted harmonics. For frequencies below 100 MHz, the first harmonic is used and higher harmonics are filtered out. For frequencies between 100 MHz and 300 MHz, the third harmonic is used. For higher frequencies, the fifth harmonic is used.

Startup and RF Control Modes

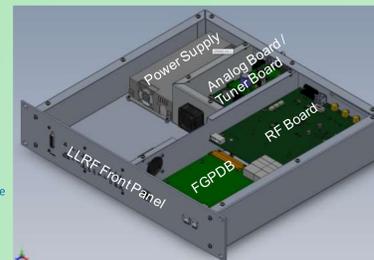
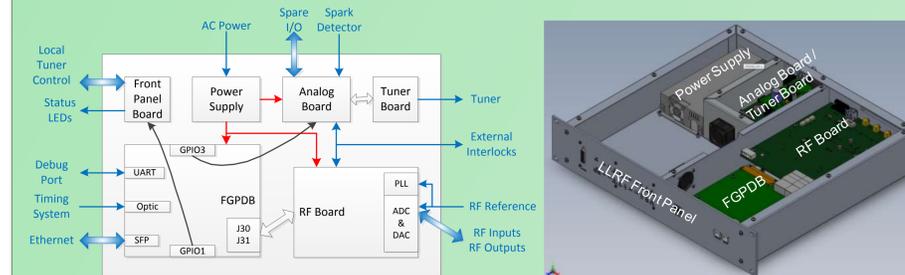
RF amplitude and phase are controlled with an Active Disturbance Rejection Control (ADRC) shown below. This control outperformed PID by approximately 4x in our steady state cavity testing and Eliminated overshoot and ringing on set-point changes. A digital self-excited loop has also been implemented to more easily turn on the cavities.

An automatic turn-on routine (shown on right) has been implemented to make things easier and more reliable for operators.



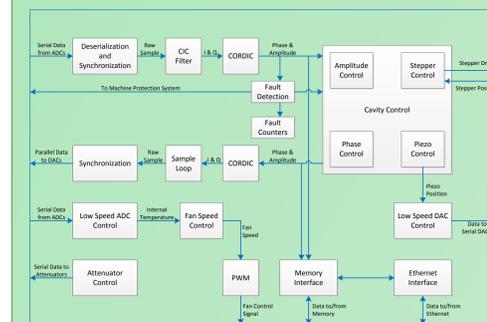
Modular Design

The FRIB LLRF Controller is packaged in a standard 2U chassis. The design is split onto five separate circuit boards to facilitate future upgrades and component reuse with other FRIB projects. Power is provided by a standard 1U server power supply.



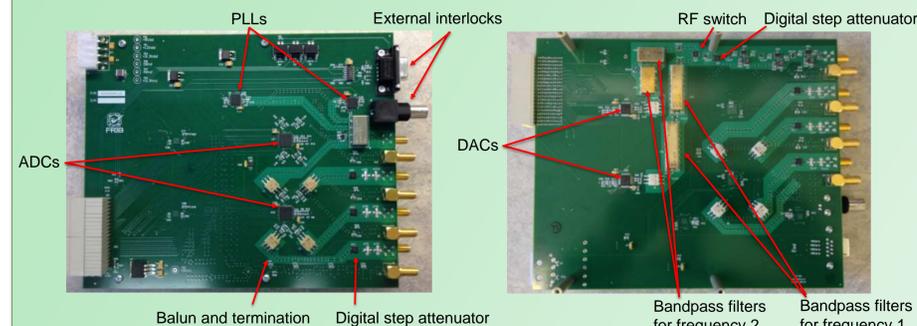
FPGA Board

The heart of the controller is the FRIB general purpose FPGA board. This board is based around a Xilinx Spartan-6 LX150T FPGA and is in a μ TCA form-factor. The LLRF Controller does not use μ TCA; this functionality is expected to be used in other devices used by the diagnostics group such as beam position monitors, beam current monitors, and other projects. The FPGA board connects to the RF front-end via two high-density connectors in the back and has Ethernet, SFP, and USB connections on the front.



RF Board

The RF Board is designed for direct, non-IQ sampling with minimal hardware on the RF inputs. The input signals pass through only a variable attenuation stage before being sampled at the ADC; all filtering is done digitally in the FPGA. Two output DACs are installed so that each LLRF can be switched between two frequencies with no hardware changes required. Almost all RF systems in FRIB will be at either 80.5 MHz or 322 MHz, so the standard configuration of the LLRF can select between those frequencies. A handful of systems run at other frequencies (20.125, 40.25, 120.74, or 161 MHz) so the controllers for those cavities will have different band pass filters installed on their outputs. The RF board also serves as the connection for the fast external interlocks, which directly disable the RF via an internal RF switch.



Modular Design

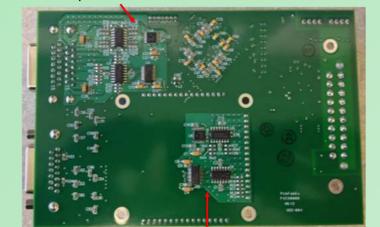
Analog Board

The analog board has eight analog inputs and eight analog outputs. Four of each are dedicated to the tuner driver board, which stacks on top of the analog board. The analog inputs are updated at up to 96 KSPS and outputs are updated at up to 1 MSPS. The others are provided as spare external I/O for future use. This board also includes the interface circuitry for optical spark detectors.

Optical spark detector interface



ADC and DAC for spare I/O



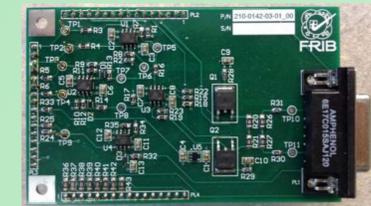
Spartan-3AN FPGA for ADC/DAC control

Serial link to FPGA board

ADC and DAC for tuner board

Tuner Board(s)

So far, two types of tuners are expected to be used in FRIB. The 80.5 MHz QWR cavities will use a piezo actuator and a stepper motor. The 322 MHz HWR cavities will use a pneumatic tuner. The modular design allows controllers to be quickly reconfigured for either cavity type by swapping the tuner board and will support future tuner upgrades.



Front Panel Board

The front panel of the module provides several status LEDs and a manual tuner control interface that will be useful during installation and commissioning.



Summary

The previous version of the LLRF controller has been successfully used on the NSCL reaccelerator for several years. While the old version does meet the FRIB control requirements, this version of the controller improves performance even more (especially long term drift and crosstalk) and adds the capability to operate at multiple frequencies without hardware changes.

The single circuit board of the older version is split into several separate boards to allow component sharing with other FRIB projects and to reduce the cost of potential future upgrades.