PAUL SCHERRER INSTITUT

FMC ADC/DAC Experiences for SwissFEL

LLRF

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Abstract

Modern digital LLRF control systems especially for pulsed machines demand multiple fast sampling and high precision data acquisition channels per RF station. The performance of such an acquisition channel is mainly limited by the used ADC/DAC type, clock distributor chips, and the layout and circuitry around those integrated circuits.

With FMC (FPGA Mezzanine Card), a standardized form factor was made available in 2008 and it solves an essential design question of each digital board designer: Where to place ADC/DAC and FPGA chips and how to connect them? Due to standardized digital interface, FMC provides an easy and well defined upgrade path for ADC / DAC mezzanines.

This poster shows how PSI solves the integration issues of 800 high speed and high precision data acquisition channels for SwissFEL using FMC mezzanines. It deals with special aspects the designer should take care for optimal use of the FMC standard. Finally performance figures for evaluated ADC/DAC FMC mezzanines are presented.

Figure 1: PSI's IFC1210 dual FMC carrier equipped with 2x ADC_3110 8 channel A/D

FMC cards tested with PSI carrier IFC1210

	Type	FMC	FPGA Chip	CPU Chip	Communication Infrastructure	Year
Carrier	**IFC_1210** *PSI / IOxOS*	2 slots	Virtex-6 LX130T IO voltage 2.5V	Freescale P2020 dual core 1.2 GHz	PCIe Gen2 + VME	2012

	Type	Channels	Converter Chip	Sample rate / Bits	Clock Chip	ENOB *)	Year
A/D	**FMC-516** *Curtiss Wright*	4 ch AC-s	4x ILSA216P	250 Msps/16 Bit	LMK02000	12.06 Bits FS	2012
A/D	**FMC108** *4dsp*	8 ch AC-s	4x ADS62P49	250 Msps/14 Bit	AD9510	11.60 Bits FS	2012
A/D	**ADC_3110** *IOxOS*	8 ch AC-s	4x ADS42LB69	250 Msps/16 Bit	LMK04906	11.92 Bits FS	2013
A/D	**FMC168** *4dsp*	8 ch AC-s	4x ADS42LB69	250 Msps/16 Bit	AD9517-3	TBD	4Q 2013
D/A	**FMC204** *4dsp*	4 ch AC-s	2x DAC5682z	1000 Msps / 16 bit	AD9517-3		2012
D/A	**FMC-250** *Innovative Integration*	2 ch DC-d 2 ch DC-s	1x AD9122 DAC 2x ISLA216P ADC	615 Msps/16 Bit 250 Msps/16 Bit	LMK04806B	11.53 Bits FS	2013

Table 1: List of FMC mezzanines tested with PSI carrier; *)ENOB measurement setup similar as in Figure 2

The time from pre-order and quotation phase of an FMC mezzanine until the first successful data acquisition test on a custom carrier depends much on the early availability and the quality of a mezzanine manual. An already pre-existing firmware example will help to speed-up the process. Overall one should calculate with 1-2 months for a full firmware integration into a custom carrier board. It is important to make performance measurements on the custom carrier due to influences towards mezzanine from power supply, chassis or environment.

ADC_3110: 8 ch / AC-single ended / 250 Msps / 16 bit performance measurement with PSI carrier

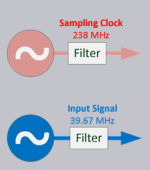

Figure 2: Clock setup

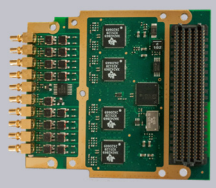

Figure 3: DUT ADC_3110

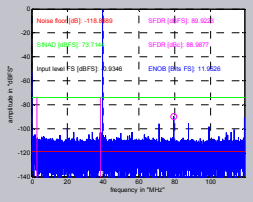

Figure 4: 64k aquisition and post processing

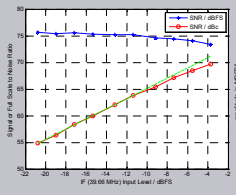

Figure 5: SNR vs. Input Signal Level

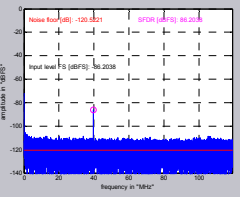

Figure 6: Crosstalk

Sampling Clock 238.0 MHz
Input Signal 39.67 MHz

- Average integrated noise floor **-75.5 dBFS**
- Average SFDR **90 dBFS**
- Average ENOB **11.92 Bits** (FS)
  - Min. 11.87 Bits (FS)
  - Max. 11.95 Bits (FS)
- Average SINAD **72.60 dBFS**
- Worst case channel isolation **85 dB**
- Worst case clock-to-ADC input isolation **77 dB**

FMC mezzanine: Considerations for design, evaluation/comparison and carrier board compatability checking

Signal Conditioning

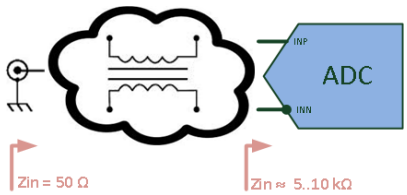

Figure 7: ADC input matching overview block diagram

The signal conditioning stage fulfills three main requirements and can occupy only limited space due to the small form factor of FMC.

It is used for mode conversion from single-ended to differential which is found on all high speed ADC's on input pins. A second task is the impedance matching from 50Ω to kΩ range. Finally it shall band limit the input signal according the application requirement.

All these tasks should be implemented ideally on one single PCB layer using passive elements such as **center-tap RF transformers** or **transmission line balun's** and **discrete filters**.

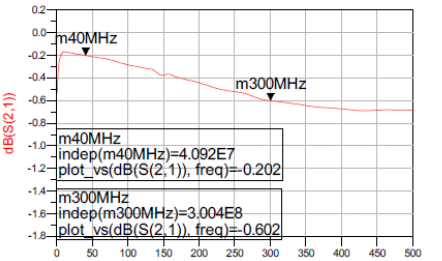

Figure 8: Simulation of an amplitude transfer function from 50Ω single ended input to ADC's internal high-Z buffers.

Clock

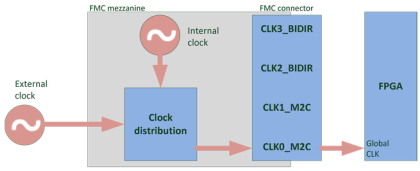

Figure 9 : FMC standard dedicated clock lines, example with external sampling clock towards FMC and FPGA.

For high speed and high quality A/D and D/A signal conversion applications the spectral purity of the sampling clock is essential. The obvious and proven way is **not** to use sampling clocks coming from carrier board. Instead of carrier clocks, local and clean on-board oscillators or external clocks are used.

Indepenent of the chosen clock source, a clock distributor circuit is required on the FMC board. Integrated circuits like the AD95xx or the LMK0xxxx families can handle several issues related to clock distribution such as availability to drive different levels and signal-ing standards such as LVDS or LVPECL.

Important checks for clocking capability:

- Is **CLK0_M2C** used and is connected to an FPGA global clock input on carrier board?
- Has the clock distributor debug output of its distribution clock for performance measurements?
- If not necessary, dont use clock distributor PLL and divider functionalities, instead provide **1:1 high quality external clock**.
- Band limit the clock input of FMC card

Power Supply

Voltage Supply	Allowable Voltage Range	No Pins	Max Amps	Tolerance	Max Capacitive Load
VADJ	0 – 3.3V	4	4	+/- 5%	1000 uF
VIO_B_M2C	0 – VADJ	2	1.15	+/- 5%	500 uF
VREF_A_M2C	0 – VADJ	1	1mA	+/- 2%	10 uF
VREF_B_M2C	0 – VIO_B_M2C	1	1mA	+/- 2%	10 uF
3P3VAUX	3.3V	1	20mA	+/- 5%	150 uF
3P3V	3.3V	4	3	+/- 5%	1000 uF
12P0V	12V	2	1	+/- 5%	1000 uF

Table 2: FMC standard power supply specification.

The final performance figures of A/D D/A cards depend strongly on the power supply of the carrier and the crate. Clean supplies for ADC or DAC chips in range of 1.8 .. 2.5V are typical required values.

Multistage power supply design with proper **filtering** is a must. Possible usable supplies are VADJ, 3P3V or 12P0V (1A limit), each with it's own disadvantage.

Conclusions

Using FMC as a connection in between fast AD/DA converters and an FPGA fulfills the requirements for flexibility and provides a well defined upgrade path.

Performance measures such as SFDR, SINAD or ENOB, on several ADC cards showed, that the FMC form factor does not limit ADC's dynamic performance compared to other form factors. The most critical issue for FMC is clean power supply design due to the limited space on the mezzanine itself. Finally one can only compare different FMC's on the same carrier board.

For LLRF operation the performance should be evaluat-ed within a real RF system environment. There other figures such as RF or beam stability give a better measure than above mentioned ADC's dynamic performance parameters measured in lab.