# Clock generation for the HIE-Isolde linac

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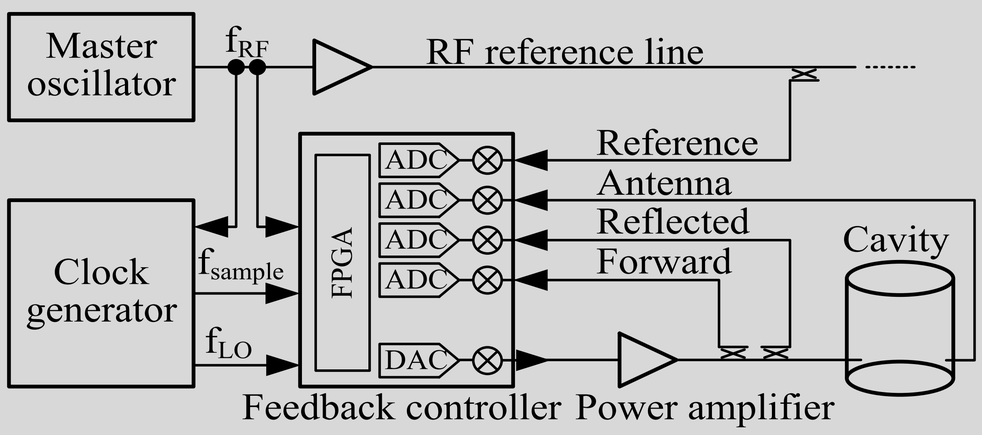
## ABSTRACT

*The HIE-ISOLDE project is a major upgrade of the ISOLDE and REX-ISOLDE (radioactive nuclear beams) facilities at CERN. The most significant improvement will come from replacing most of the existing REX accelerating structure by a 40 MV superconducting linac based on 32 independently phased superconducting quarter-wave resonators (cavities). The resonators operate at a frequency of 101.28 MHz and at a relatively high Q, providing an operational bandwidth of only a couple of Hertz.*

*The LLRF system is designed to be fully digital, with direct RF sampling and digital quadrature demodulation, as well as direct RF generation by a fast DAC. The field in the superconducting resonator needs to be stabilized with an accuracy of 0.2°/0.2%. This imposes strict requirements on the system reference clock quality in terms of stability and aperture jitter. A low phase-noise clock generator locked to a GPS disciplined reference oscillator has been developed. This poster presents the design and performance of the clock generator as well as achieved results with the direct RF sampling and generation.*

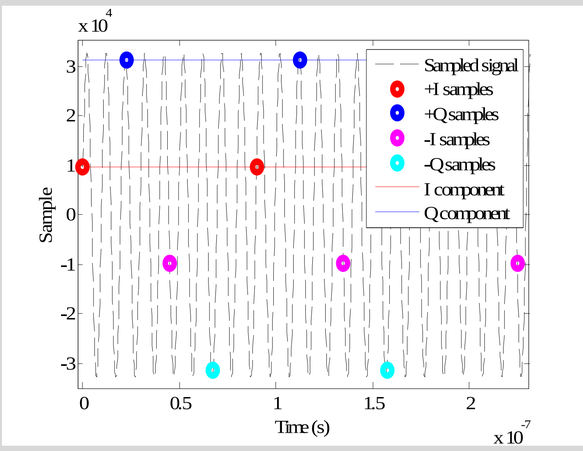
## HIE-Isolde low level RF system

The low level RF system is fully digital, using LHC-style VME form factor with custom LLRF backplane.
The HIE-Isolde is a stand alone machine without particle transfer from, or to other accelerators. It has a single frequency RF system, working at 101.28 MHz.
The RF clock quality is crucial for machine operation. Both long time stability, low frequency drifts, as well as fast phase noise are important.

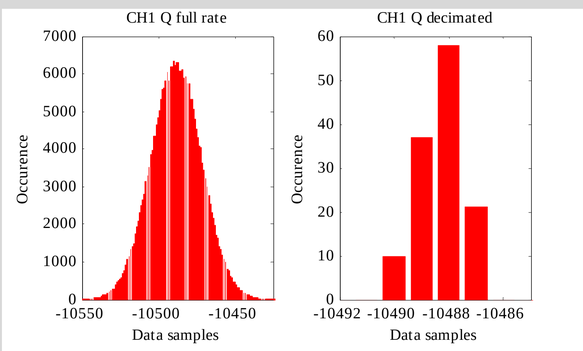



## Direct RF sampling and Quadrature demodulation

The direct digital demodulation is achieved by sampling the input signal at times corresponding to multiples of a 90° phase advance. The quadrature sampling will be achieved every time when the sampling frequency and the RF frequency are locked in a rational ratio defined as $f_{sample} = 4*f_{RF}/(n+1)$.

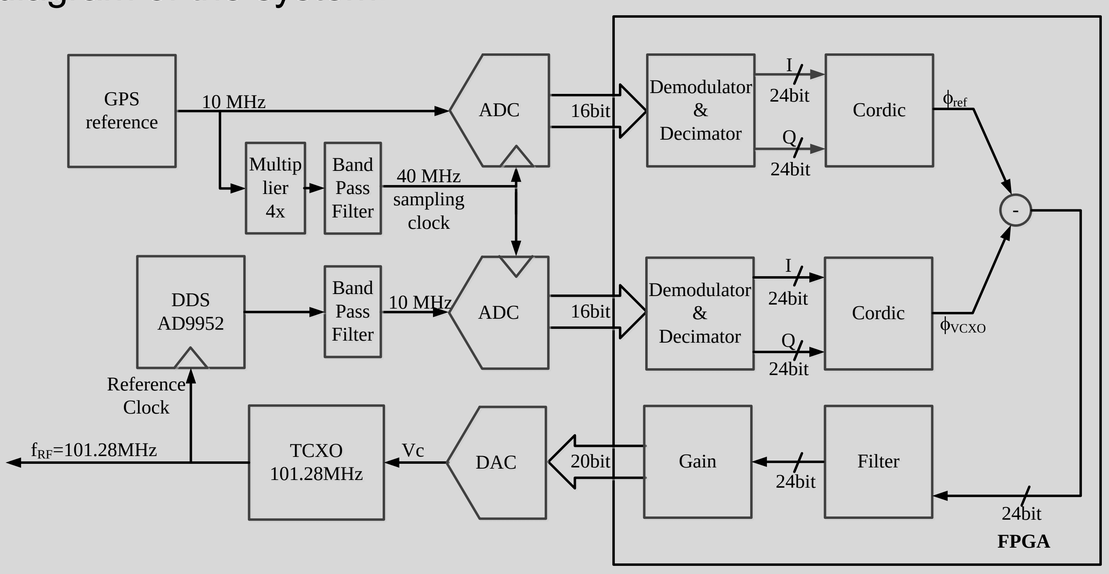



HIE-Isolde RF frequency 101.28 MHz lays well within analogue bandwidth of the modern fast ADCs, therefore direct RF sampling is possible. Moreover, the feedback loop bandwidth is limited to few tens of Hz, allowing us also to undersample the RF signal.
The sampling clock needs to have a very well controlled phase noise. The total aperture jitter must be kept below 2.5 ps to achieve an ENOB of 9 bits, with decimation obtaining >14 bit "noise free" data for the feedback controller.
For HIE Isolde we have chosen n = 36, leading to $f_{sample}$ = 10 949 189 Hz. The sampling clock is prepared by a set of ECL dividers without further VCXO-PLL filtering. The figure shows acquired data quality before and after decimation.




## Master RF Clock generation

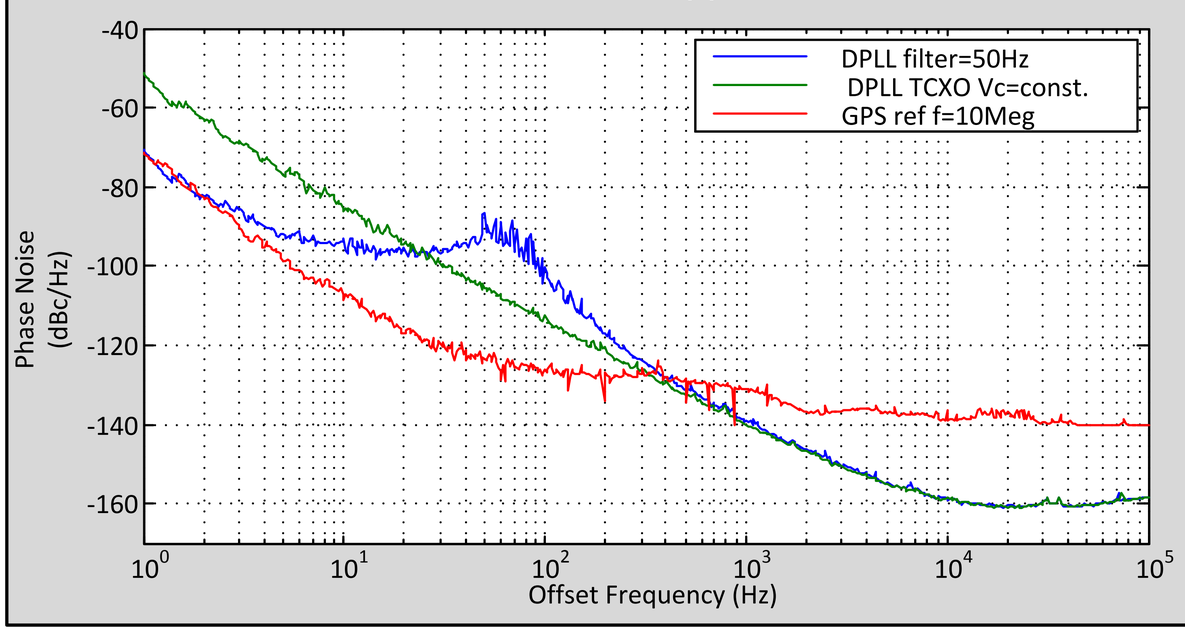
The master RF clock is generated by a low phase noise Axtal 101.28 MHZ VCXO phase locked to an Oscilloquartz 10 MHz GPS disciplined reference oscillator.
The clock generator and its PLL was implemented as fully digital, into existing llrf hardware. The goal was to have a handle to optimize the PLL loop filter response to match the phase noise spectrum of the VCXO and the GPS. Figure below shows a block diagram of the system.




The 101.28 MHz VCXO signal is divided down to 10 MHz by an external discrete DDS chip. This signal is sampled by a 16 bit ADC and digitally quadrature demodulated. The GPS reference 10 MHz signal is also sampled and demodulated by a second ADC.
Phase of both signals is processed by a programmable digital loop filter. Phase correction control TCXO frequency by 20bit DAC.

## First results

The plot shows phase noise spectra of the system. Red trace corresponds to the GPS standard (scaled to 101.28 MHz), green trace the standalone VCXO. The blue trace is measurement of the master RF generator output. The PLL filter frequency response was not optimized yet, the excess of phase noise between 10 Hz and 200 Hz wrt. the bare VCXO will be suppressed.



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