THE STUDY OF DIGITAL LLRF CONTROL SYSTEM FOR CSNS LINAC

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Abstract
China spallation neutron source(CSNS) is located in Dongguan city in Guangdong province. The accelerators of CSNS mainly consist of an H-linac which accelerates the H- beam energy to 81 MeV and a rapid cycling synchrotron (RCS) accelerator which accelerates the proton beam to a high current pulse and then accelerates it to 1.6 GeV. The infrastructure and equipment manufacture are now in progress. The RF system for the 81 MeV Linac requires 9 units of RF power sources: two 4616 tubes power RFQ, 4 klystrons power DTLs, and 3 solid state amplifiers power two bunchers and one deboocher. Each unit has one independent digital low level RF (LLRF) control system which is used to stabilize the amplitude and phase of the RF accelerating field along the linac, and to minimize beam loss. Now the LLRF prototype has been developed, the test results show that the fluctuation range of amplitude and phase satisfy our requirements. This paper will address the layout of CSNS linac LLRF system, the related hardware designs and the algorithm implementations.

INTRODUCTION

The RF power systems of CSNS 81 MeV Linac operate at RF frequency 324MHz, repetition rate 25 pps, RF pulse width 650 µs, and duty cycle 1.625%. Eight power sources are used throughout the CSNS linac: two 4616 tubes power RFQ, four klystrons power DTLs, and three solid state amplifiers power two bunchers and one deboocher. The overview of the RF system configuration is showed in Fig. 1. Identical FPGA-based digital LLRF control systems are used for all cavities throughout the linac. In order to increase the speed of digital signal processing, we choose the LO frequency of the LLRF control system which is used to stabilize the amplitude and phase of the RF accelerating field along the linac, and to minimize beam loss. Now the LLRF prototype has been developed, the test results show that the fluctuation range of amplitude and phase satisfy our requirements.

SCHEME OF THE LLRF CONTROL SYSTEM

All the analog units including the analog moudle (AM) and clock distribution module (CDM) are put into a temperature stabilizing chamber. The digital controller module (DCM) implements the digital IQ de-modulation, PI controller and the NCO module,etc. It includes 4 channel ADCs, 4 channel DACs, one Altera strix II FPGA and two TI C6000 DSPs. In this module, the cavity detuning frequency and Q value are also automatically monitored by sampling the cavity field trailing delay waveform just after RF pulse shutoff. The high power protection module (HPM) is mainly in charge of the precise power measurement and VSWR protection along the power transfer system. The basic architecture of the LLRF system is showed in Fig. 2.

THE 324MHZ REFERENCE LINE AND 360MHZ LO MODULE

The reference line is placed in sub-tunnel of CSNS Linac, the phase stable cable is wrapped in a constant temperature water jacket, the variation range of temperature will be limited into ± 0.1°, each LLRF station will get the reference signal through a Narda 3000 coupler. The source of LO module is also from the reference line through coupler, a low noise amplifier fans out nigh 360MHz LO signals to each LLRF station.
HARDWARE AND THE SOFTWARE
ALGORITHM OF LLRF

The Design of Analog Module (AM) and Clock Distribution Module (CDM)

The AM and CDM are put into a temperature stabilizing chamber to reduce the effects from the temperature variation, the range of the temperature variation can remain ± 0.1 ℃, the picture of the temperature stabilizing chamber is showed in Fig. 3. The AM is comprised of four down conversion channels and two up conversion channels, all these channels are designed to be symmetrical layout. The CDM outputs different frequency clocks used by the digital components, such as ADCs, DACs and FPGA, etc, the input of this module comes from the signal mixed by reference and LO.

Figure 3: the temperature stabilizing chamber

The Digital Controller Module (DCM) hardware and Control Algorithm

The DCM hardware consists of a motherboard and two daughterboards, one of the daughterboards owns four 14bit, 144MHz ADC channels, and the other one owns four 14bit, 144MHz DAC channels. The core devices in the motherboard are one Altera stratax II FPGA and two TI C6000 DSPs, the primary control logic is implemented in the high-speed and high-density FPGA, the DSPs is mainly responsible for the communication with IPC through Ethernet and some coefficient calculations.

This structure can reduce the logic elements usage and simplify the floating point arithmetic, also make the Ethernet communication easy to realize. The picture of the digital module is shown in Fig. 4.

Figure 4: the motherboard and two daughterboards of the DCM

Two clocks are provided into the FPGA of DCM, the 144MHz clock is from the ADC output associated with the digital datas. In order to ensure the 144MHz clock consistent with the received data window, a PLL is necessary to deskew it. The other 36MHz clock is directly sent into the clock pin of FPGA, this clock frames I, Q, -I, -Q data stream to keep the phase of the RF driving signal constant. A pure digital signal processing flow is blocked out (see Fig. 5).

Figure 5: The digital signal processing flow in FPGA
The FPGA control logics are implemented with Verilog Hardware Description Language. The PI feedback control and feedforward table are adopted to satisfy the requirements of cavity field amplitude and phase less than $\pm 1\%$ and $\pm 1^\circ$. Except for the primary signal processing algorithms including I/Q demodulation, auto-offset correction, input rotation matrix and PI controller, etc, some new experiments have been added to the signal processing flow.

(1) Auto-Tuning for Cavity Warm-Up

When the RF power feed into cavity, the temperature of cavity will rise gradually, so the cavity resonant frequency will change associated with the temperature rising. In order to make the cavity warm up quickly, an auto-tuning function has been applied into our LLRF control system.

The cavity detuning frequency is obtained through sampling the field decay proceeding. The method is the same as I/Q sampling. When the $I, Q, -I, -Q$ sequence is gotten, we can calculate the amplitude and phase of decay field from it. The detuning frequency can be achieved based on the phase variation curve during the cavity field decay processing. The expression of detuning frequency is given by $\Delta f = \frac{d\theta}{2\pi \times dt}$, $\theta$ is the cavity field phase which is given by $\theta = \arctan\left(\frac{Q}{I}\right)$.

This method has been verified at a 352.2MHz RFQ accelerator through a FPGA development board.

The actual phase curve showed in Fig. 6 with blue dot line is directly acquired from the rude I/Q, the red solid line is fitted out by the way of least square method. According to the expression above, the detuning frequency of RFQ is 17.061KHz.

![Figure 6: The phase curve during cavity field decay](image)

Figure 6: The phase curve during cavity field decay

When the detuning frequency is gotten, a numerical controlled oscillator (NCO) IP core is adopted to complete the auto-tuning, when this function starts to work, the frequency of RF driving signal is always consistent with the cavity natural frequency, the setting time of cavity field reduces greatly. The proceeding of sweeping frequency was recorded by spectrum analyzer during function commissioning.

(2) The Cavity Auto-Ageing process

When the accelerating cavity begin to feed RF power, the ageing process is necessary to protect it against arc damage. This process maybe take a long time, so we designed the auto-ageing method to do it. This method needs to cooperate with the high power protection module. First, we divide the RF amplitude into ten levels, the power will be increased step by step from the first level, if arc counts exceed the threshold during a setting time, the power will decease one level, if no arc is detected during this time, the power will increase one level, the algorithm flowchart is showed in Fig. 8.

![Figure 8: the cavity auto-ageing algorithm flowchart](image)

Figure 8: the cavity auto-ageing algorithm flowchart
Introduction of High Power Protection Module (HPM)

The RF power detection and VSWR protection are achieved in HPM, the RF signals come from different couplers distributed in the power transfer line, HPM has the same motherboard with DCM, only one daughterboard owns eight channel ADCs, a logarithmic Detector is installed in the front end of each channel to send DC pulse into ADC. The detector is designed by ourself, the rising edge can reach 60ns, the performance absolutely meets our demand. The VSWR protection logic is realized in FPGA. All the detected RF power values are sent to IPC through Ethernet, and display in real-time on screen.

Figure 10: The fluctuation range of cavity field phase

CONCLUSION

The design of CSNS Linac digital LLRF control system is complete, the initial commissioning results indicate that the performance met our requirements of amplitude ± 1% and ± 1°. Next, we will begin to installation, more performance measures will be reported in our future publications.

REFERENCES