The Study of Digital LLRF Control System for CSNS LINAC

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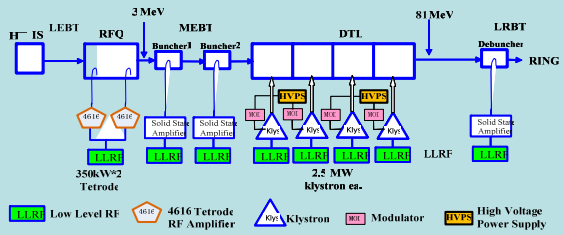
Abstract

China spallation neutron source(CSNS) is located in Dongguan city in Guangdong province. The accelerators of CSNS mainly consist of an H- linac which accelerates the H- beam energy to 81 MeV and a rapid cycling synchrotron (RCS) accelerator which accumulates the proton beam to a high current pulse and then accelerates it to 1.6 GeV. The infrastructure and equipment manufacture are now in progress. The RF system for the 81 MeV Linac requires 9 units of RF power sources: two 4616 tubes power RFQ, 4 klystrons power DTLs, and 3 solid state amplifiers power two bunchers and one debuncher. Each unit has one independent digital low level RF (LLRF) control system which is used to stabilize the amplitude and phase of the RF accelerating field along the linac, and to minimize beam loss. Now the LLRF prototype has been developed, the test results show that the fluctuation ranges of amplitude and phase satisfy our requirements. This paper will address the layout of CSNS linac LLRF control system, the related hardware designs and the algorithm implementations.

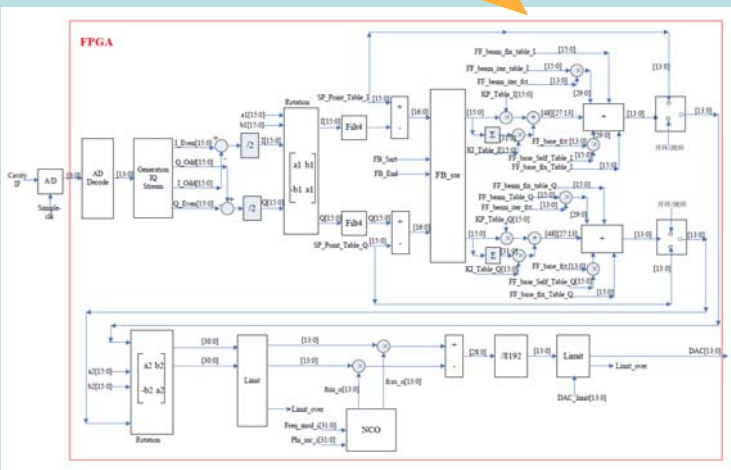
INTRODUCTION

The RF power systems of CSNS 81 MeV Linac operate at RF frequency 324MHz, repetition rate 25 pps, RF pulse width 650 μs, and duty cycle 1.625%. Identical FPGA-based digital LLRF control systems are used for all cavities throughout the linac. In order to increase the speed of digital signal processing, we choose the LO frequency of the LLRF system to be 360MHz, the IF frequency 36MHz, the ADC sample clock frequency and FPGA signal processing speed can be set to 144MHz, the key controller with all-digital implementation has successfully achieved lower system latency and wider control bandwidth.



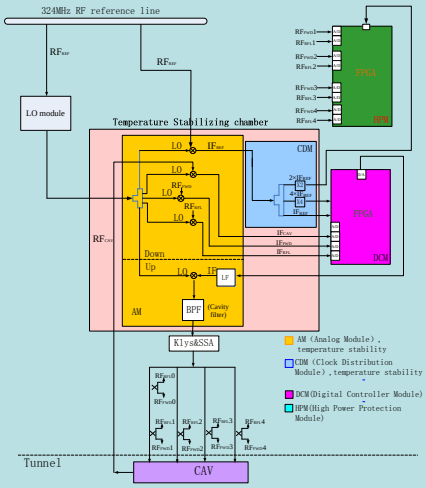
The DCM hardware consists of a motherboard and two daughterboards, one of the daughterboards owns four 14bit, 144MHz ADCs, and the other one owns four 14bit, 144MHz DACs. The core devices in the motherboard are one Altera straix II FPGA and two TI C6000 DSPs, the primary control logic is implemented in the high-speed and high-density FPGA, the DSPs is mainly responsible for the communication with IPC through Ethernet and some coefficient calculations. This structure can reduce the logic elements usage and simplify the floating point arithmetic, also make the Ethernet communication easy to realize.

The FPGA control logics are implemented with Verilog Hardware Description Language. The PI feedback control and feedforward table are adopted to satisfy the requirements of cavity field amplitude and phase less than ±1% and ±1°.



SCHEME OF THE LLRF CONTROL SYSTEM

All the analog units including the analog moudle (AM) and clock distribution module (CDM) are put into a temperature stabilizing chamber. The digital controller module (DCM) implements the digital IQ de-modulation, PI controller and the NCO module,etc. It includes 4 channel ADCs, 4 channel DACs, one Altera straix II FPGA and two TI C6000 DSPs. In this module, the cavity detuning frequency and Q value are also automatically monitored by sampling the cavity field trailing delay waveform just after RF pulse shutoff. The high power protection module (HPM) is mainly in charge of the precise power measurement and VSWR protection along the power transfer system.



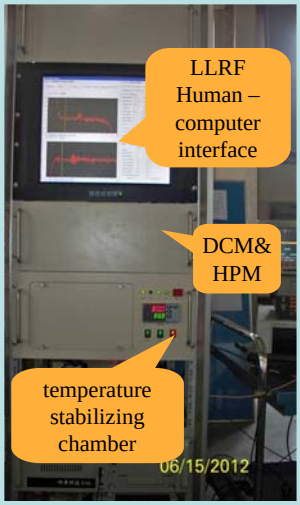


Figure: The Basic Architecture of the CSNS Linac Digital LLRF Control System

Figure: The cabinet Layout of the Digital LLRF Control System

PERFORMANCE

The assemble of the prototype was finished in May, 2012, the commissioning was done with the available 352.2MHz RFQ accelerator. The test results satisfied the design requirements, The delay of LLRF control system is 676ns, including 348ns consumed by digital signal processing. The control precision of cavity field amplitude and phase is less than ±0.4% and ±0.6°,respectively, with the beam pulse width 50us and the beam loading 40mA.

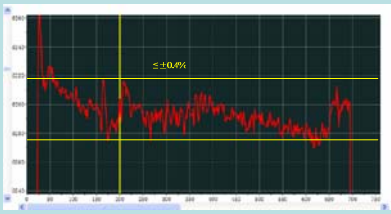


Figure: The fluctuation range of cavity field amplitude

Figure: The fluctuation range of cavity field phase

CONCLUSION

The design of CSNS Linac digital LLRF control system is complete, the initial commissioning results indicate that the performance met our requirements of amplitude ±1% and phase ±1°. Next, we will begin to installation, more performance measures will be reported in our future publications.

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