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PCIe and VME low latency data transfer in scalable LLRF systems

LLRF

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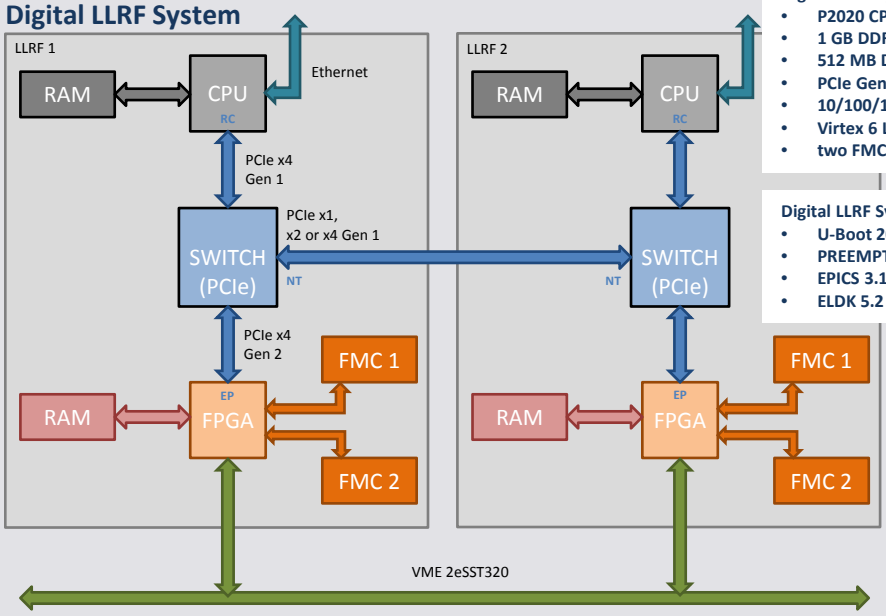
Abstract

The design of a digital LLRF system for SwissFEL with repetition rate of 100 Hz and distributed ADC channels demands for a concept with high-speed and low latency data transfer links and a variable number of connected boards. The modular unit of such LLRF system is a VME board with PCI express based infrastructure between FPGA, CPU and external PCI express devices. Two FMC mezzanine slots are available for connection of ADC/DAC cards. Since feedback algorithms shall run on a central carrier board, where the DAC mezzanine card is located, the data transfer of all required ADC's has to be implemented in a flexible manner with lowest possible latency. Performance figures for latency values for different link types (VME bus, PCI express) as a function of data packet size are presented.

Digital LLRF System



Digital LLRF System Hardware
- P2020 CPU 1.2 GHz
- 1 GB DDR3 RAM (CPU)
- 512 MB DDR3 RAM (FPGA)
- PCIe Gen 2 switch PES32NT24AG2
- 10/100/1000 Base T Ethernet
- Virtex 6 LX130T FPGA
- two FMC HPC slots

Digital LLRF System Software
- U-Boot 2011.12
- PREEMPT_RT Linux 3.6.11.5-rt37
- EPICS 3.14.12
- ELDK 5.2 (cross development tool)

Figure 1 Digital LLRF system with two boards (IOxOS IFC1210)

Digital LLRF System Requirement and Implementation

Requirements:
1. The board should be usable with old and existing VME crates
2. CPU with low power consumption and adequate performance
3. Fast data transfer between boards, variable number of connected boards, good software support
4. Generic solution to connect ADC and DAC cards

Implementation:
1. 6U VME64x board
2. P2020, typically with 8W power consumption
3. PCI express switch and connector on board
4. FMC slots and FPGA on board

Network on Chip, TOSCA-II switch

One of the key components of the digital LLRF system is the IOxOS TOSCA-II switch inside the FPGA. This switch is a full mesh switch connecting together different resources like VME Bus, PCI express, DDR3 memory and FMC slots. Every resource connected to the switch can act as Master or Slave.
Due to point-to-point connections the bandwidth is not shared and can be specifically defined by the Master and Slave implementation. Another advantage of a point-to-point connection is the control of the latency, because it is no more related to the media sharing.

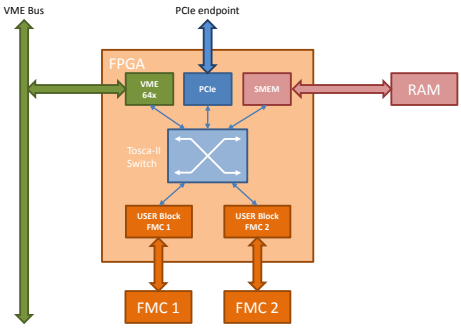


Figure 2 Tosca-II switch

Every connection is handled independently and therefore simultaneous transactions are possible. An individual connection of switch and resource reach 1.6 Gbyte/s. The switch can handle PCI express x8 Gen 1 or PCI express x4 Gen 2. By default the switch supports DMA data packet transactions up to 1Kbyte.

Measurement setup

The goal of the measurements is to find out how fast the different transactions from VME bus and PCI express are. Two performance figures are of interest: The achievable data rate and the latency of the transaction. For all measurements a counter in the USER block of the FPGA was used. The counter was clocked with 100 MHz. A program in user space controlled the hardware counter for the measurements.
Tested transactions:
1. Reading data from FPGA RAM (local LLRF system) by PCIe to CPU RAM
2. Reading data from FPGA RAM (neighbor LLRF system) by VME bus to CPU RAM
3. Reading data from FPGA RAM (neighbor LLRF system) by PCIe to CPU RAM

Measurement Results

The figure below shows the achieved data rates of the SwissFEL digital LLRF system. Transactions between two LLRF systems reached 180 Mbyte/s by VME and 420 Mbyte/s by PCIe x2 Gen 1.

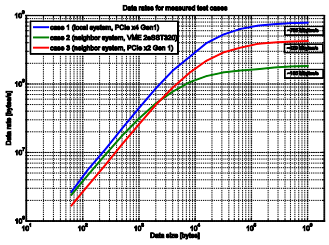


Figure 3 Data rates

An interesting point of figure 3 is the crossing between VME bus and PCIe bus data rates. This happens if the data size is approximately 2 Kbyte. Below this data size the VME 2eSST320 has a faster data rate compared to PCIe x2 Gen 1.

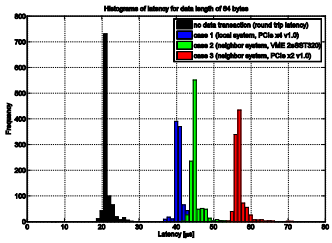


Figure 4 Latencies

Figure 4 shows histograms for the three test cases. For every histogram 1000 transactions were executed. The transferred data size was 64 bytes. The black histogram shows the round trip latency (hw counter start → PCIe → application → PCIe → hw counter stop) of the system if no data transaction was executed. Sometimes the transaction time is very high. Figure 4 does not show these rare latencies. Mostly 3 or 4 of 1000 transactions have latencies of approximately 800 µs.

Future improvements

The current digital LLRF system has possible improvement points:
- Connection between neighbor cards should be PCIe Gen 2
- CPU with PCIe Gen 2
- Fix latency issue

Conclusion

Digital LLRF system for the SwissFEL is ready to fulfill the required flexibility of ADC/DAC channels and scalability of modular units. The currently reached data rates and latencies allow the use of the system with 100 Hz repetition rate. However the system has feasible improvement points.

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