PAUL SCHERRER INSTITUT

# SwissFEL C-band LLRF Prototype System

## LLRF

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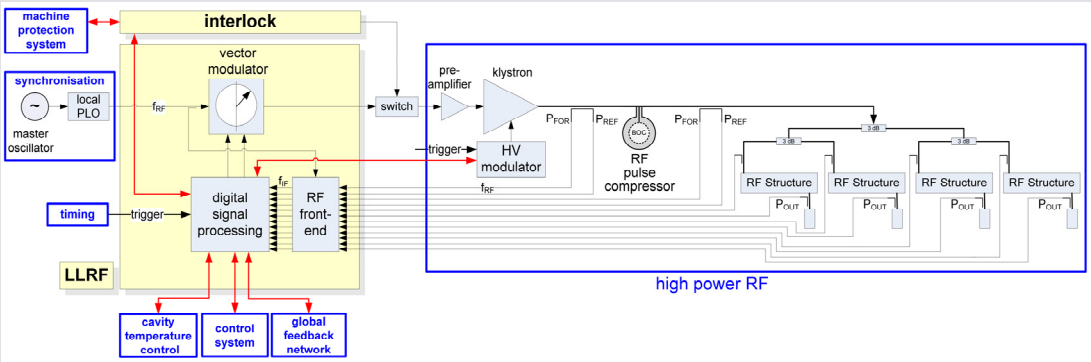
## Abstract

A first prototype of the C-band LLRF system for the SwissFEL accelerator project was developed at PSI. It handles up to 16 RF channels converting 5.712 GHz RF pulses down to 40 MHz IF and includes one baseband vector modulator.
The LLRF system is based on a first version of an analog C-band front end and a newly developed FMC based digital backend with 250Msps/16bit ADC readout channels. The repetition rate of the pulsed system is 100 Hz and fully integrated into PSI's EPICS control system.
The complete prototype system was tested in the laboratory and installed into the SwissFEL C-band test facility.


## SwissFEL C-Band Station




Topology of a C-band station

## SwissFEL Design Parameters

| | |
|---|---|
| Charge per bunch | 200 pC |
| Beam energy for 1 Å | 5.8 GeV |
| Peak current at undulator | 2.7 kA |
| Bunch length | 25 fs (rms) |
| Bunch compression factor | 125 |
| Number of bunches | 2 |
| Bunch spacing | 28 ns |

## Requirements for C-band Station

| | |
|---|---|
| C-band frequency: | 5.712 GHz |
| Repetition rate | 100 Hz |
| RF pulse length | 0.02-5 us |
| Amplitude stability of C-band in LINAC | 1.8e-4 rel. |
| Phase stability of C-band in LINAC | 0.036° |
| Number of channels per RF station | 24 |
| Channel to channel drift | 0.1° / day |

## Results from LLRF Prototype System

| | |
|---|---|
| Pulse to pulse phase jitter (only LLRF system, 40 pulses, intra pulse average) | 0.036° |
| Pulse to pulse amplitude jitter | 4e-4 rel. |
| Phase readback error | < 0.1° |
| Amplitude readback error | < 0.1% |
| Number of channels | 16 |

### Carrier Card IFC1210

- Processor: Freescale P2020 (dual core 1.2 GHz)
  - 1 Gbyte DDR3 RAM
  - 2x Gigabit Ethernet
- PREEMPT_RT Linux Kernel 3.6.11.5-rt37
- RT user applications & EPICS server
- Fast data processing on FPGA Virtex-6 LX130T
  - 512 MByte DDR3 RAM, 3.2 Gbyte/s
- Scalable system (PCIe, VME64x)
- Fast links over rear transition modules (FPGA serial transceiver or PCIe)

### LO & Clock Generation

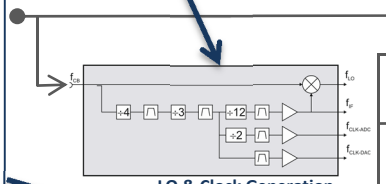
- input from MO: 5712 MHz
- LO output: 5752.667 MHz
- ADC/DAC clock: 238 MHz
- optional clock: 476 MHz
- IF reference : 39.667 MHz

### Power Supply

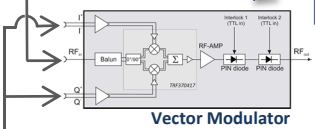
- RF front end: switched AC/DC power supply
- ADC/DAC: switched power supply in VME crate

### Vector Modulator

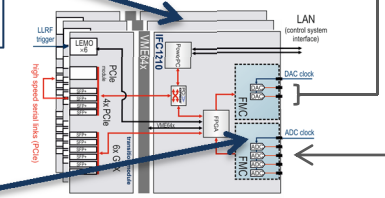
- Based on a single modulator chip
- 50 ohm pseudo differential, DC-coupled baseband inputs
- Redundant PIN switches for interlock capability
- 20 MHz bandwidth for 180°phase jump



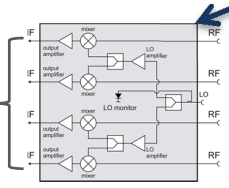
LO & Clock Generation



Vector Modulator



Digital Processing



Down Converter

### Down Converter

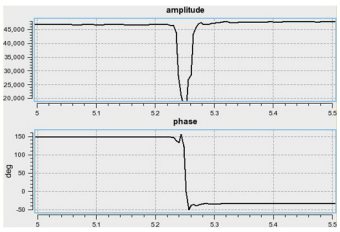
- 16 channel in 2 unit 19'' box
- IF frequency: 39.667 MHz
- Bandwidth: 48 MHz
- Channel to channel isolation: 60 dB

### ADC/DAC

- ADC/DAC piggyback: FMC standard, HPC
- ADC: 4 Channel 16 Bit / 250 Msps FMC-516 Curtiss Wright
- DAC: pseudo-differential 16 bit / 250 Msps FMC-250 Innovative Integration
- Switched power supply in VME crate

### Signal Processing

- 1/6 nonIQ-algorithm (bandwidth: 34 MHz)
- Reference tracking for LO drift compensation
- Raw data / IQ-data/ phase, amplitude

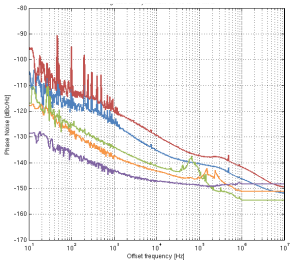



180° phase jump generated & measured with LLRF system

## Phase Noise Measurements

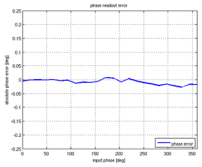
- ADC clk: 120 fs @ $f_{ADC}$ / 0.01° (absolute)
- DAC clk: 97 fs @ $f_{DAC}$ / 0.016° (absolute)
- LO: ~ 3.6 fs @ $f_{LO}$ / 0.008° (added)
- VM: ~ 2.7 fs @ $f_c$ / 0.006° (added)
- RX: ~ <5 fs @ $f_c$ / 0.01° (added)

(offset frequency range: 10 Hz – 10 MHz)

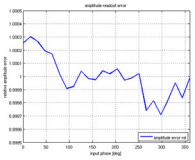


## Linearity

Verification* of absolute phase and amplitude measurement accuracy of the LLRF system.
* measured with vector network analyzer



absolute phase readback error: < 0.1 °



absolute amplitude readback error: < 0.1%

26.09.2013