

Abstract

A 4GSa/s signal processing system has been developed for proof of concept transverse intra-bunch closed loop feedback control studies at the CERN SPS. This system contains a beam pickup, analog front end receiver, signal processor, back end driver, power amplifiers and kicker structure. The main signal processing function is performed digitally, using very fast (4GSa/s) data converters to bring the system signals into and out of the digital domain. The digital signal processing function itself is implemented in an FPGA allowing for maximum speed and flexibility, utilizing the FPGA's DSP-specific resources to implement FIR based control filters. In addition to the feedback function, an excitation feature was added allowing the system to run as a bursted arbitrary waveform generator. These operating modes are complemented with a set of diagnostics, which includes a programmable snapshot memory for recording of input data. This system has served well in proof of concept studies at the SPS and will be expanded with further capabilities and features. The signal processor utilizes commercial silicon and is a modular design consisting of commercial and custom components. This approach allowed for a rapidly-developed prototype to be delivered in a short time with very limited resources. Though designed for a specific purpose, its topology and FPGA implementation allow it to be used for general-purpose applications beyond that of its original design.

Introduction and Background

Introduction:

- High Intensity LHC beam is known to cause transverse instabilities driven by the electron cloud effect and Transverse Mode Coupled Instabilities (TMCI) in the SPS.
- A research and development effort has been undertaken between CERN and SLAC under the auspices of the US LHC Accelerator Research Program (LARP) to develop techniques for controlling these using feedback.
- Goal: Achieve feedback control of intra-bunch instabilities
- The result of this work was the development of a high-speed (4GSa/s) feedback processor [1-3].

A Modular & Flexible Design:

FPGA-Based:

- All Signal processing is performed in a large, fast FPGA [4] contained on a motherboard with high-density, high-speed I/O connectors.
- FPGA design is done in VHDL, using the Xilinx ISE tool suite for compilation and Modelsim PE for simulation. All DSP blocks use Xilinx corgen library structures.

Modular:

- The ADC [5] and DAC [6] are implemented as daughterboards that plug into the FPGA motherboard [7].

Operating Modes:

The system can run in two modes:

- Feedback: ADC → FIR → DAC
- Excitation: A memory feeds the DAC, making the system a fast arbitrary waveform generator

Both modes run triggered (external triggers input) and synchronous (external accelerator system clock input)

Diagnostics:

- Contains an ADC snapshot memory, capable of conditionally storing up to 65000 turns of pre-processed bunch data

Communication:

- USB 2.0 port (Cypress Semi EZ-USB)
- Expandable to Ethernet (using Virtex-6 MAC core)

Packaging:

- The processor fits into a 7U, 19 inch wide, 22 inch deep rack-mount chassis
- Signal I/O, AC mains power and USB for comms with host computer.

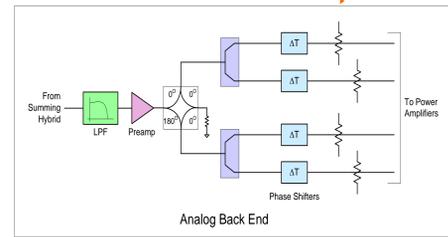
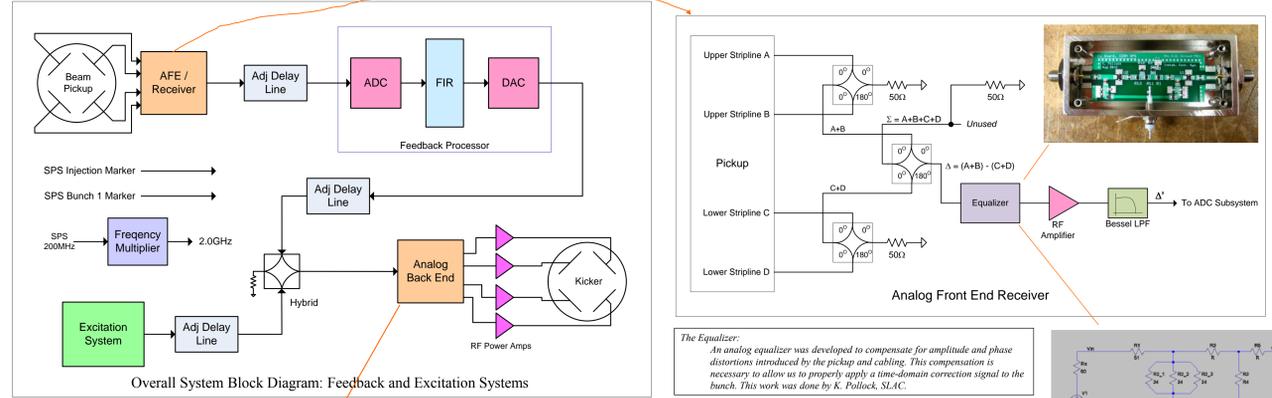
Summary:

This processor, along with its Analog Front- and Back-Ends forms a flexible signal processing system. Although developed for Transverse Feedback applications, it is expandable and can be tailored to other accelerator systems (longitudinal feedback, bunch-by-bunch current monitor, LLRF, etc.).

References

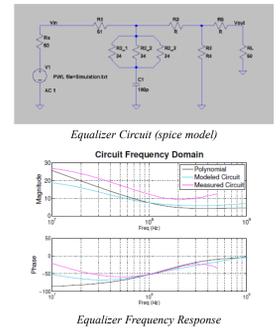
- [1] J. Dusatko et al., "A 4 GSa/s Instability Feedback Processing System for Intra-Bunch Instabilities", IPAC2013, Shanghai, China, May 2013, WEPME059.
- [2] J. Dusatko et al., "The Hardware Implementation of the CERN Ultrafast Feedback Processor Demonstrator", IBIC2013, Oxford, UK, September 2013, MOPC28.
- [3] J. Fox et al., "A 4 GS/s Feedback Processing System for Control of Intra-Bunch Instabilities", IBIC2013, Oxford, UK, September 2013, TUBL2.
- [4] FPGA: Xilinx Virtex-6 XC6VHX565T www.xilinx.com
- [5] ADC: Maxim Semi MAX1069 www.maxim-ic.com
- [6] DAC: Maxim Semi MAX19693 www.maxim-ic.com
- [7] FPGA Motherboard: Dini Group, Inc. DNMEG_V6HXT www.dinigroup.com

Full System Overview

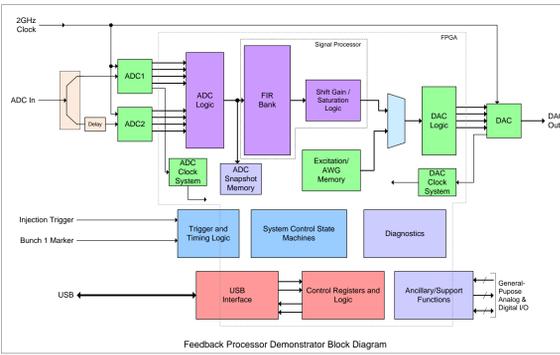


System Overview:

- We have built a single-bunch, ultrafast high bandwidth transverse feedback demonstrator system.
- This feedback system is essentially a high bandwidth re-configurable digital signal processing channel with an input ADC and output DAC capable of sampling at 4GSa/s. An FPGA implements the signal processor and the current design contains a 16-tap FIR bandpass filter.
- The feedback system acquires 16 samples or slices across one bunch, and outputs 16 correction samples, both at the 4GSa/s rate.
- For our measurements in the SPS, we use Feedback and Excitation systems together, which allow us to drive the bunch into instability and then correct with feedback along the same signal path.
- Both sub-systems receive the RF Clock, Injection and Bunch 1 markers from SPS LLRF and Timing systems / used to synchronize and sequence operations.
- The 200MHz SPS RF Clock is multiplied to obtain the 2GHz sample clock, this clock is then doubled by the ADC and DACs to achieve 4GSa/s.
- Adjustable delay lines are included to align the input sampling, feedback output and excitation output to the beam bunch (10ps delay step resolution).
- RF Power Amplifier Specs: 0.02 to 1 GHz, 80 Watts (derated from 100W) / Manufacturer: Amplifier Research (Modular RF, Bethell, WA USA)

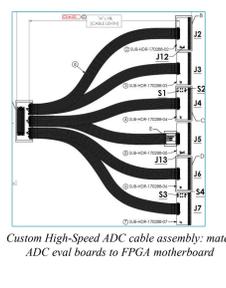
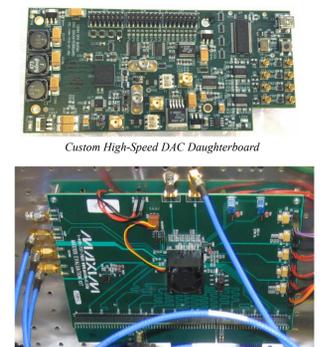
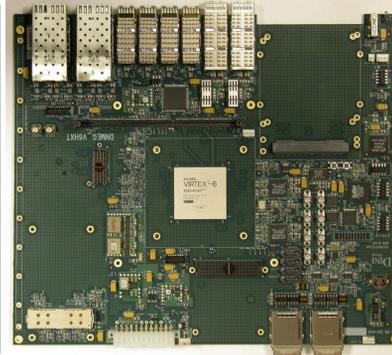


The Feedback Processor

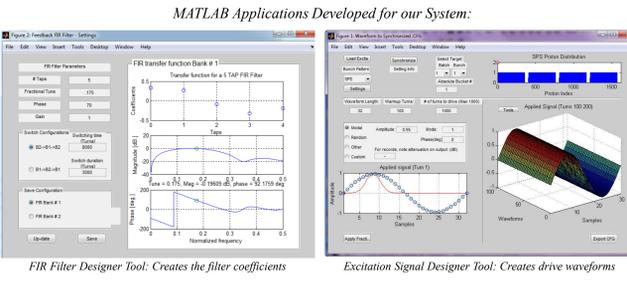


Feedback Processor:

- The Feedback Processor is a rapidly developed prototype, implemented using a mixture of commercial and custom-designed hardware. The entire system was designed, constructed and delivered to CERN in less than 10 months.
- The design is modular, based around a commercial FPGA motherboard, with a custom-designed DAC daughterboard plus two commercial ADC evaluation boards. The ADC boards connect to the motherboard using a custom high-speed cable assembly, developed commercially (Santec Corp). This design approach allowed us to quickly develop a solution within the confines of limited time and engineering resources.
- The custom DAC daughterboard contains the high-speed DAC, clocking circuits, trigger circuitry, general purpose analog and digital I/O and a USB 2.0 interface.
- The DAC is a Maxim Semi MAX19693 device (12-bit, 4GSa/s device used in 8-bit mode). The ADC is a MAX109 device (8-bits, 2GSa/s), two ADCs are used in interleaved mode to achieve the effective 4GSa/s rate. We used two MAX109 EVM evaluation boards to implement the ADC subsystem.
- All signal processing is implemented in the motherboard Xilinx Virtex-6, XC6VHX565T FPGA. The present design implements a bank of 16, 16-tap FIR filters. The filters are bandpass type, centered at the betatron frequency. The FIR Filters follow the relation: $y(n) = \sum_{k=0}^{15} h(k)x(n-k)$
- Diagnostic features include a special ADC snapshot memory that allows us to selectively capture up to 65536 turns of pre-processed ADC data and save for later analysis.
- Feedback Processor can also operate as an excitation driver (arbitrary waveform generator) as well.
- All processing takes place on edges of the SPS RF clock. Acquisition, processing and output operations are sequenced from the SPS Injection and Bunch 1 marker signals.

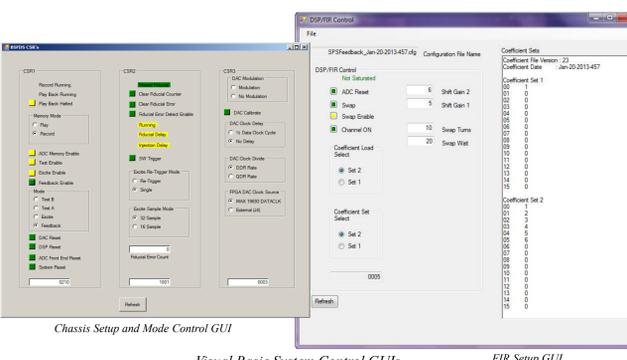


System Software

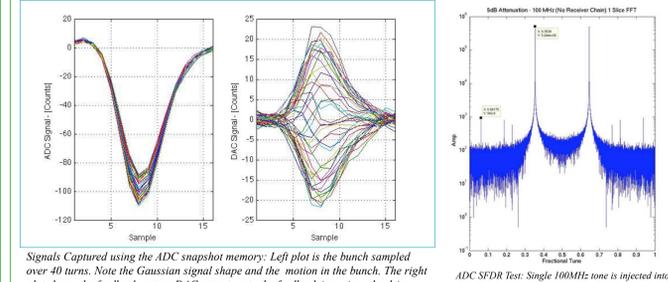


System Software:

The system control and data transfer software is GUI based and developed in Microsoft Visual Basic 2010. The GUIs interface with the system over USB using driver calls. A suite of offline MATLAB-based applications have been developed to facilitate configuration of the feedback mode, generation of excitation data files, design of the FIR filters, and analysis and display of the ADC snapshot data. Transfer between Visual Basic and MATLAB is done using text based configuration and data files, generated automatically by the SW. The software runs on a Windows 7 PC. All USB I/O uses Windows driver calls. Additional off-line Matlab tools have been developed for data analysis and simulation.

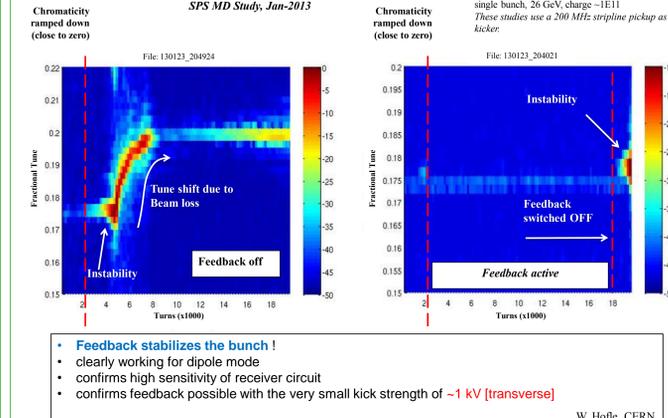


Results/Performance



Results and Operational Experience:

MD measurements were made at the SPS between Nov-2012 and Feb-2013. A large amount of data was collected. Preliminary results indicate that we were successfully able to control mode 0 instabilities with feedback. Higher order modes were also observed. See [3].



• Feedback stabilizes the bunch!
 • clearly working for dipole mode
 • confirms high sensitivity of receiver circuit
 • confirms feedback possible with the very small kick strength of ~1 kV [transverse]