LLRF Using SoC FPGA's in a Multiple Development Tool Environment

P. Varghese, B. Chase, E. Cullerton
FNAL, AD-LLRF Group

Introduction

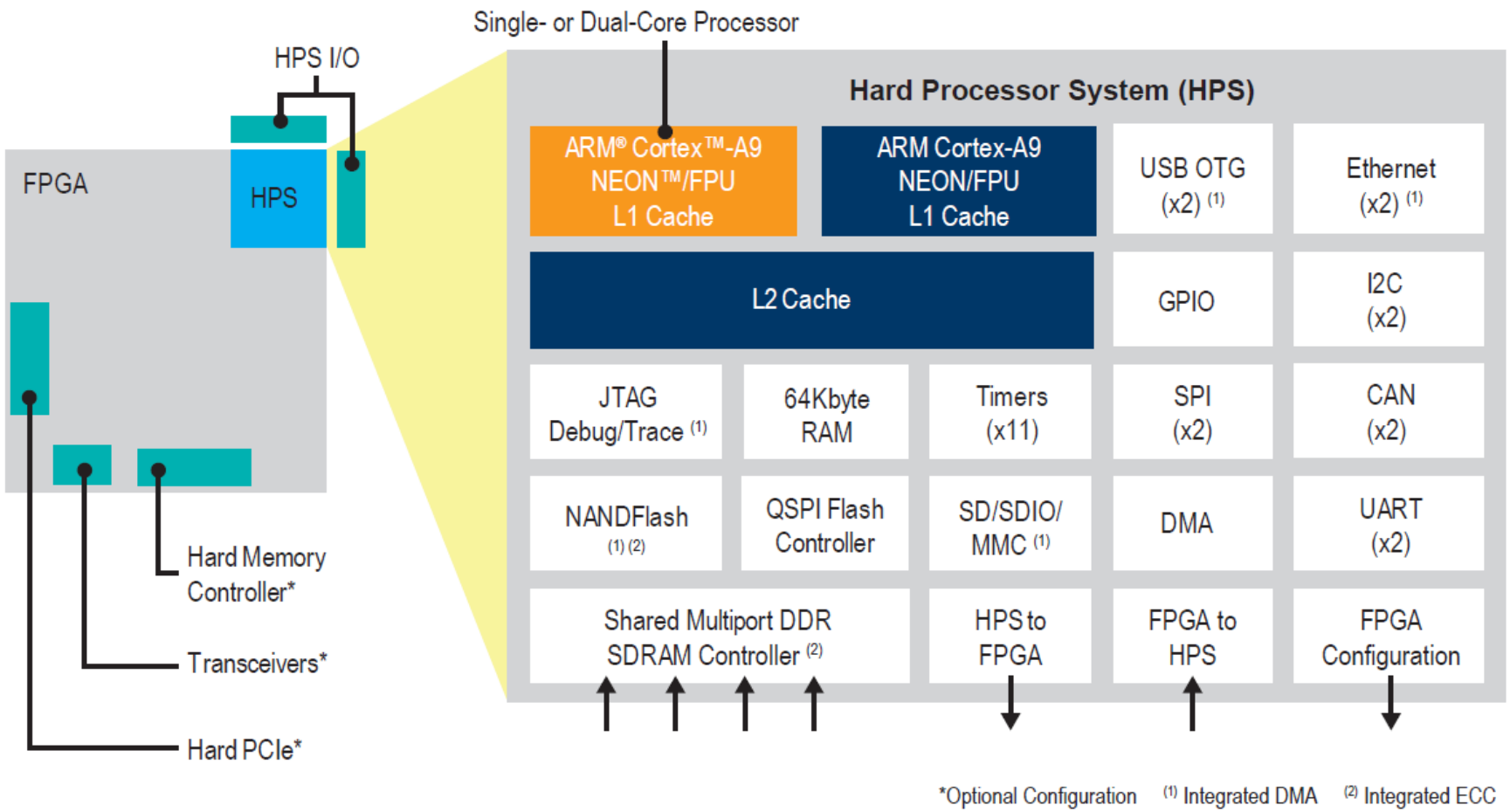
- What is in a SoC FPGA – Architecture and Available Devices from Altera and Xilinx

- Design and Development Tools for FPGA , ARM Hard Processor core and NIOS Soft Processor core

- Altera Cyclone V SoCKit

- LLRF system Design Example on the SoCKit

SOC FPGA

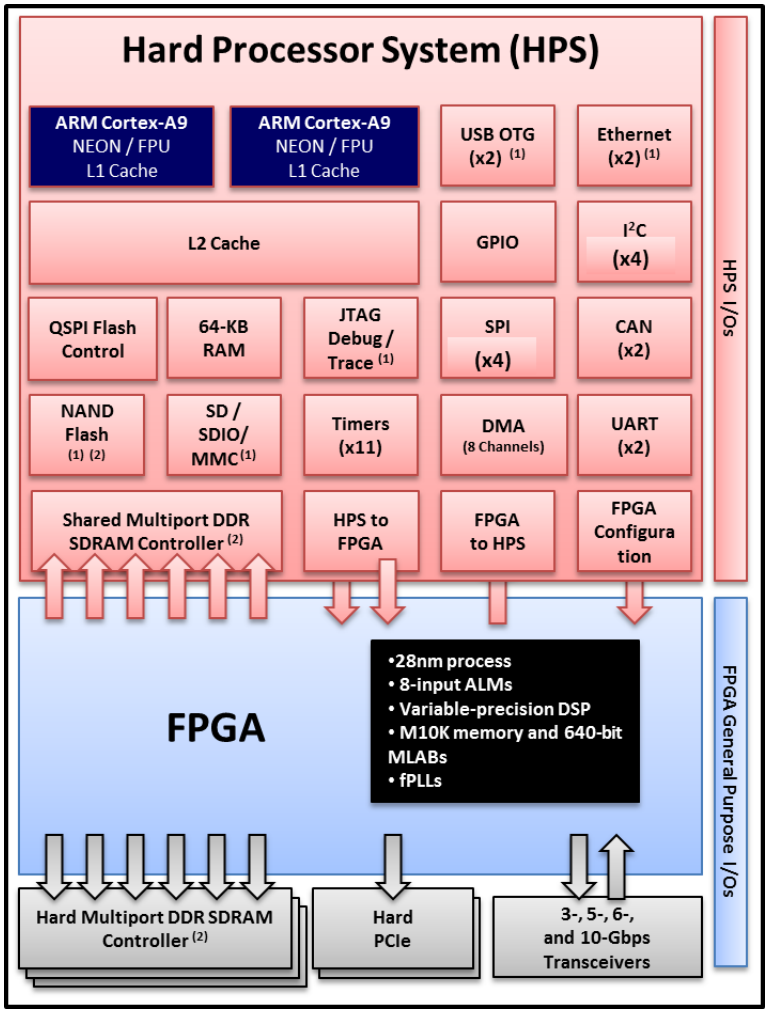

Single- or Dual-Core Processor
HPS I/O
FPGA
HPS
Hard Memory Controller*
Transceivers*
Hard PCIe*
Hard Processor System (HPS)
ARM® Cortex™-A9 NEON™/FPU L1 Cache
ARM Cortex-A9 NEON/FPU L1 Cache
USB OTG (x2) (1)
Ethernet (x2) (1)
L2 Cache
GPIO
I2C (x2)
JTAG Debug/Trace (1)
64Kbyte RAM
Timers (x11)
SPI (x2)
CAN (x2)
NANDFlash (1) (2)
QSPI Flash Controller
SD/SDIO/ MMC (1)
DMA
UART (x2)
Shared Multiport DDR SDRAM Controller (2)
HPS to FPGA
FPGA to HPS
FPGA Configuration
*Optional Configuration
(1) Integrated DMA
(2) Integrated ECC

Development Tools and Devices

Altera	**Xilinx**
Quartus II	ISE
QSYS	VIVADO
Nios EDS (soft processor core)	SDK Embedded Software Tools
DS-5 (ARM hard processor core)	
DSP Builder (Altera Simulink BlockSet)	System Generator
Cyclone V SoC, Arria V SoC	ZYNQ-7000
460K LE, 20 Mb Onchip RAM	444K LE, 24 Mb Onchip RAM

SoC System Architecture

- Processor
  - Dual-core ARM® Cortex™-A9 MP Core™ processor
  - 4,000 MIPS (up to 800 MHz per core)
  - NEON coprocessor with double-precision FPU
  - Rich set of embedded peripherals
  - 32-KB/32-KB L1 caches per core
  - 512-KB shared L2 cache
- Multiport SDRAM controller
  - Up to 533-MHz DDR3 and LPDDR2*
  - Up to 400-MHz DDR2
  - Integrated ECC support
  - Cache coherency between ARM & FPGA IP
- High-bandwidth on-chip interfaces
  - > 125-Gbps HPS-to-FPGA interface
  - > 125-Gbps FPGA-to-SDRAM interface

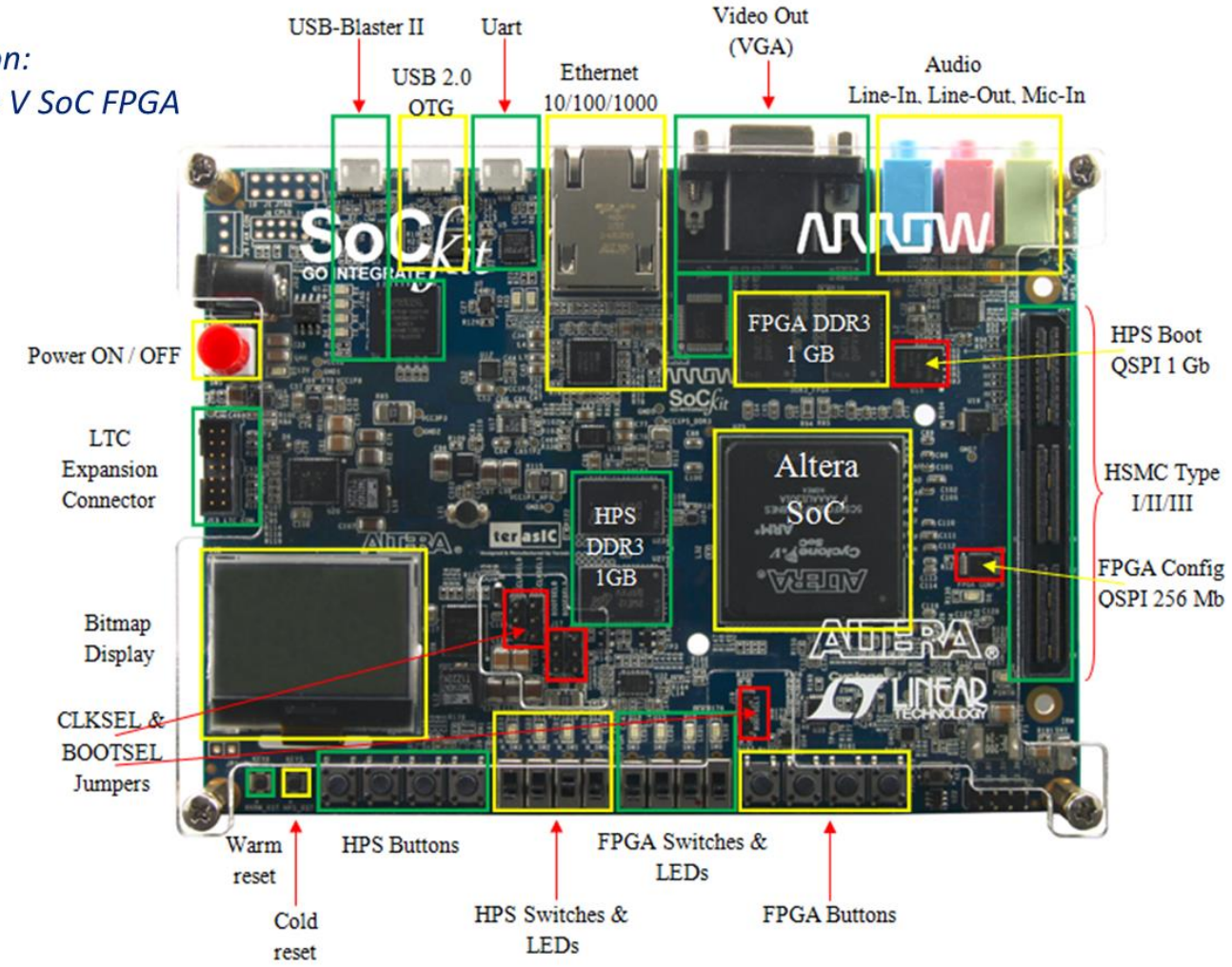


FPGA – HPS Connections

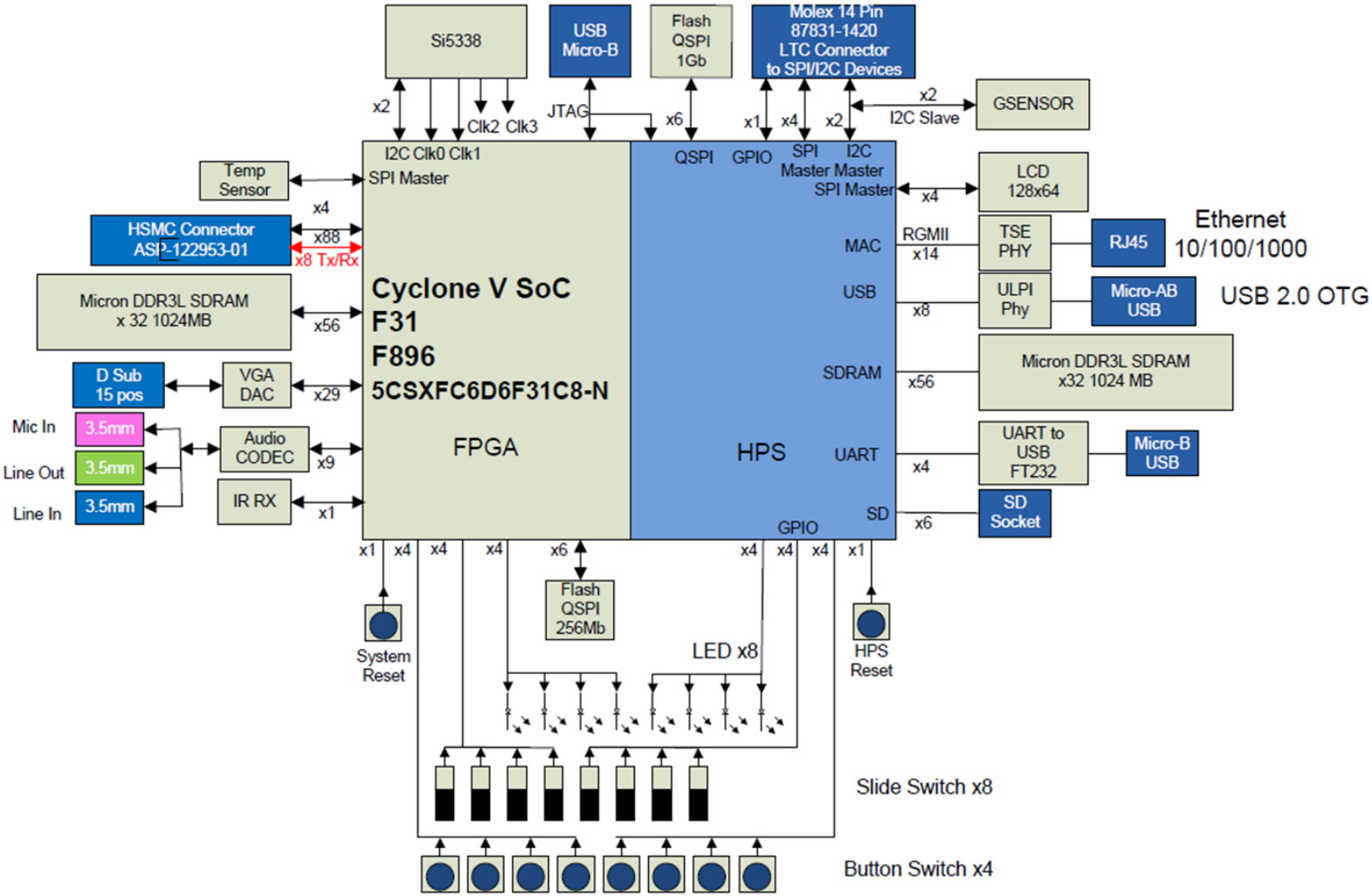
FPGA		HPS
(AXI, 32 / 64 / 128 bit)	→	FPGA-to-HPS bridge (L3 Interconnect)
(AXI, 32 / 64 / 128 bit)	←	HPS-to-FPGA bridge
(AXI 32-bit)	←	Lightweight HPS-to-FPGA bridge
FPGA-to-HPS SDRAM	→	(Up to six ports, 32 / 64 / 128 / 256 bit)
FPGA clocks and resets	↔	HPS clocks and resets
(FPGA JTAG)	←	HPS-to-FPGA JTAG (Scan Manager)
(HPS trace data to FPGA)	←	TPIU trace
(FPGA trace events to HPS trace))	→	FPGA System Trace Macrocell (STM)
(FPGA triggers to/from HPS)	↔	HPS Cross-trigger
(4 channels)	↔	DMA peripheral interface
(FPGA config, boot and GPIO signals)	↔	FPGA manager interface
(MPU interrupts from FPGA)	→	MPU Interrupts (64)
(MPU status to FPGA)	↔	MPU standby, wake and events

Arrow's SoCkit Development Board

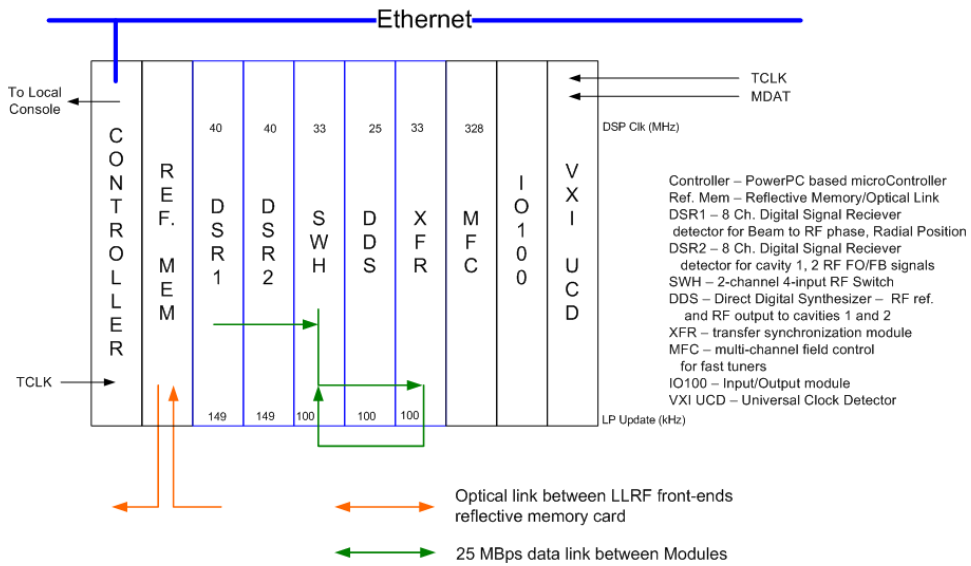
Based on:
Cyclone V SoC FPGA

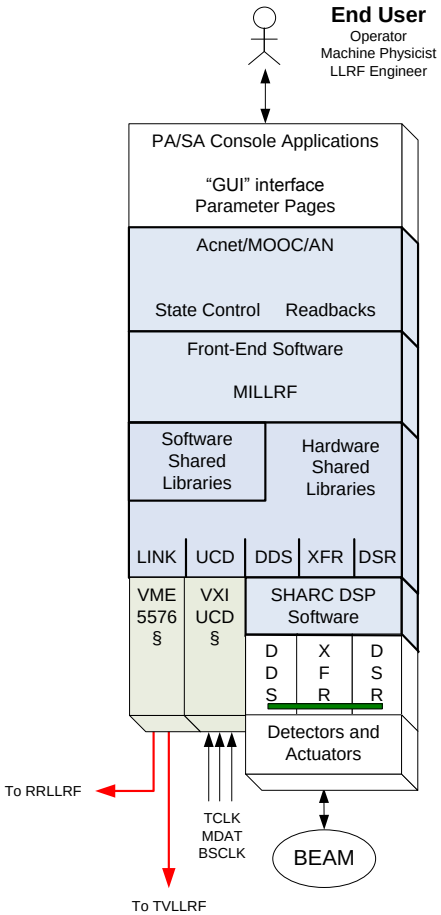


SoCKit Peripherals

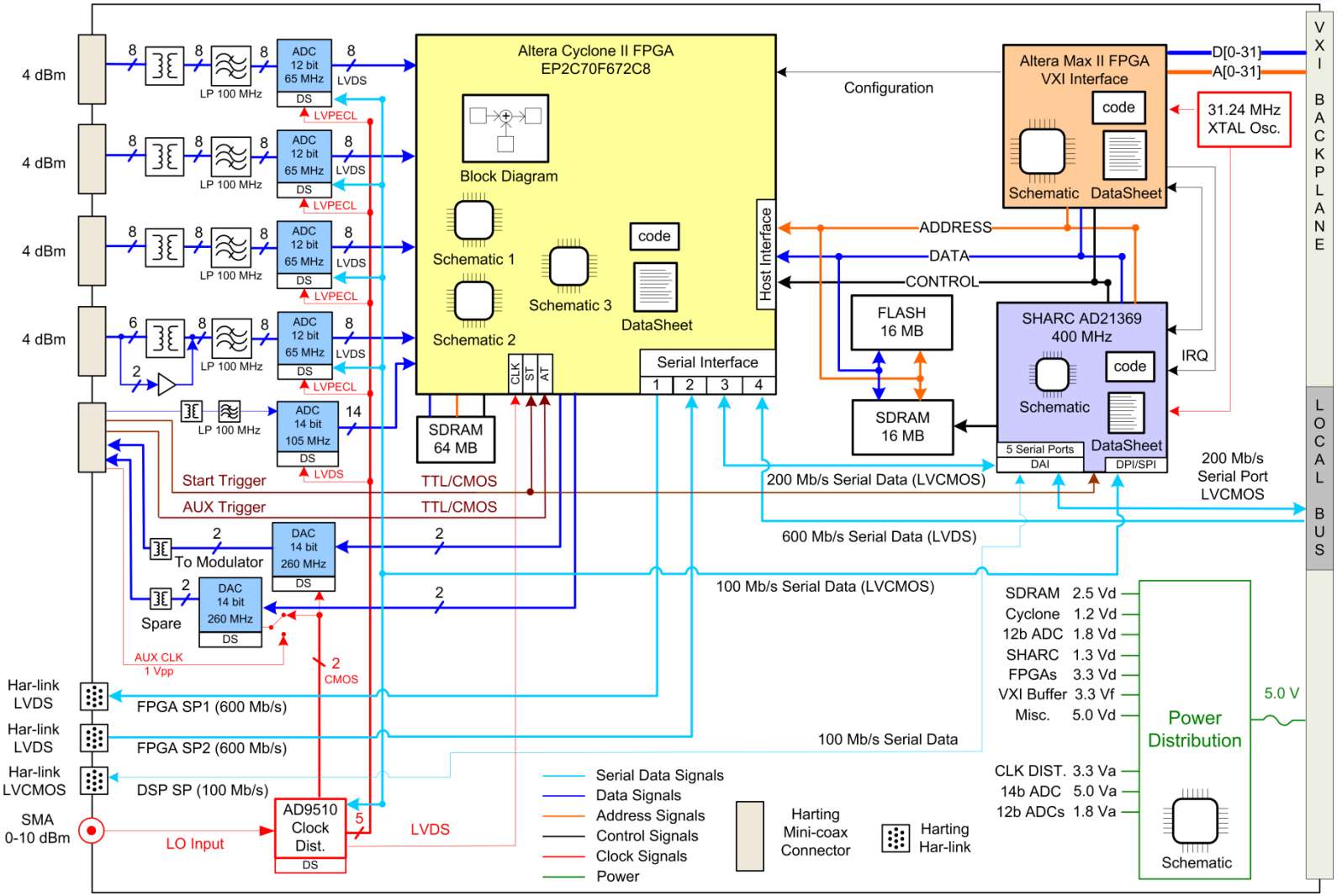


LLRF Hardware and Software

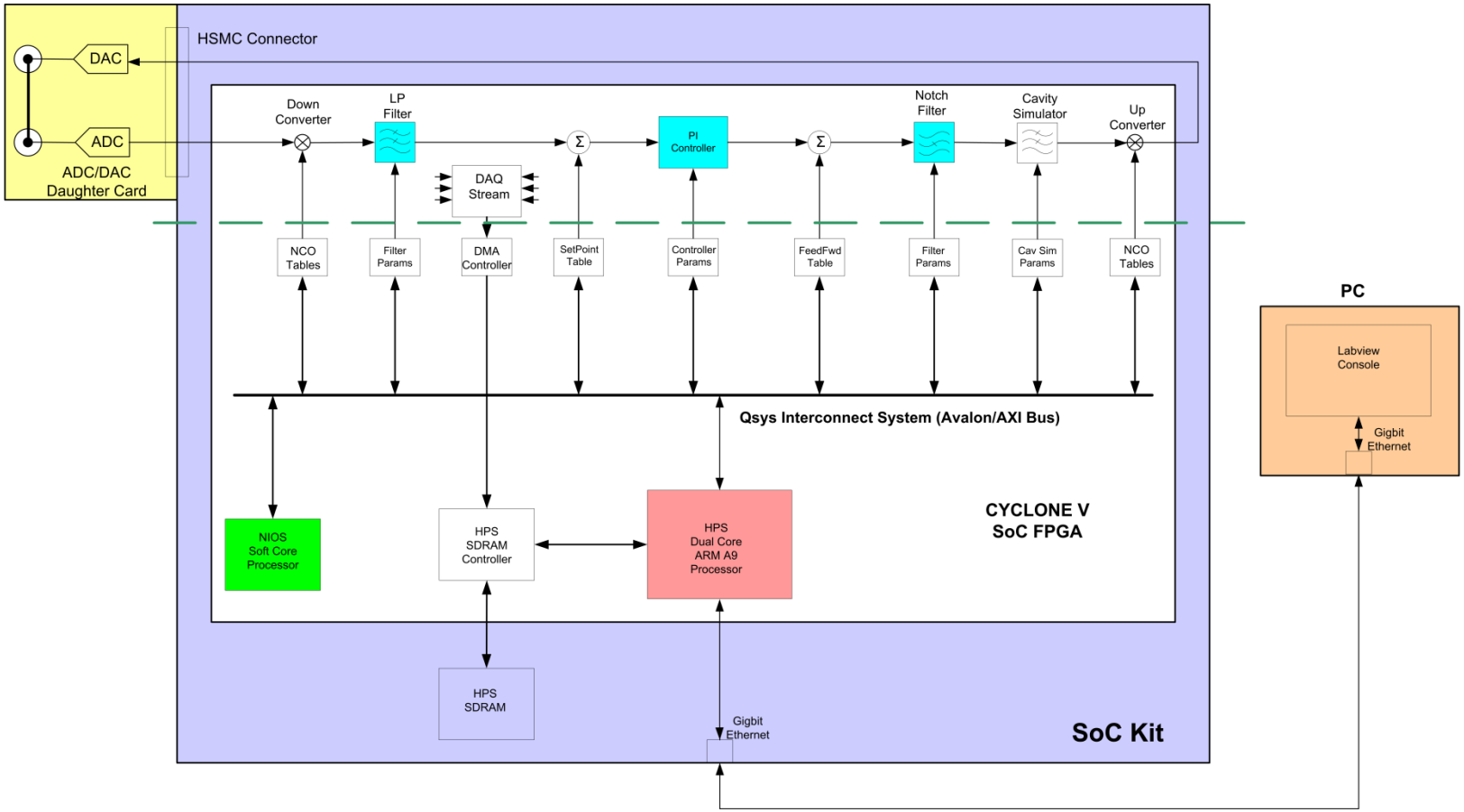




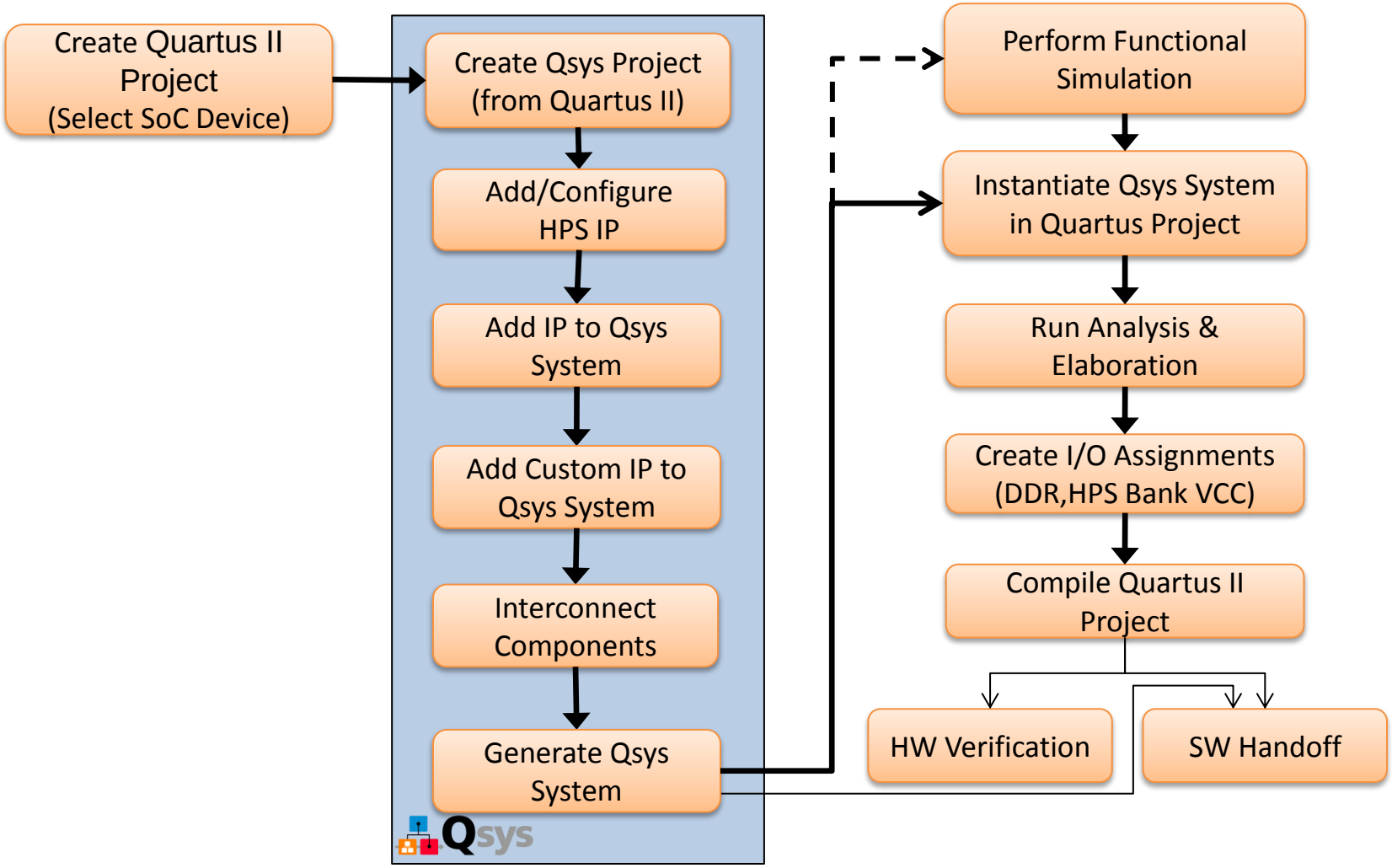
MFC VXI Card


4 dBm
LP 100 MHz
ADC 12 bit 65 MHz
DS
LVDS
LVPECL
ADC 14 bit 105 MHz
Altera Cyclone II FPGA
EP2C70F672C8
Block Diagram
Schematic 1
Schematic 2
Schematic 3
code
DataSheet
Host Interface
Serial Interface
CLK
ST
AT
SDRAM 64 MB
Configuration
Altera Max II FPGA
VXI Interface
Schematic
DataSheet
D[0-31]
A[0-31]
31.24 MHz XTAL Osc.
ADDRESS
DATA
CONTROL
FLASH 16 MB
SDRAM 16 MB
SHARC AD21369 400 MHz
IRQ
5 Serial Ports
DAI
DPI/SPI
VXI BACKPLANE
LOCAL BUS
Start Trigger
AUX Trigger
TTL/CMOS
200 Mb/s Serial Data (LVCMOS)
200 Mb/s Serial Port LVCMOS
600 Mb/s Serial Data (LVDS)
100 Mb/s Serial Data (LVCMOS)
100 Mb/s Serial Data
To Modulator
Spare
DAC 14 bit 260 MHz
AUX CLK 1 Vpp
CMOS
Har-link LVDS
FPGA SP1 (600 Mb/s)
FPGA SP2 (600 Mb/s)
Har-link LVCMOS
DSP SP (100 Mb/s)
SMA 0-10 dBm
LO Input
AD9510 Clock Dist.
SDRAM 2.5 Vd
Cyclone 1.2 Vd
12b ADC 1.8 Vd
SHARC 1.3 Vd
FPGAs 3.3 Vd
VXI Buffer 3.3 Vf
Misc. 5.0 Vd
CLK DIST. 3.3 Va
14b ADC 5.0 Va
12b ADCs 1.8 Va
Power Distribution
5.0 V
Serial Data Signals
Data Signals
Address Signals
Control Signals
Clock Signals
Power
Harting Mini-coax Connector
Harting Har-link

LLRF System Example



FPGA Design Flow



QSYS System Interconnect Tool

File Edit System View Tools Help

Component Library

- Project
  - New Component...
  - My_IP_Cores
    - reg16_component
    - reg32_component
    - reg8_component
  - Other
  - System
    - soc_system
- Library
  - Config-Bypass App Example
  - Bridges
  - Bridges and Adapters
  - Clock and Reset
    - Clock Source
    - Reset Controller
  - Configuration & Programming
  - DSP
  - Embedded Processors
    - Bitswap
    - Custom Instruction Interconnect
    - Custom Instruction Master Translator
    - Custom Instruction Slave Translator
    - Floating Point Hardware
    - Hard Processor System
    - Nios II Processor
  - Interface Protocols
  - Memories and Memory Controllers
    - External Memory Interfaces
    - On-Chip
  - Merlin Components
  - Microcontroller Peripherals
    - Altera Avalon Mutex
  - Peripherals
  - PLL
  - Qsys Interconnect
  - Verification
  - Window Bridge

New... Edit... Add...

System Contents | Address Map | Clock Settings | Project Settings | Instance Parameters | System Inspector | HDL Example | Generation

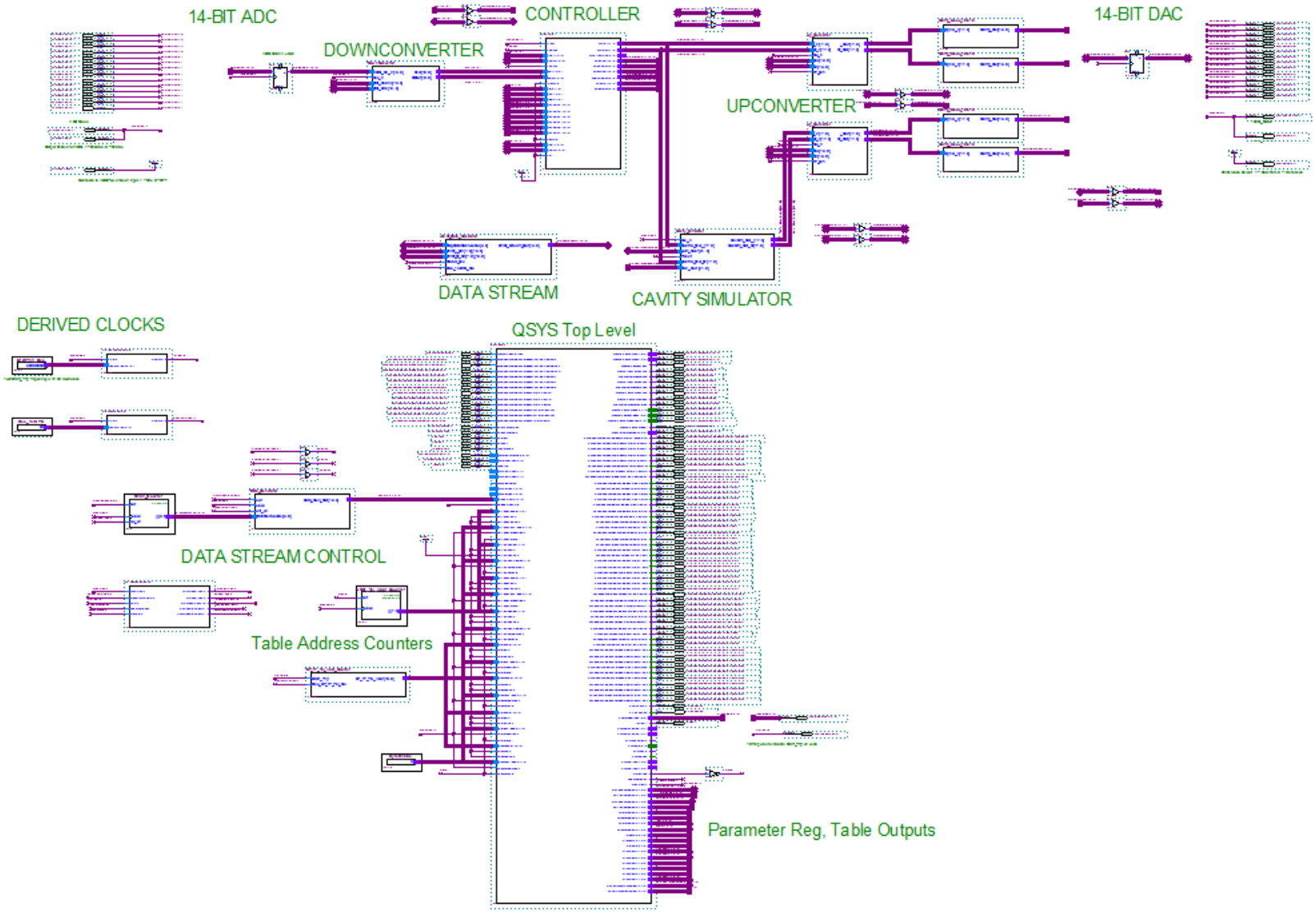
Use	C...	Name	Description	Export	Clock	Base	End	IRQ
✓		hps_0	Hard Processor System		multiple	0x0000_0000	0xffff_ffff	
✓		onchip_memory2_0	On-Chip Memory (RAM or ROM)		clk_0	0x0000_0000	0x0000_ffff	
✓		master_secure	JTAG to Avalon Master Bridge		clk_0			
✓		sysid_qsys	System ID Peripheral		clk_0	0x0001_0000	0x0001_0007	
✓		led_pio	PIO (Parallel I/O)		clk_0	0x0001_0040	0x0001_004f	
✓		dipsw_pio	PIO (Parallel I/O)		clk_0	0x0001_0080	0x0001_008f	0
✓		button_pio	PIO (Parallel I/O)		clk_0	0x0001_00c0	0x0001_00cf	1
✓		jtag_uart	JTAG UART		clk_0	0x0002_0000	0x0002_0007	2 1
✓		master_non_sec	JTAG to Avalon Master Bridge		clk_0			
✓		intr_capturer_0	Interrupt Capture Module		clk_0	0x0003_0000	0x0003_0007	
✓		clk_0	Clock Source					
✓		nios2_qsys	Nios II Processor		clk_0	0x0001_4800	0x0001_4fff	
✓		onchip_memory2	On-Chip Memory (RAM or ROM)		clk_0	0x0006_0000	0x0007_ffff	
✓		timer	Interval Timer		clk_0	0x0001_5a40	0x0001_5a5f	0
✓		pll_qsys	Altera PLL		clk_0			
✓		key	PIO (Parallel I/O)		clk_0	0x0001_5a60	0x0001_5a6f	3
✓		daq_sgdma	Scatter-Gather DMA Controller		clk_0	0x0001_5a00	0x0001_5a3f	2
✓		daq_desc_mem	On-Chip Memory (RAM or ROM)		clk_0	0x0001_5600	0x0001_57ff	
✓		Down_Converter_Tbl_Cos1	On-Chip Memory (RAM or ROM)		multiple	multiple	multiple	
✓		Down_Converter_Tbl_Sin1	On-Chip Memory (RAM or ROM)		multiple	multiple	multiple	
✓		Up_Converter_Tbl_Cos1	On-Chip Memory (RAM or ROM)		multiple	multiple	multiple	
✓		Up_Converter_Tbl_Sin1	On-Chip Memory (RAM or ROM)		multiple	multiple	multiple	
✓		Set_Point_Tbl_I	On-Chip Memory (RAM or ROM)		multiple	multiple	multiple	
✓		Set_Point_Tbl_Q	On-Chip Memory (RAM or ROM)		multiple	multiple	multiple	
✓		Feed_Fwd_Tbl_I	On-Chip Memory (RAM or ROM)		multiple	multiple	multiple	
✓		Feed_Fwd_Tbl_Q	On-Chip Memory (RAM or ROM)		multiple	multiple	multiple	
✓		Int_Gain	reg32_component		clk_0	0x0001_5a7c	0x0001_5a7f	
✓		Prop_Gain	reg16_component		clk_0	0x0001_5a8c	0x0001_5a8d	
✓		Int_Pole	reg32_component		clk_0	0x0001_5a78	0x0001_5a7b	
✓		NtchA_D2	reg16_component		clk_0	0x0001_5a8a	0x0001_5a8b	
✓		NtchA_N0	reg16_component		clk_0	0x0001_5a88	0x0001_5a89	
✓		NtchA_N1	reg16_component		clk_0	0x0001_5a86	0x0001_5a87	
✓		NtchB_D2	reg16_component		clk_0	0x0001_5a84	0x0001_5a85	
✓		NtchB_N0	reg16_component		clk_0	0x0001_5a82	0x0001_5a83	
✓		NtchB_N1	reg16_component		clk_0	0x0001_5a80	0x0001_5a81	
✓		Cav_Sim_Num_Coef	reg32_component		clk_0	0x0001_5a74	0x0001_5a77	
✓		Cav_Sim_Den_Coef	reg32_component		clk_0	0x0001_5a70	0x0001_5a73	

Interconnect Detail

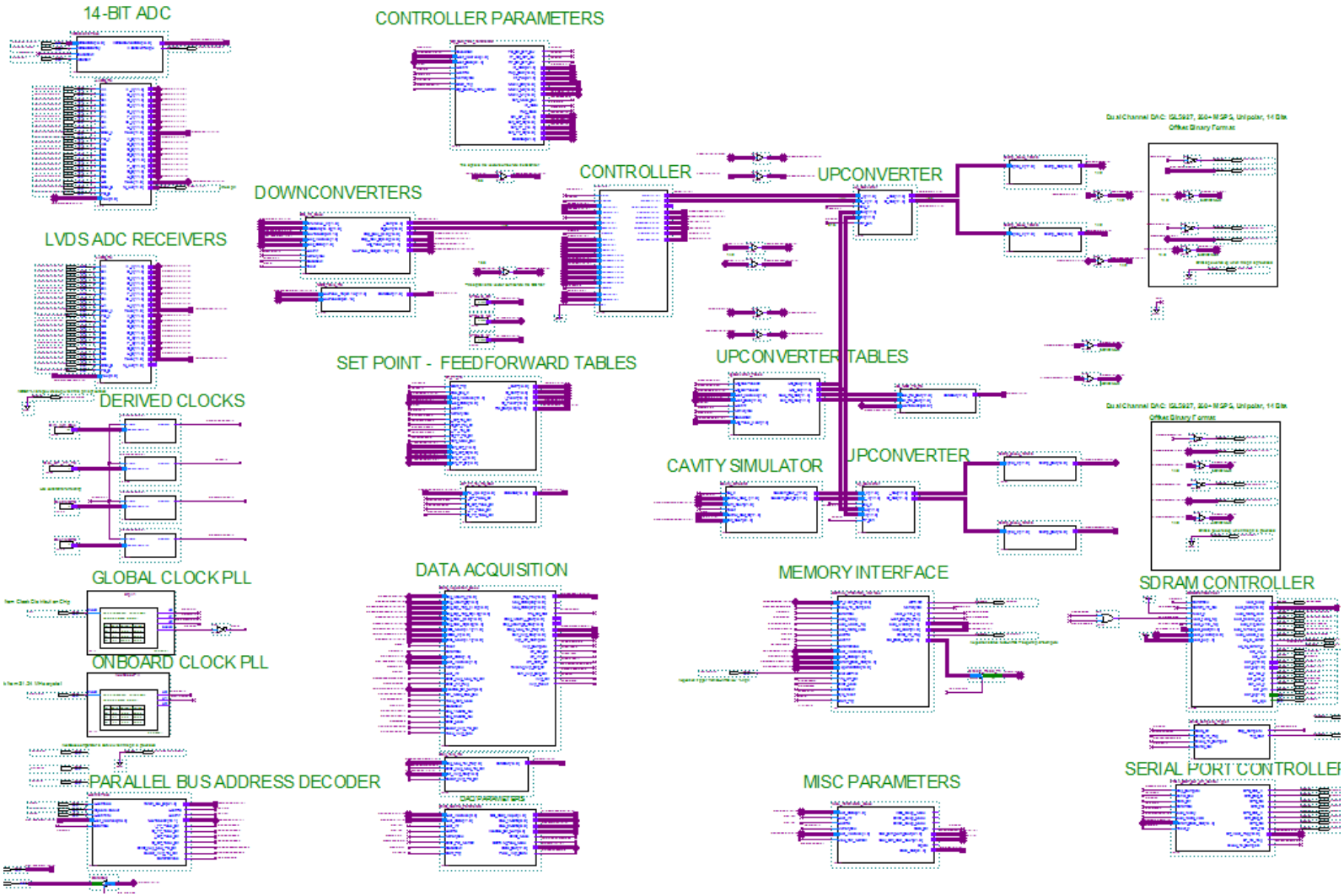
System Contents | Address Map | Clock Settings | Project Settings | Instance Parameters | System Inspector | HDL Example | Generation

Connections	Name	Description	Export	Clock
	hps_0	Hard Processor System		
	memory	Conduit	memory	
	hps_io	Conduit	hps_0_hps_io	
	h2f_reset	Reset Output	hps_0_h2f_reset	
	h2f_axi_clock	Clock Input	Double-click to export	clk_0
	h2f_axi_master	AXI Master	Double-click to export	[h2f_axi_clock]
	f2h_axi_clock	Clock Input	Double-click to export	clk_0
	f2h_axi_slave	AXI Slave	Double-click to export	[f2h_axi_clock]
	h2f_lw_axi_clock	Clock Input	Double-click to export	clk_0
	h2f_lw_axi_master	AXI Master	Double-click to export	[h2f_lw_axi_clock]
	onchip_memory2_0	On-Chip Memory (RAM or ROM)		
	clk1	Clock Input	Double-click to export	clk_0
	s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]
	reset1	Reset Input	Double-click to export	[clk1]
	master_secure	JTAG to Avalon Master Bridge		
	clk	Clock Input	Double-click to export	clk_0
	clk_reset	Reset Input	Double-click to export	
	master	Avalon Memory Mapped Master	Double-click to export	[clk]
	master_reset	Reset Output	Double-click to export	
	sysid_qsys	System ID Peripheral		
	clk	Clock Input	Double-click to export	clk_0
	reset	Reset Input	Double-click to export	[clk]
	control_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]
	led_pio	PIO (Parallel I/O)		
	clk	Clock Input	Double-click to export	clk_0
	reset	Reset Input	Double-click to export	[clk]
	s1	Avalon Memory Mapped Slave	Double-click to export	[clk]
	external_connection	Conduit	led_pio_external_connection	
	dipsw_pio	PIO (Parallel I/O)		
	clk	Clock Input	Double-click to export	clk_0
	reset	Reset Input	Double-click to export	[clk]
	s1	Avalon Memory Mapped Slave	Double-click to export	[clk]
	external_connection	Conduit	dipsw_pio_external_conne...	
	button_pio	PIO (Parallel I/O)		
	clk	Clock Input	Double-click to export	clk_0
	reset	Reset Input	Double-click to export	[clk]
	s1	Avalon Memory Mapped Slave	Double-click to export	[clk]
	external_connection	Conduit	button_pio_external_conne...	
	jtag_uart	JTAG UART		
	clk	Clock Input	Double-click to export	clk_0

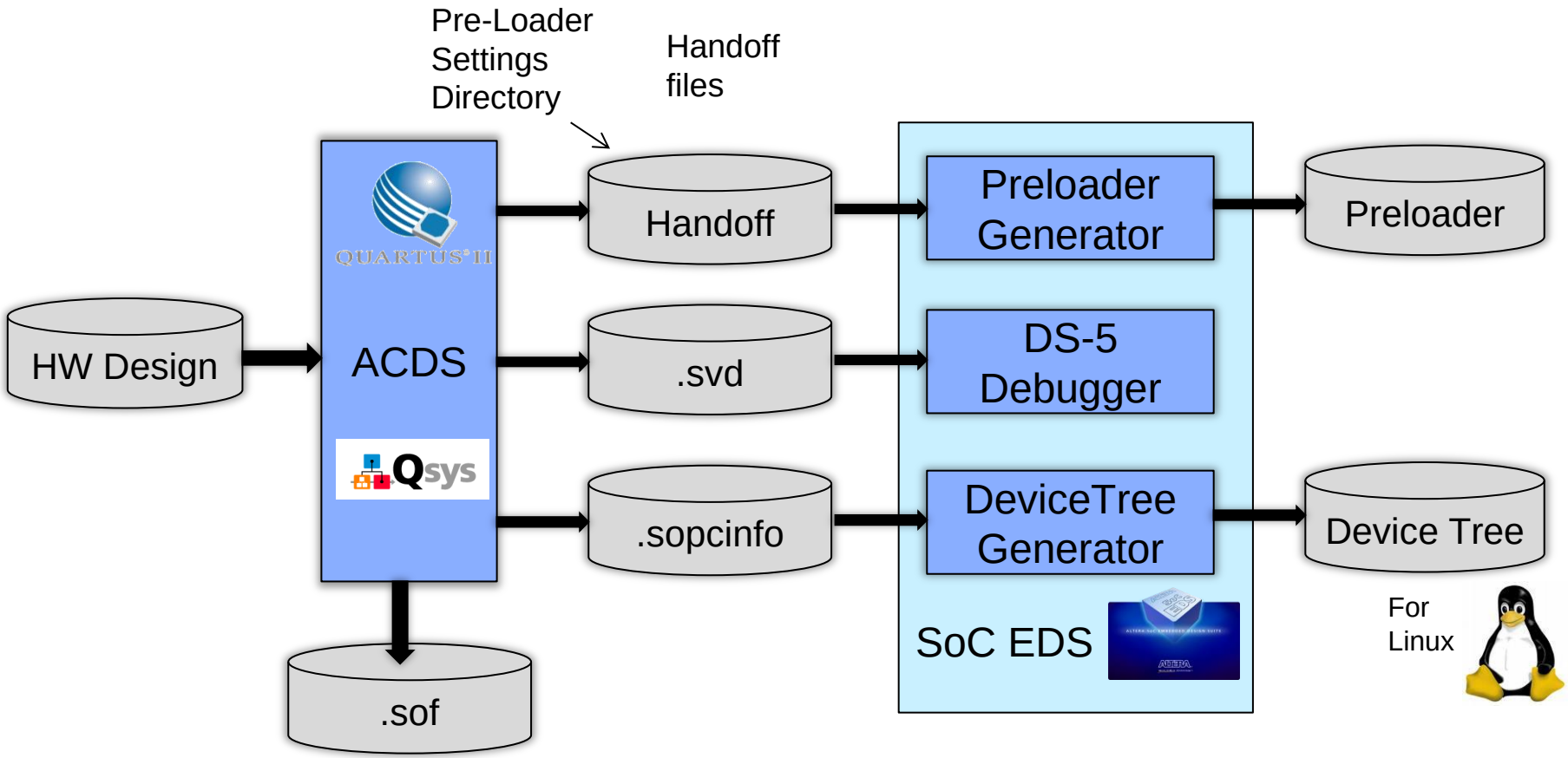
FPGA Project for Example Design



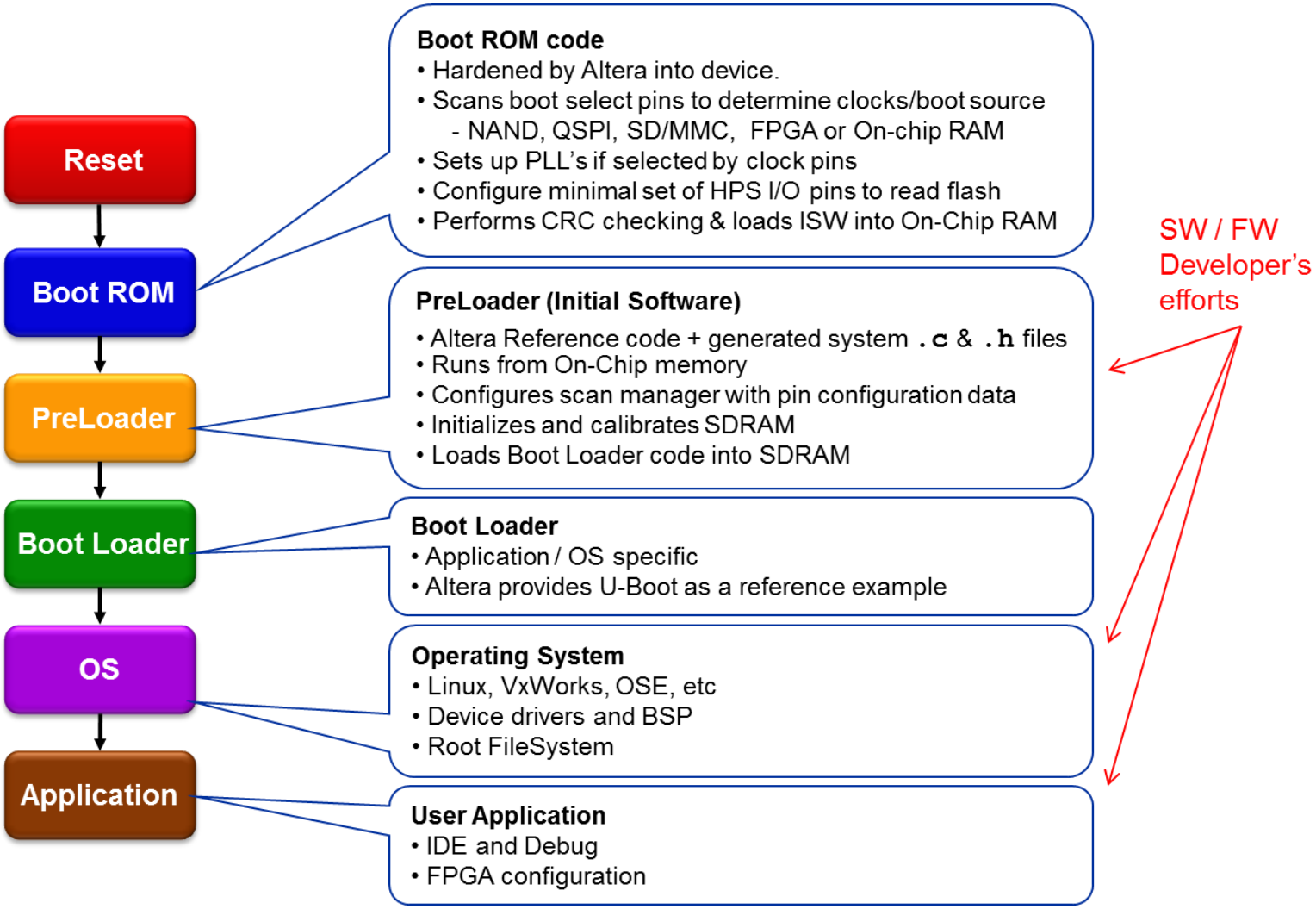
FPGA Project for 8-Cavity CM



Hardware/Software Design Flow

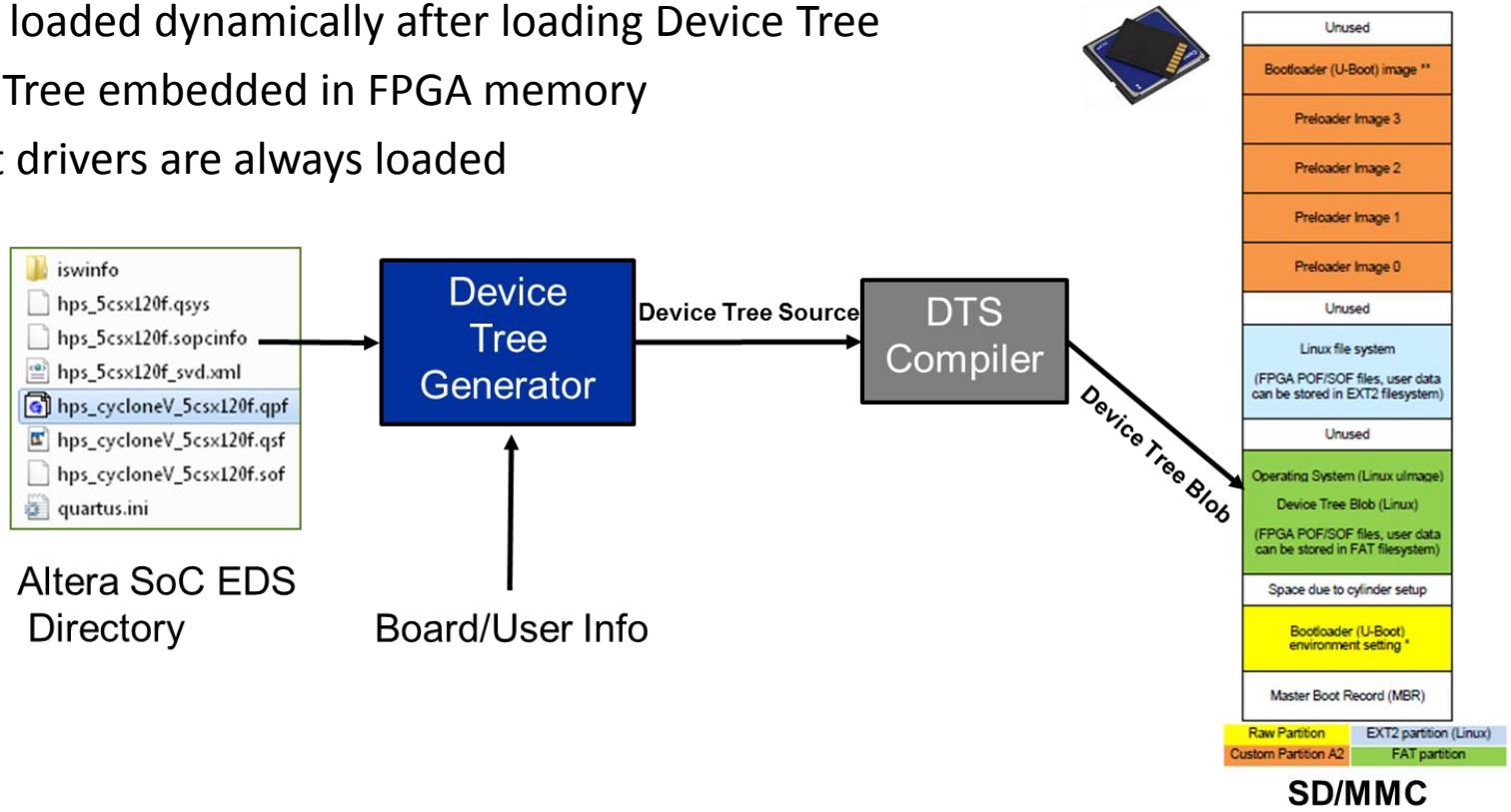


HPS Boot Stages

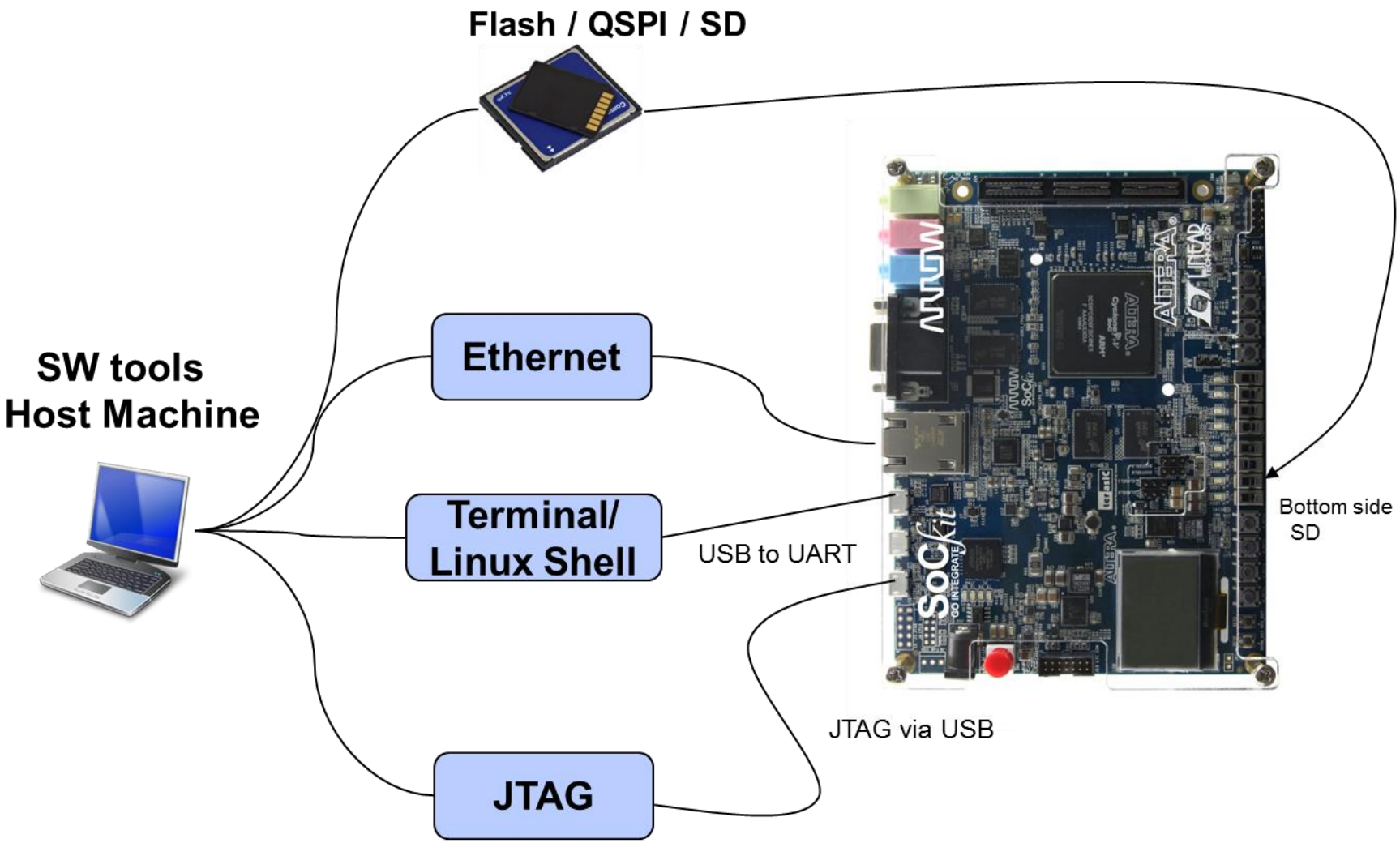


Device Tree

- A Data Structure for describing hardware
- Enables Device Drivers to be linked to Linux kernel at run-time
  - No Linux kernel recompile required
  - Drivers loaded dynamically after loading Device Tree
  - Device Tree embedded in FPGA memory
  - Correct drivers are always loaded



Debug Interfaces



DS-5 Debugger for ARM

DS-5 Debug - HPS/linux-bringup/drivers/gpio/gpio-altera.c - Eclipse Platform

File Edit Source Refactor Navigate Search Project Run Window Help

Debug Cont | Project Expl | Remote Sys

Altera SoC FPGA connected
Active Threads
blinky #4 stopped on breakpoint #2 (PID 481 w
arch_local_irq_save
altera_gpio_set+0x8
gpio_set_value_cansleep+0x6C
gpio_value_store+0xC0
dev_attr_store+0x18
flush_write_buffer+0x40
sysfs_write_file+0x108
vfs_write+0xA4
sys_write+0x40
S:0x8000E700

Altera SoC FPGA connected

Commands | History | Scripts

Linked: Altera SoC FPGA

```
wait
continue
Execution stopped at breakpoint 2: S:0x7F000038
In thread 2 (OS thread id 479)
S:0x7F000038   85,0   {
wait
continue
Execution stopped at breakpoint 2: S:0x7F000038
In thread 3 (OS thread id 478)
S:0x7F000038   85,0   {
wait
continue
Execution stopped at breakpoint 2: S:0x7F000038
In thread 4 (OS thread id 481)
S:0x7F000038   85,0   {
```

Command: Press (Ctrl+Space) for Content Assist Submit

Breakpoints | Expressions | Functions

Linked: Altera SoC FPGA

Name	Start Address
altera_gpio_get	S:0x7F000000
altera_gpio_set	S:0x7F000038
altera_gpio_dir_in	S:0x7F000068
altera_gpio_dir_out	S:0x7F00009C
altera_gpio_save_regs	S:0x7F0000F0

Variables

Linked: Altera SoC FPGA

Name	Value	Type	Count	Size	Location
Locals	1 variable				
flags	27	long unsigned int		32	$R3
File Statics (current)					
Globals	954 variables				

gpio-altera.c

```
78  * @gpio:   GPIO signal number.
79  * @val:    Value to be written to specified signal.
80  *
81  * This function writes the specified value in to the
82  * GPIO device.
83  */
84 static void altera_gpio_set(struct gpio_chip *gc, uns
85 {
86     unsigned long flags;
87     struct of_mm_gpio_chip *mm_gc = to_of_mm_gpio_chi
88     struct altera_gpio_instance *chip = to_altera_gpi
89
90     spin_lock_irqsave(&chip->gpio_lock, flags);
91
92     /* Write to shadow register and output */
93     if (val)
94         chip->gpio_state |= 1 << gpio;
95     else
96         chip->gpio_state &= ~(1 << gpio);
97     __raw_writel(chip->gpio_state, mm_gc->regs + ALTE
98
99     spin_unlock_irqrestore(&chip->gpio_lock, flags);
100 }
101
102 /*
```

Disassembly

Linked: Altera SoC FPGA

<Next Instruction> 100

Address	Opcode	Disassembly
S:0x7F000024	15903050	LDRNE r3,[r0,#0x50]
S:0x7F000028	E5933000	LDR r3,[r3,#0]
S:0x7F00002C	E1A01133	LSR r1,r3,r1
S:0x7F000030	E2010001	AND r0,r1,#1
S:0x7F000034	E12FFF1E	BX lr
		altera_gpio_set
S:0x7F000038	E10F3000	MRS r3,APSR ; forme
S:0x7F00003C	F10C0080	CPSID i
S:0x7F000040	E3A0C001	MOV r12,#1
S:0x7F000044	E3520000	CMP r2,#0
S:0x7F000048	E5902054	LDR r2,[r0,#0x54]
S:0x7F00004C	1182111C	ORRNE r1,r2,r12,LSL r
S:0x7F000050	01C2111C	BICEQ r1,r2,r12,LSL r
S:0x7F000054	E5902050	LDR r2,[r0,#0x50]
S:0x7F000058	E5801054	STR r1,[r0,#0x54]
S:0x7F00005C	E5821000	STR r1,[r2,#0]
S:0x7F000060	E121F003	MSR CPSR_c,r3
S:0x7F000064	E12FFF1E	BX lr
		altera_gpio_dir_in
S:0x7F000068	E52D4004	PUSH {r4}

M | E | O | A | T | E | C | P | R

Linked: Altera SoC FPGA

Name	Value	Size	Access
sptimer0			
sptimer1			
stm			
sysmgr			
uart0			
uart1			
usb0			
usb1			
PIO_inst_0			
PIO_inst_0_DATA	0x0000000E	32	R/W
PIO_inst_0_DIRECTION	0x00000000	32	R/W
PIO_inst_0_IRQ_MASK	0x00000000	32	R/W
PIO_inst_0_EDGE_CAP	0x00000000	32	R/W
PIO_inst_0_SET_BIT	write only	32	WO
PIO_inst_0_CLEAR_BITS	write only	32	WO
UART_inst_0			
JTAG_UART_inst_0			
SYSID_inst_0			

Writable | Smart Insert | 86 : 25

Nios EDS Debugger

Nios II Debug - SoCKit_GHRD_DAQ/main.c - Eclipse

File Edit Source Refactor Navigate Search Run Project Nios II Window Help

Debug

SoCKit_GHRD_DAQ Nios II Hardware configuration [Nios II Hardware]
Altera CDI GDB Debugger (9/25/13 5:49 PM) (Suspended)
Thread [1] (Suspended: Signal 'SIGTRAP' received. Description: Trace/breakpoint trap.)
4 _exit() alt_exit.c:70 0x0006d608
3 exit() exit.c:67 0x0006d250
2 alt_main() alt_main.c:156 0x0006a4a4
1 _start() crt0.S:437 0x000601fc
<terminated, exit value: 0> nios2-download (9/25/13 5:49 PM)
nios2-download (9/25/13 5:49 PM)
nios2-elf-gdb (9/25/13 5:49 PM)

Variables | Breakpoints | Registers | Memory

0x0 : 0x0 <Hex> | New Renderings...

Address	0 - 3	4 - 7	8 - B
00000000	07FE07F8	07F807F8	07F807F8
00000010	07F807F8	07F807F8	07F807F8
00000020	07F907F9	07F907F9	07F907F9
00000030	07F907F9	07F907F9	07F907F9
00000040	07F807FA	07FA07FA	07FA07FA

system.h | main.c | alt_exit.c

```
IOWR_32DIRECT(INT_GAIN_BASE, 0, 0x1234);
IOWR_16DIRECT(PROP_GAIN_BASE, 0, 0x1234);
IOWR_32DIRECT(INT_POLE_BASE, 0, 0x1234);
IOWR_16DIRECT(NTCHA_D2_BASE, 0, 0x91c9);
IOWR_16DIRECT(NTCHA_N0_BASE, 0, 0x774d);
IOWR_16DIRECT(NTCHA_N1_BASE, 0, 0x8de2);
IOWR_16DIRECT(NTCHB_D2_BASE, 0, 0x91c9);
IOWR_16DIRECT(NTCHB_N0_BASE, 0, 0x774d);
IOWR_16DIRECT(NTCHB_N1_BASE, 0, 0x8de2);
IOWR_32DIRECT(CAV_SIM_NUM_COEF_BASE, 0, 0x1234);
IOWR_32DIRECT(CAV_SIM_DEN_COEF_BASE, 0, 0x1234);

// Reset the sgdma controller
IOWR_32DIRECT(DAQ_SGDMA_BASE, 16, 0x10000);
usleep(1000);
IOWR_32DIRECT(DAQ_SGDMA_BASE, 16, 0x10000);
usleep(1000);

// Open the streaming scatter-gather DMA controller
```

Outline

terasic_includes.h
mem_verify.h
altera_avalon_sgdma.h
altera_avalon_sgdma_descriptor.h
altera_avalon_sgdma_regs.h
sys/alt_irq.h
system.h
altera_avalon_pio_regs.h
STATUS_BIT_DONE
STATUS_BIT_FAIL
STATUS_BIT_SUCCESS
Stream_DMA_desc0
Stream_DMA_callback_function() : void
pulses_done : volatile int

Console | Tasks | Nios II Console

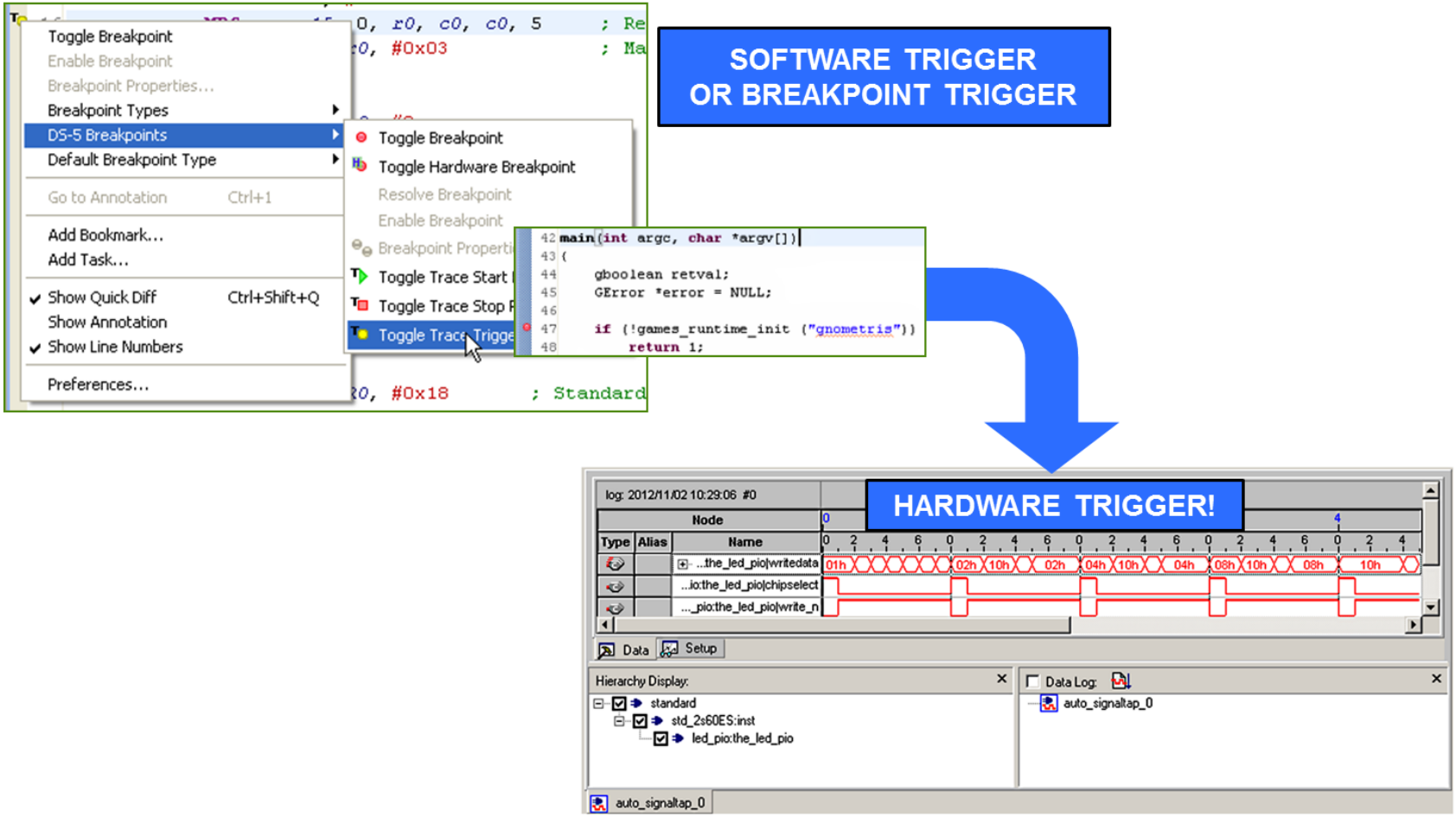
SoCKit_GHRD_DAQ Nios II Hardware configuration - cable: CV SoCKit on localhost [USB-1] device ID: 1 instance ID: 0 name: jtaguart_0

```
Number of Pulses = 3
```

Writable | Smart Insert | 103 : 1

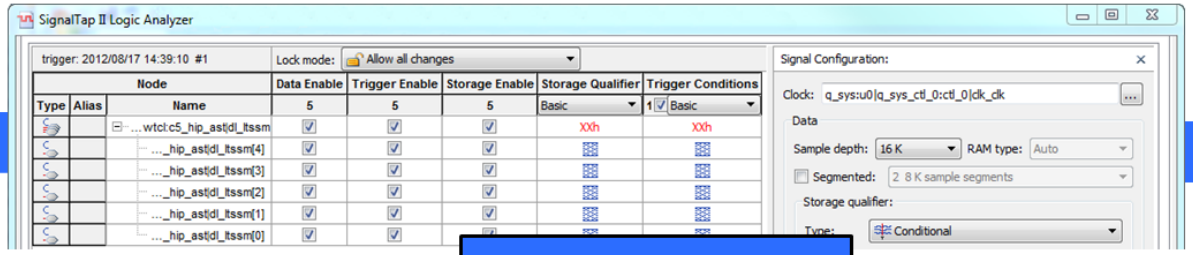
Cross Domain Debug1

- Trigger from software to FPGA



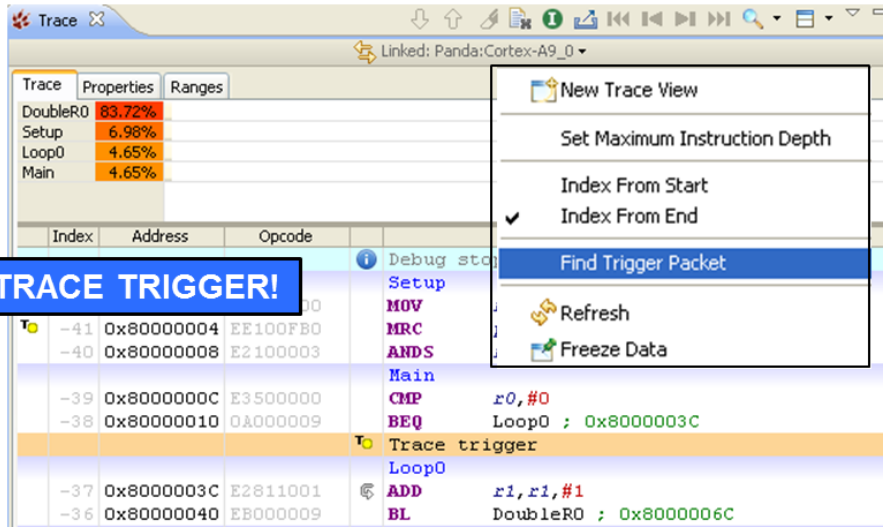
Cross Domain Debug 2

- Trigger from FPGA to software



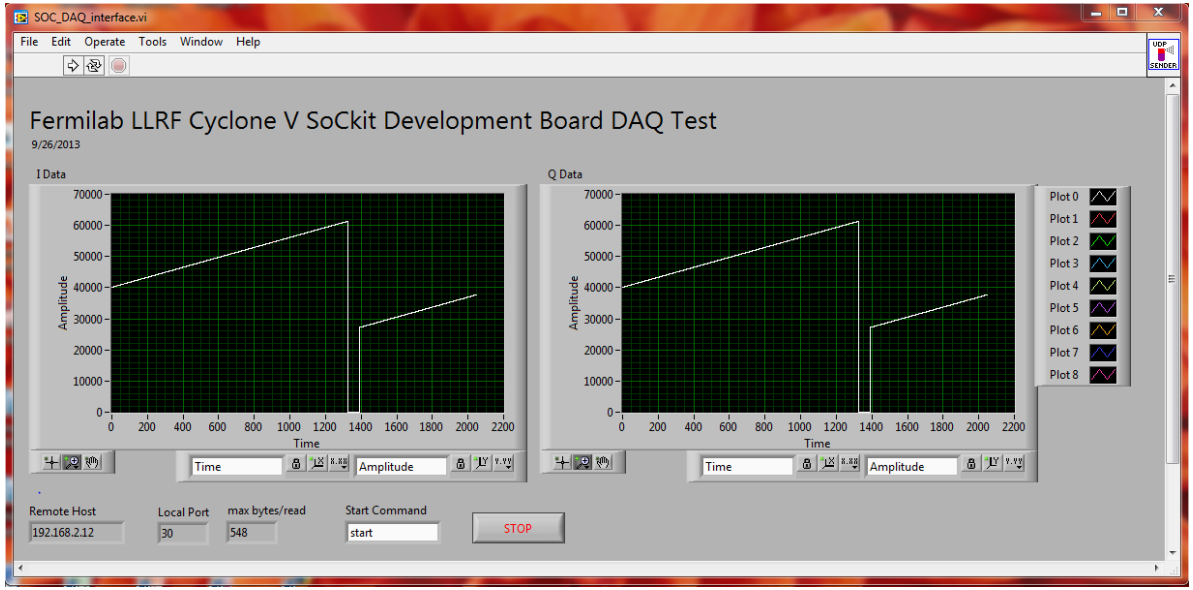
HARDWARE TRIGGER

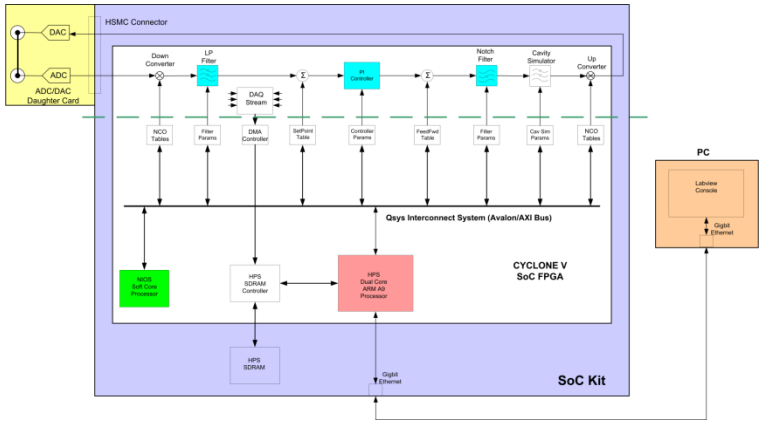
EXECUTION STOP



SW TRACE TRIGGER!

Console Output





SUMMARY

- SoC FPGA's offer the performance of application class processors with high bandwidth connections to the FPGA.

- A set of high level design and debugging tools provide the opportunity to develop complex systems with reduced development time and easier troubleshooting.

- Regardless of the choice of crate standard SoC FPGA's should help reduce system costs as there is less of a need for a CPU card.

- Board designs without external processors should simplify architecture while offering higher performance

Thank You !