

TEQnovations, LLC
Innovation in Electronics

Realizing the Potential of High-Performance Data Converters

Low Level RF 13 Workshop
Lake Tahoe, CA
October 1 – 4, 2013

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With comments from
Donald L. Herman, Jr., LSI, and
Michael J. Hoskins, PhD, Hittite Microwave

Agenda

- **Data Sheet and Reference Design Information**
- **Power and Ground Strategies**
- **Analog/RF Signal/Data Paths**
- **Sampling Clock Considerations**
- **Direct Conversion Considerations**
- **Performance Measures**
- **Summary**
- **Questions**

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DATA SHEET AND REFERENCE DESIGN INFORMATION

Reference Design

Marjorie Plisch, Jim Brinkhurst

TI Designs High Speed: Verified Design Schematic and Layout Recommendations for the GSPS ADC



TI Designs High Speed

TI Designs High Speed designs are analog solutions created by TI's analog experts. Verified Designs offer the theory, part selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

[Design Zip File](#)

[ADC10D1000](#)

[ADC10D1500](#)

[ADC12D1000](#)

[ADC12D1600](#)

[ADC12D1800](#)

[ADC12D500RF](#)

[ADC12D800RF](#)

[ADC12D1000RF](#)

[ADC12D1600RF](#)

[ADC12D1800RF](#)

Simulations, PCB, Gerber, BOM

Product Folder

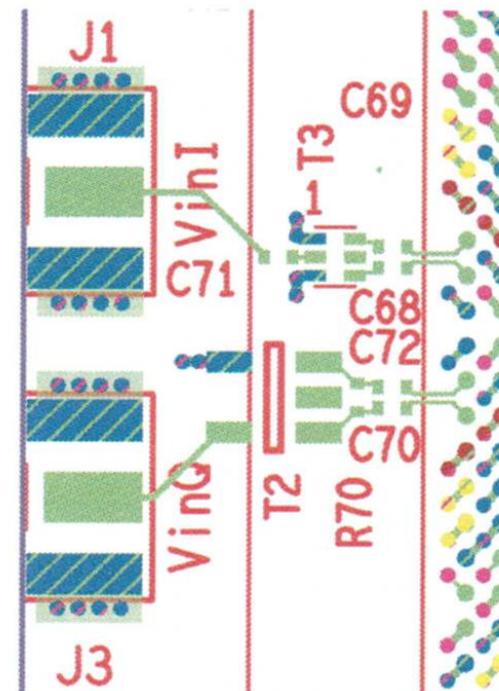
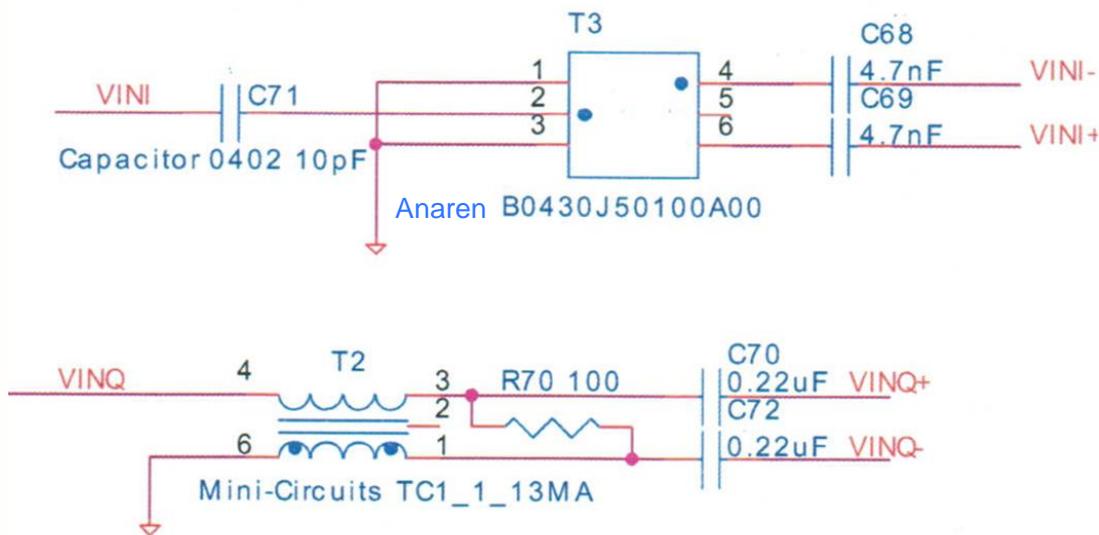
Design Description

This reference design is a guide to the schematics and layout for the system designer using a GSPS ADC in their system. Use this reference design along with the datasheet — the datasheet is always the final authority. Also, the ADC1xDxxxx(RF)RB Reference Board provides a useful reference design. All design source files for the Reference Board as well as the CAD/CAE symbols for the ADC are available on the product web page for download. For the purpose of this document, *ADC* or *GSPS ADC* refers to the ADC12D1800RF, ADC12D1600RF, ADC12D1000RF, ADC12D800RF, ADC12D500RF, ADC12D1800, ADC12D1600, ADC12D1000, ADC10D1500, ADC10D1000, ADC12D1600QML, and ADC10D1000QML.



[ASK Our Analog Experts](#)
[WebBench Calculator Tools](#)
[TI Designs Precision Library](#)

Recommended Components



Example Balun Circuits for Analog Inputs

From "Schematic and Layout Recommendations For the GPS ADC", TI/National Semi., April 2013

Detailed Information

Design Resources

[Design Zip File](#)

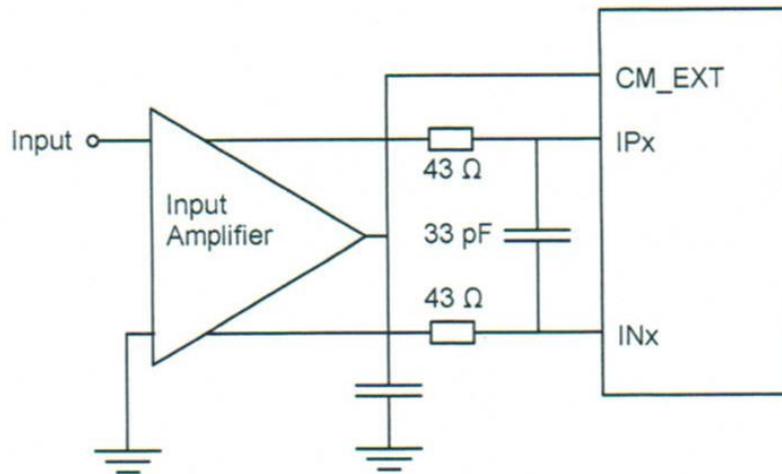
Simulations, PCB, Gerber, BOM

From "Schematic and Layout Recommendations
For the GSPS ADC", TI/National Semi., April 2013

Required Components

HMCAD1520

**HIGH SPEED MULTI-MODE 8/12/14-BIT
1000/640/105 MSPS A/D CONVERTER**



From "HMCAD1520" Data Sheet",
Hittite Microwave,



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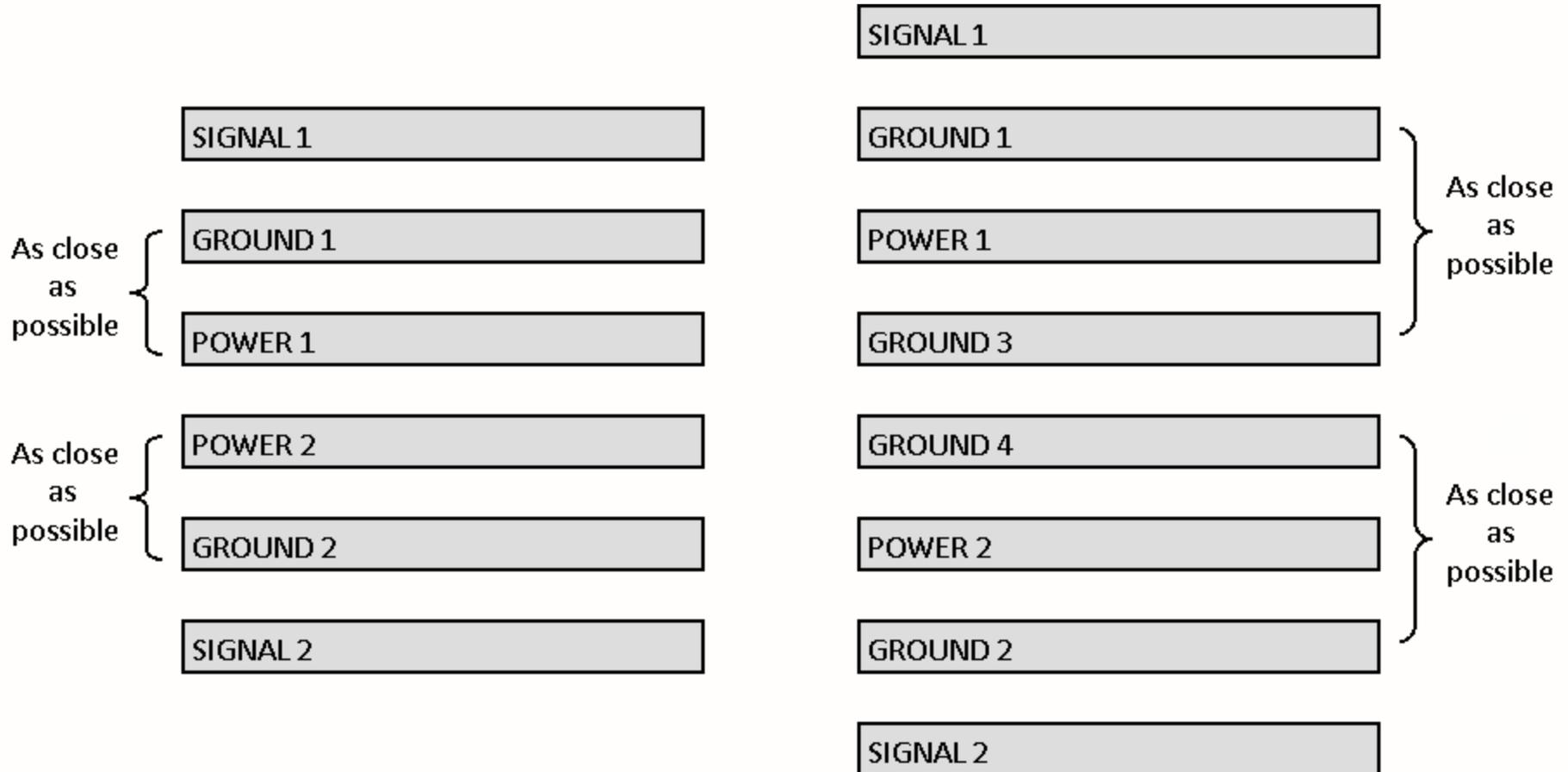


**POWER AND GROUND
STRATEGIES**

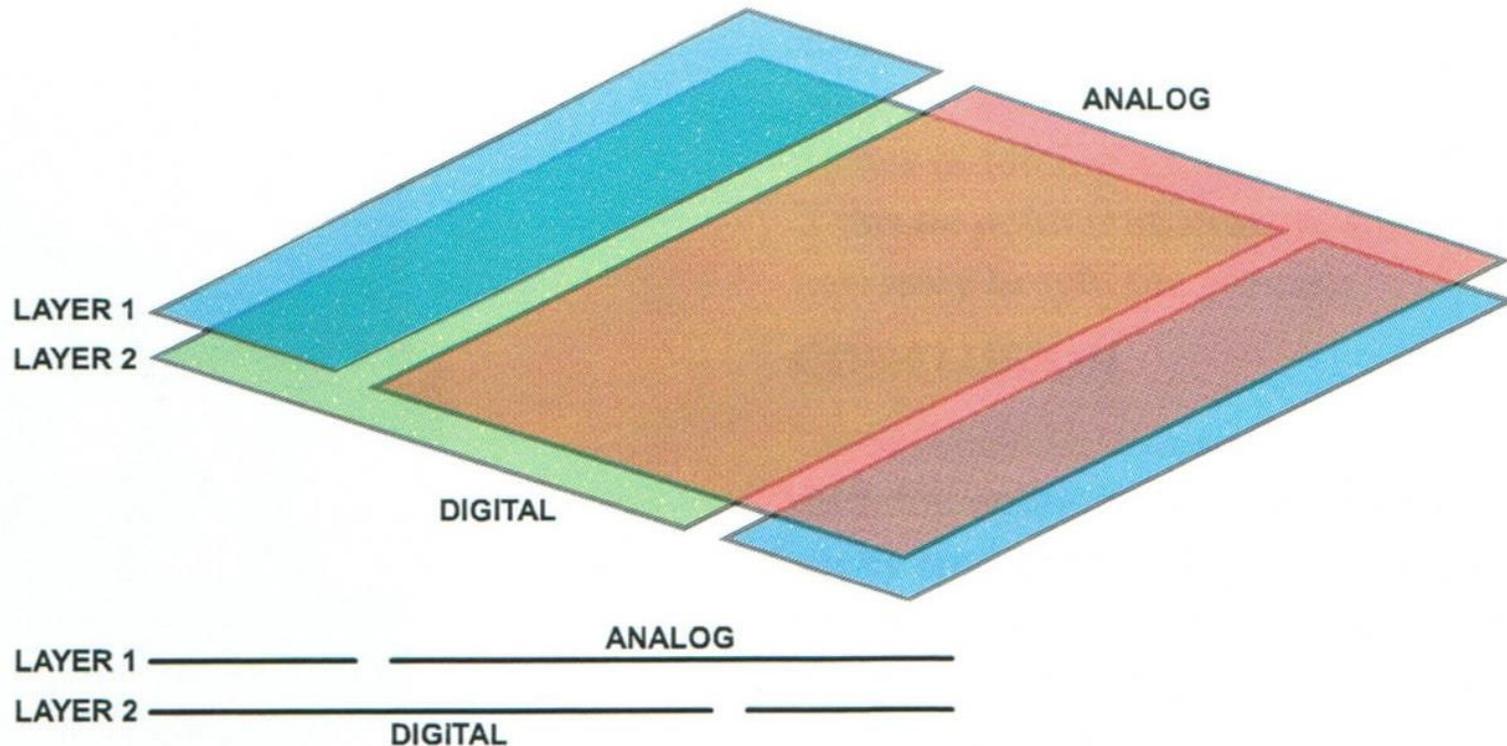
October 2013

LLRF 13 Workshop

Low-Impedance => Planes



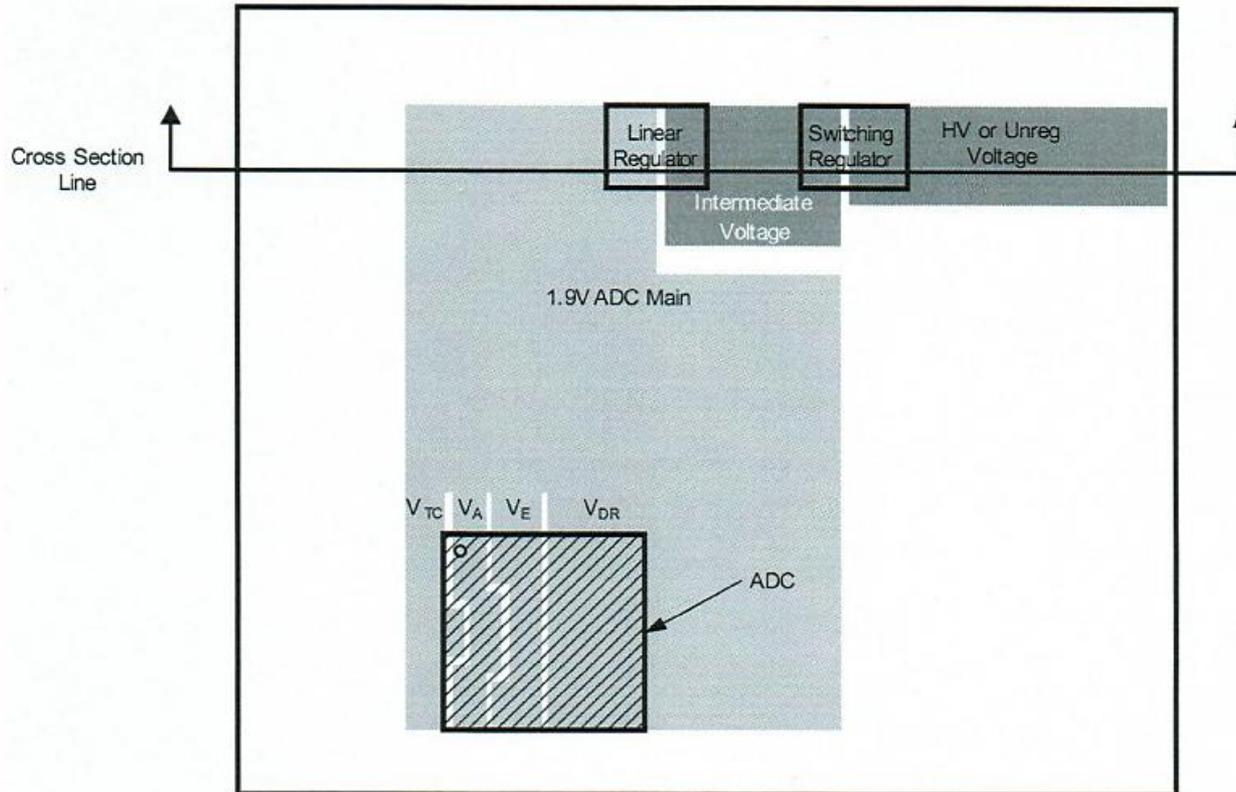
Avoid Inadvertent Coupling Between Planes



Applies to *all* planes!

From “Techniques for High Speed ADC PCB Layout”, AN-1142, Analog Devices,

Peninsulas in Power Plane



From "Schematic and Layout Recommendations For the GSPS ADC", TI/National Semi., April 2013

- **Bypass each peninsula individually**
- **Avoid necking power buses**
- **Avoid cheating ground/power planes**

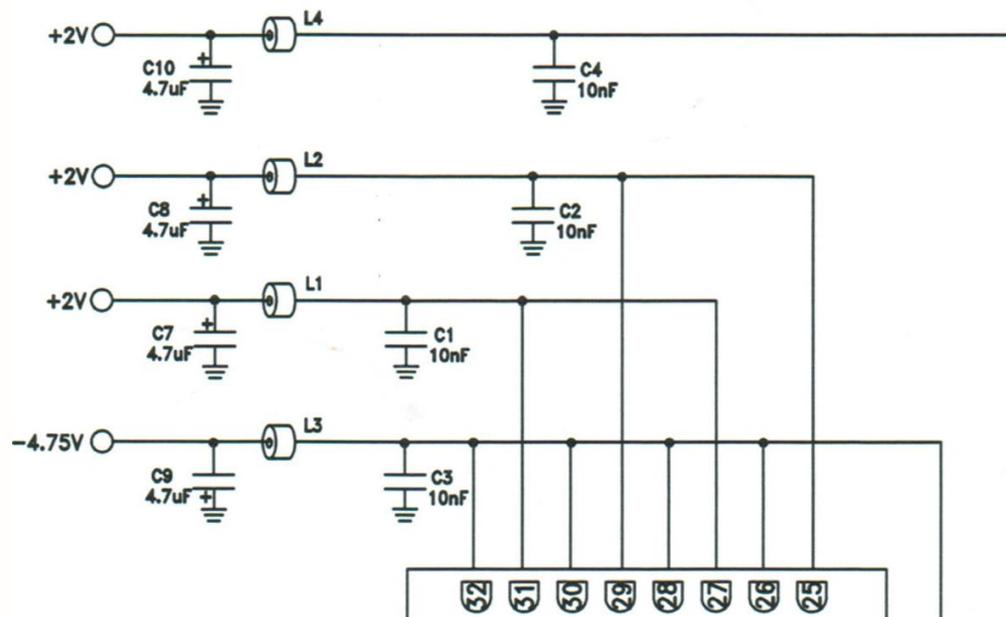
Bypassing

- **A large electrolytic capacitor (e.g., 10 μ F) where power supply connects to power plane**
 - Provides local charge reservoir for board
- **Smaller chip capacitors (e.g. 10 – 100 nF) at each IC**
 - Shorts high-frequency noise at IC
- **Connect decoupling capacitors to ground plane through vias or very short traces in ball field**
 - Minimizes inductance to ground
- **Measure resonances within capacitors and/or among parallel capacitors**
 - Insures that bypassing is capacitive, not inductive

All capacitors are not created equal!

Decoupling

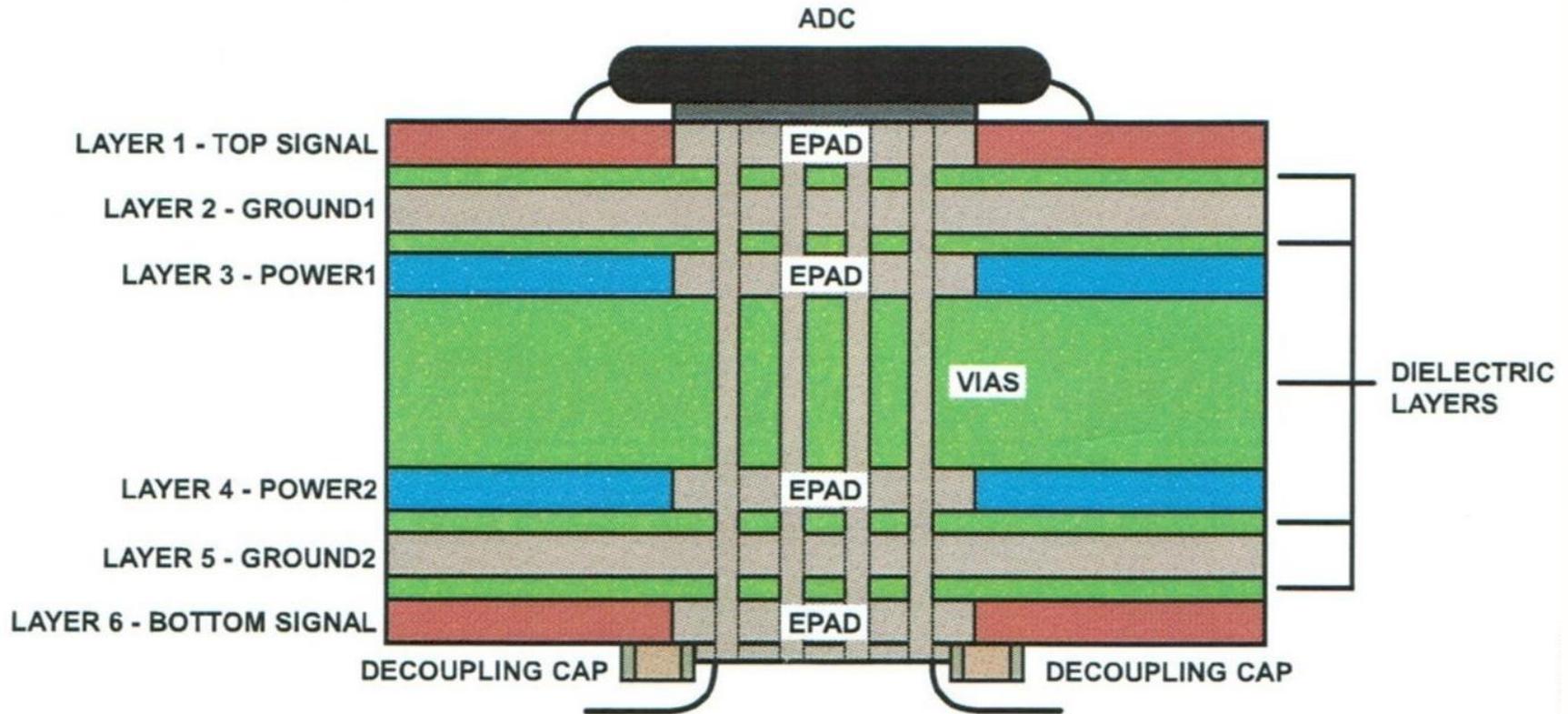
- **Place ferrite in supply line near IC to localize noise**



- Keeps external noise out of the IC
- Keeps internal noise generated within the IC from propagating to the rest of the system

From "HMC1061LC5" Data Sheet,
Hittite Microwave

Exposed Paddles (EPADs)



From "Techniques for High Speed ADC PCB Layout", AN-1142, Analog Devices,

October 2013

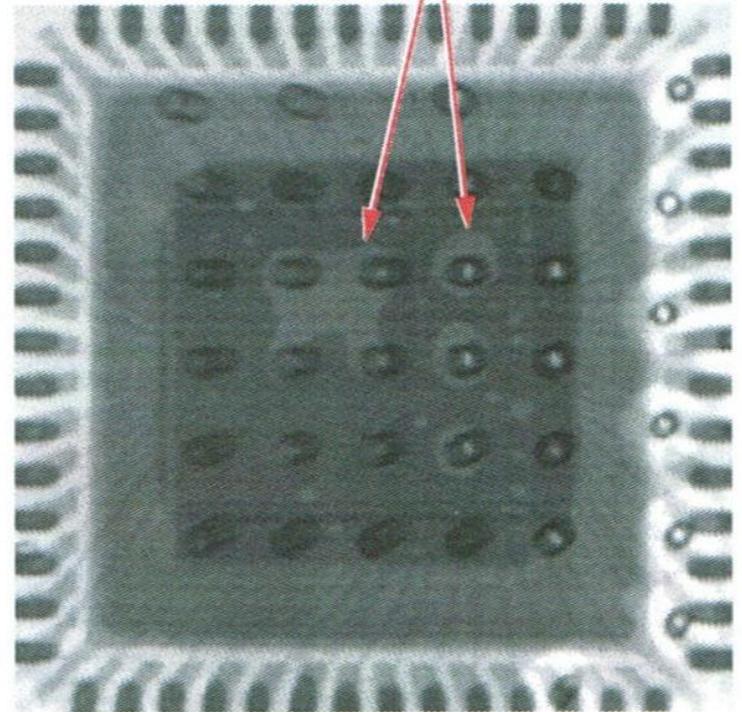
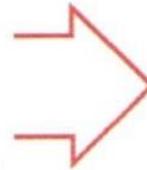
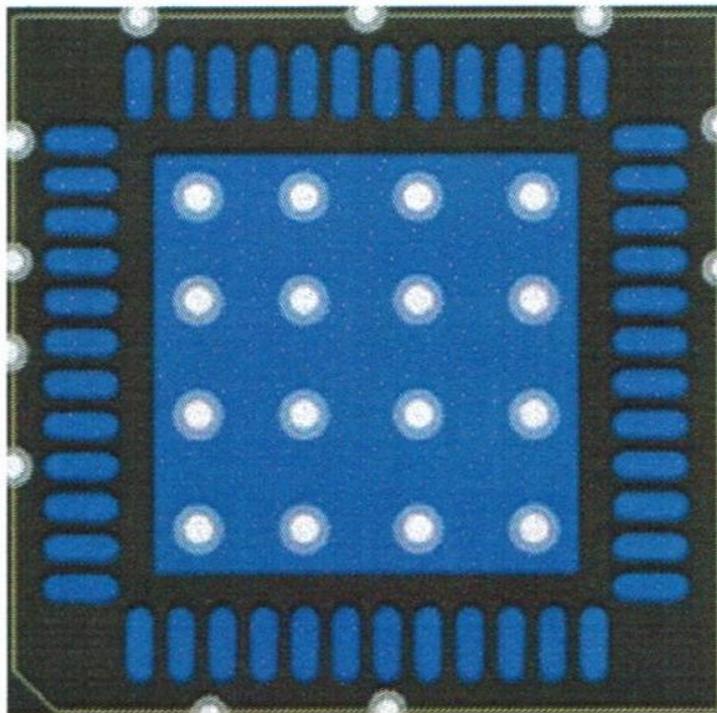
LLRF 13 Workshop

➤ **Massive ground connection and/or heat extraction path**

14

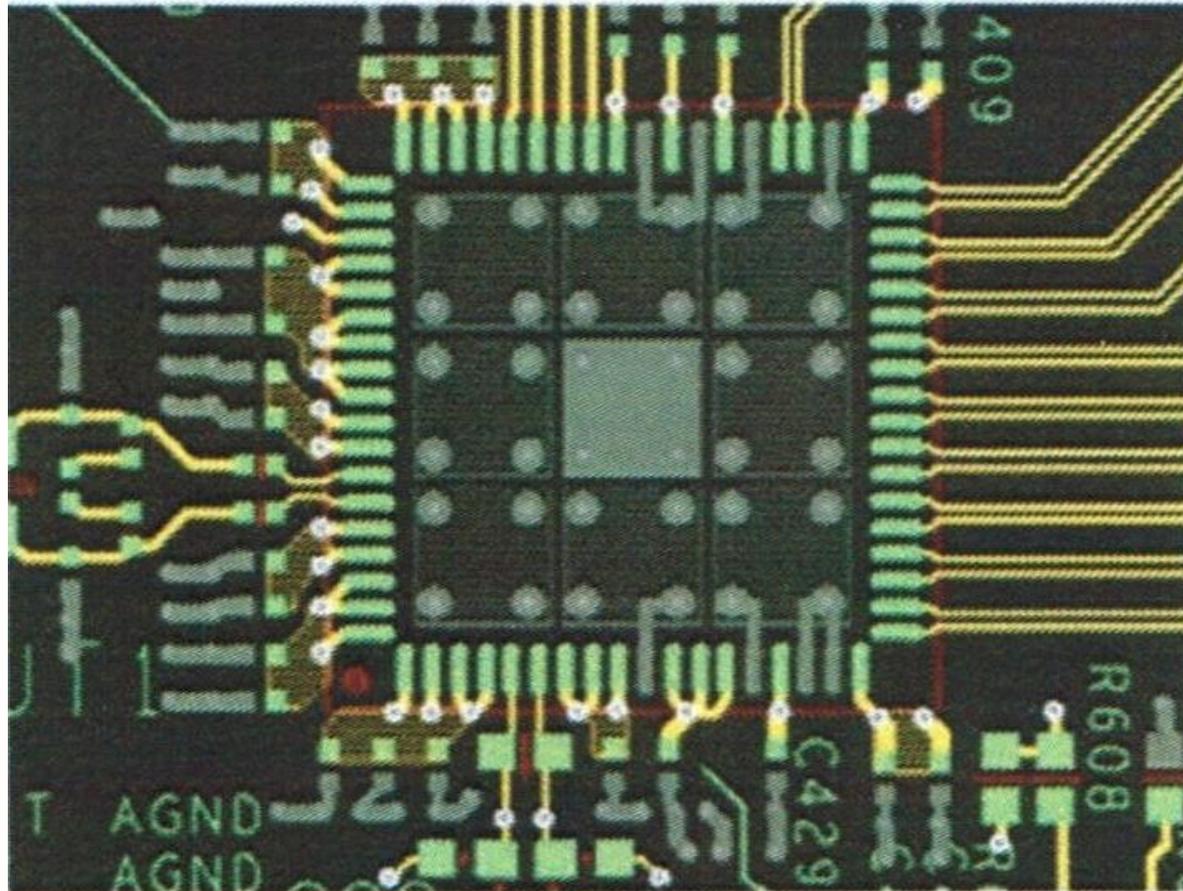
Poor EPAD Board Layout

NOTICE THE BUBBLES.



From "Schematic and Layout Recommendations for GPS ADC", SNAA206 – April 2013, TI / National Semiconductor.

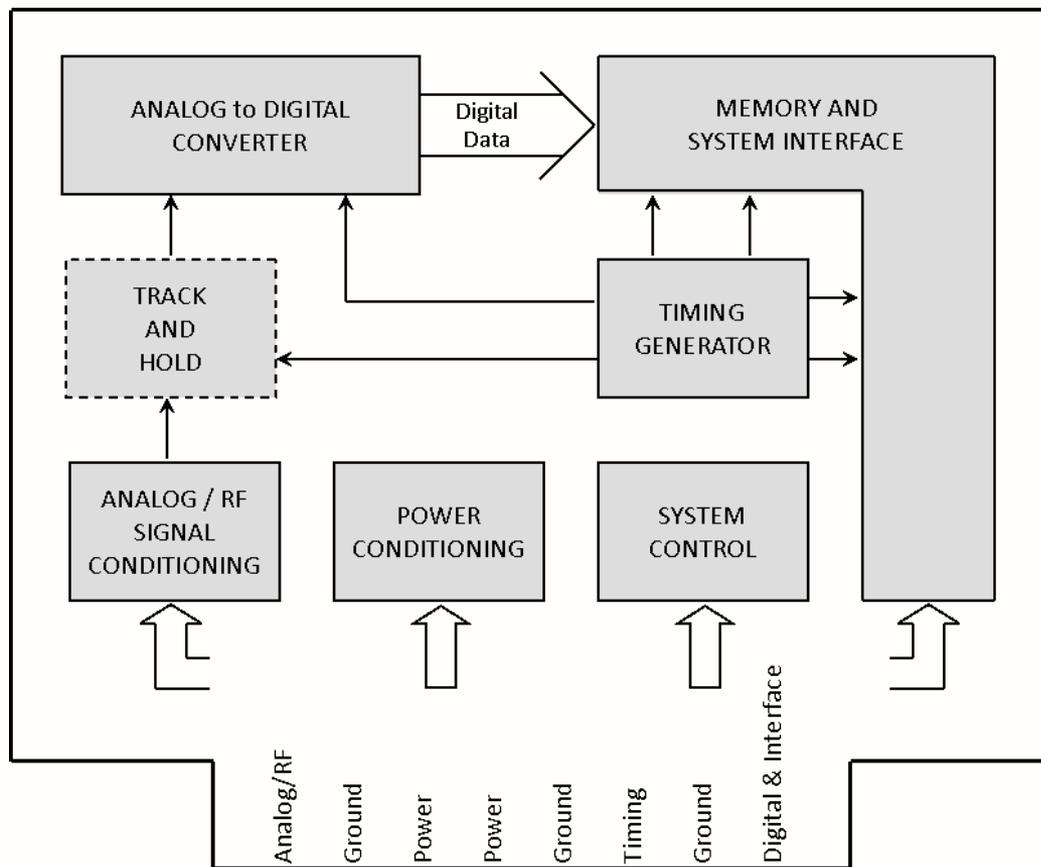
Good EPAD Board Layout



- Partition EPAD area into multiple smaller areas
- Fill vias to prevent wicking solder from beneath EPAD

From "Techniques for High Speed ADC PCB Layout", AN-1142, Analog Devices, October 2013

Place Components to Manage Return Currents



- Separate analog and digital currents
- Connect ground planes at a single point to avoid ground loops
- Isolate signal paths from clock paths to prevent cross modulation

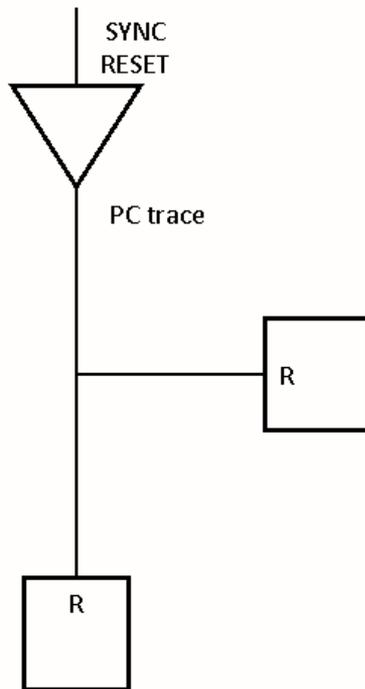
ANALOG/RF PATHS FOR SIGNAL, CLOCK, AND DIGITAL DATA

Analog and Digital RF Paths

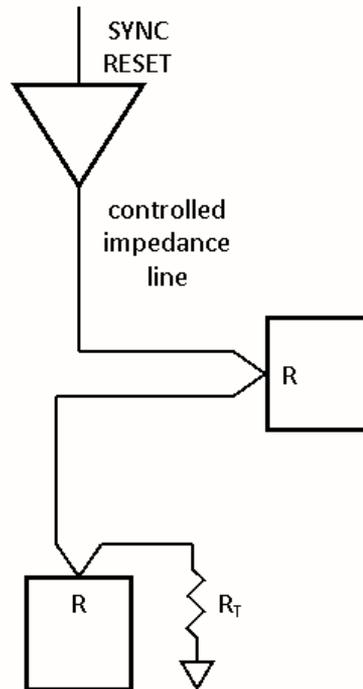
- **Path behaves as a transmission line if its length is > 1/40th wavelength of the fundamental frequency**
 - Minimize trace stubs and back-drill vias to minimize stubs
 - Keep stubs <1/10th wavelength of clock period
- **Rule of thumb: $F_{\text{fundamental}} = 0.3 / t_{r,f}$**
- **Square wave = fundamental plus odd harmonics**
 - Account for at least the 3rd harmonic
- **Increase line width and thickness to minimize resistive and inductive loss**
- **Choose appropriate dielectric to minimize dispersion**
- **Place path over quiet, continuous ground plane**

It's a Transmission Line! (whether *you* know it or not)

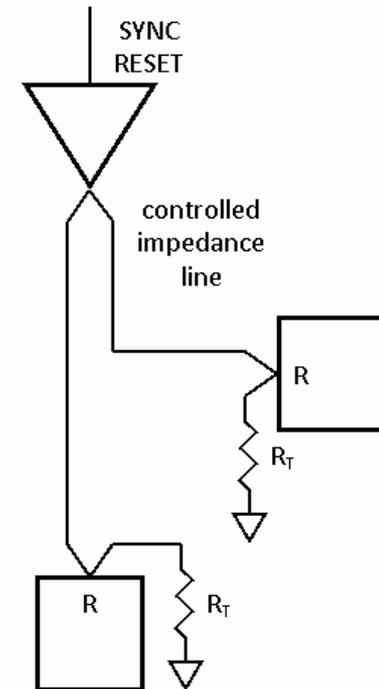
Bad



Better

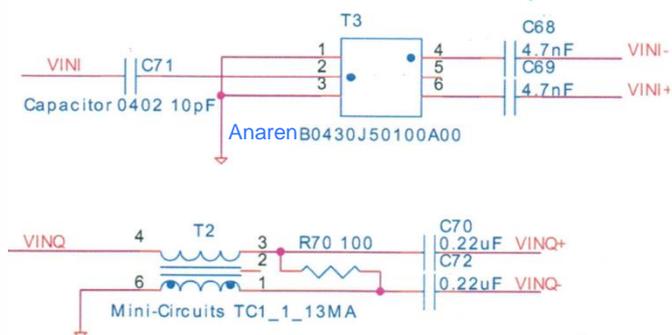


Best



Single-Ended to Differential Conversion

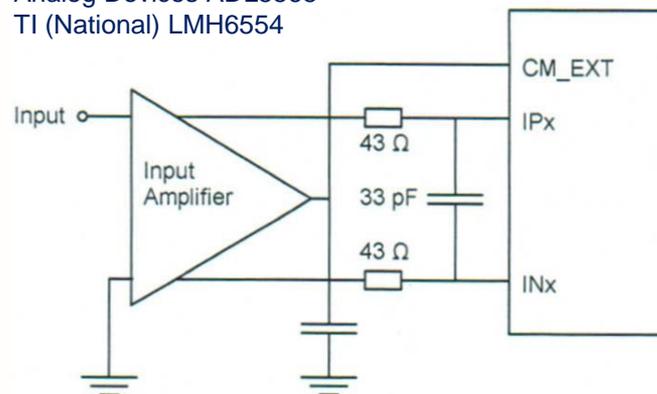
➤ Balun



From “Schematic and Layout Recommendations For the GSPS ADC”, TI/National Semi., April 2013

➤ Differential Amp

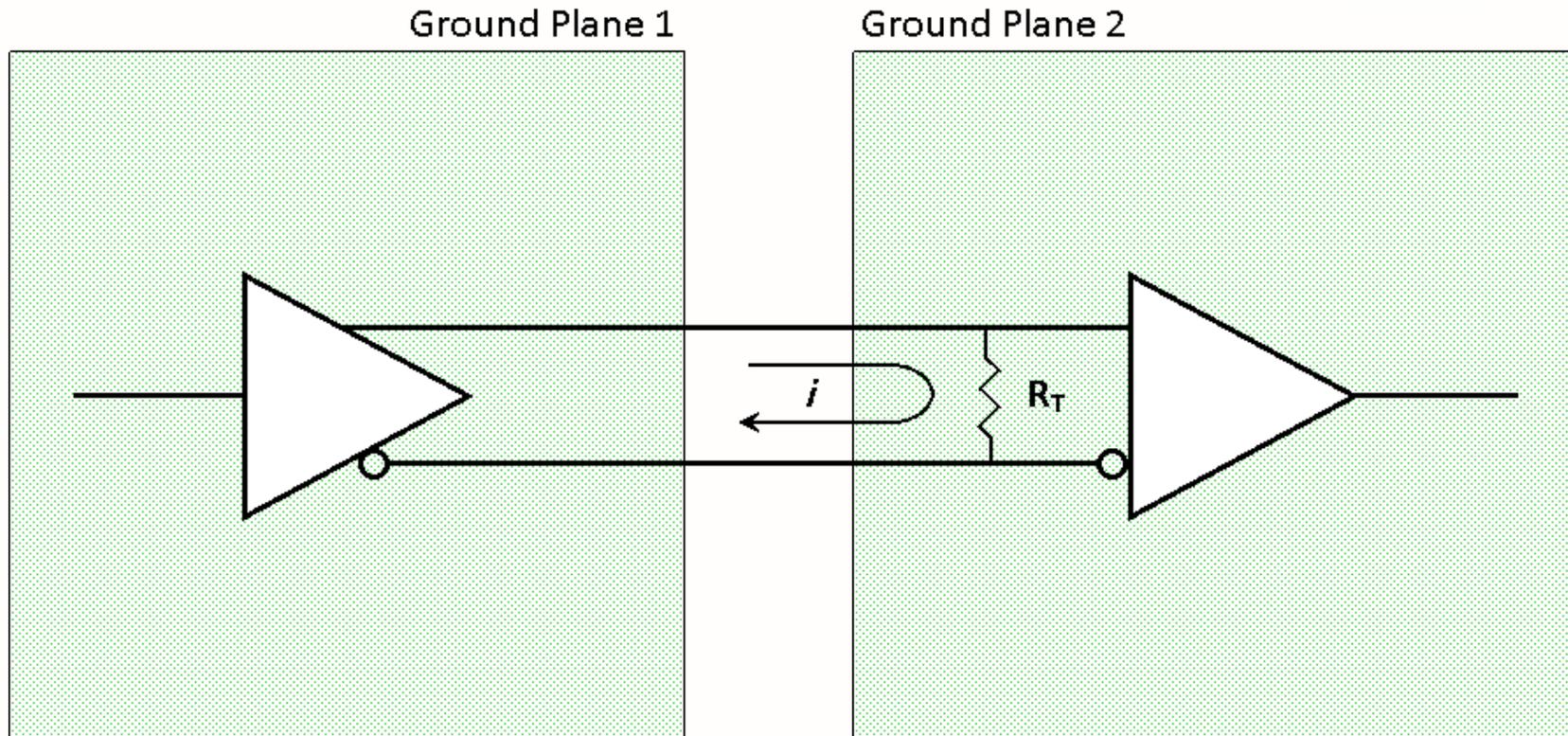
Analog Devices ADL5561
Analog Devices ADL5565
TI (National) LMH6554



From “HMCAD1520” Data Sheet”, Hittite Microwave,

- **Buffer (or filter) may be required to mitigate kick back**
- **Place in-line component close to end of transmission line**
- **Shadow (i.e. clear ground) pads of in-line components**

Differential Signaling Preferred for Digital Paths



- No return current in ground plane!
- Minimize ground-to-ground gap
- Maximize symmetry near paths

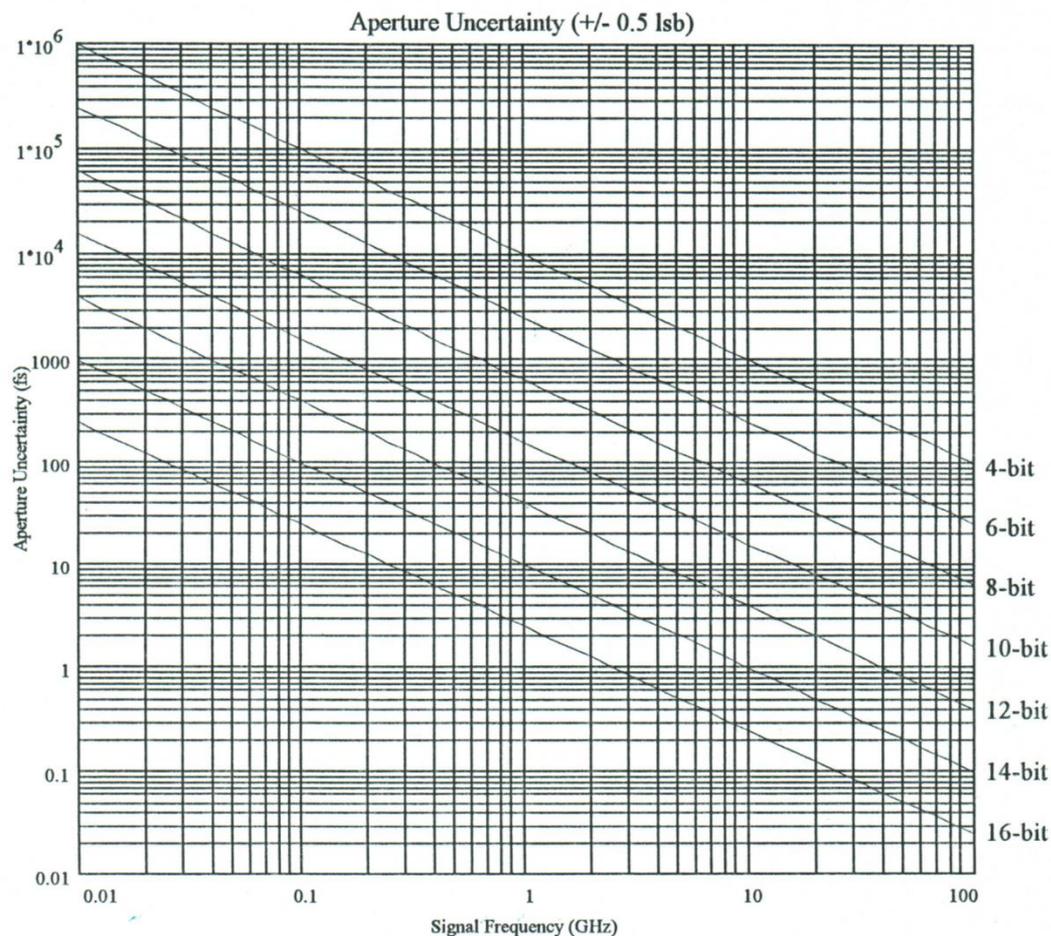
Differential Data Paths

- **ECL / CML / LVPECL / HCSL**
- **LVDS**
- **SERDES**
 - 8b/10b Encoding
 - Embedded clock
- **JESD204B***
 - 8b / 10b Encoding
 - Embedded Clock
 - Multiple, Synchronized Lanes
 - Rates up to 12.5 Gb/s (10 Gb/s data)

* From "What is JESD204 and Why Should We Pay Attention to it?",
MS-2374, Analog Devices

SAMPLING CLOCK CONSIDERATIONS

Jitter versus Signal Frequency



- Jitter is independent of sampling rate
- Applies to carrier + signal
- Graph shows worst-case jitter
- Error is proportional to slew rate
- $t_{r,f} = 0.3 / f_{\text{signal}}$
- Two basic types
 - Random
 - Deterministic
- Impact of jitter is complex

Two Types of Sampling Clocks

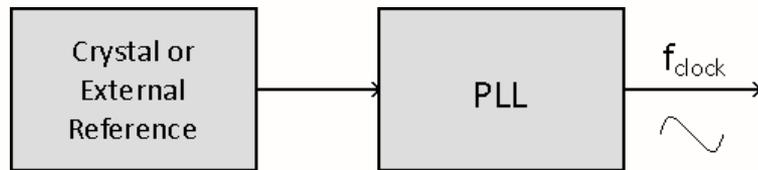
➤ Square wave

- For lower sampling rate converters
- $t_{r,f}$ of about 15 ps
- Random jitter of about 200 fs
- Deterministic jitter of about 2 ps
 - Matters if both edges of clock are critical
- Caution: high frequency content in edge!

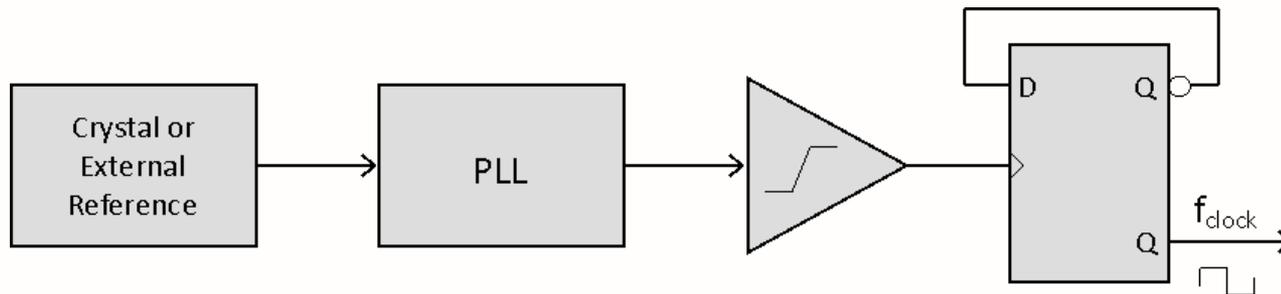
➤ Sine wave

- For most higher sampling rate converters
- Band-pass filter phase noise
- No higher frequency components

Local Clock Sampling Generation



➤ **Sine wave**



➤ **Square wave**

DIRECT CONVERSION CONSIDERATIONS

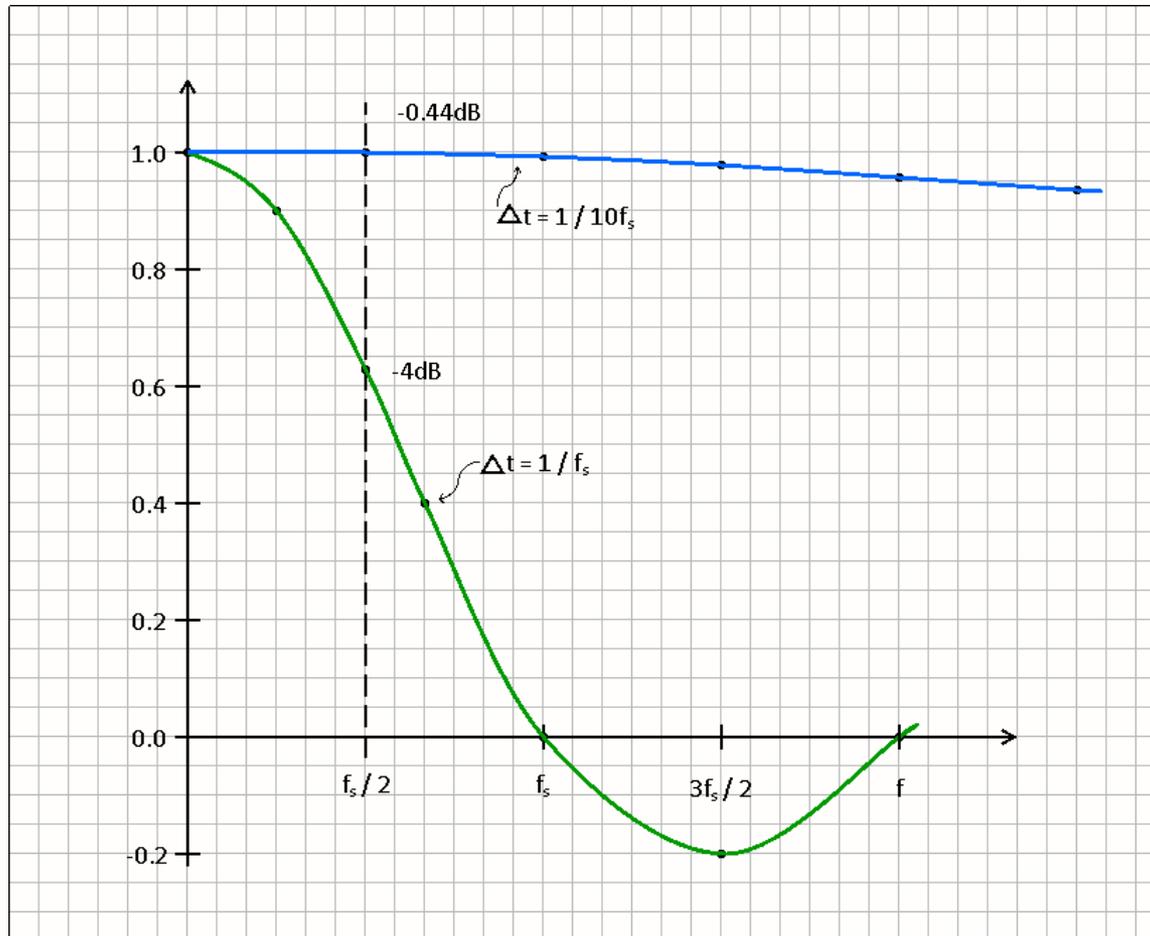
Direct Conversion Requirements

➤ Adequate analog bandwidth for signal at RF frequency

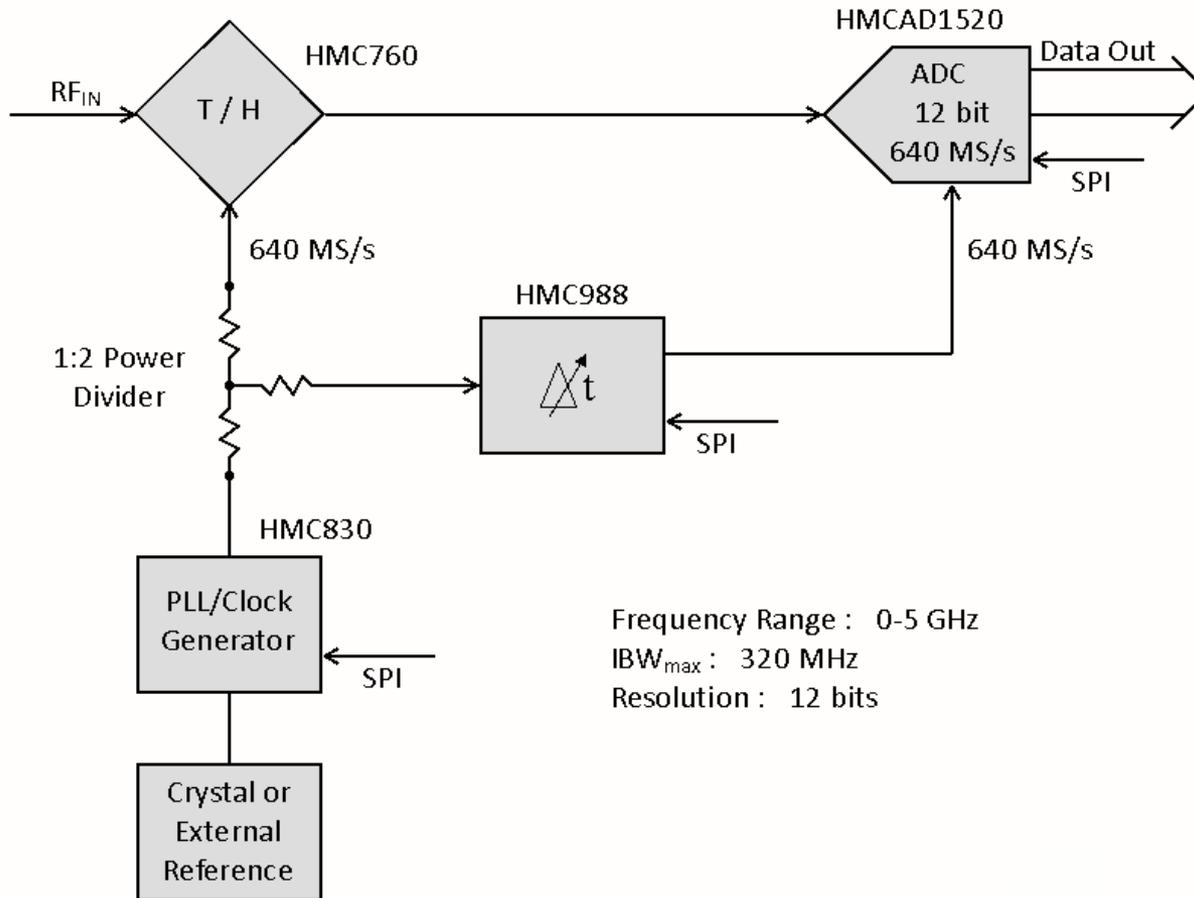
and

➤ Sufficiently small sampling aperture to accommodate (RF + signal) frequency

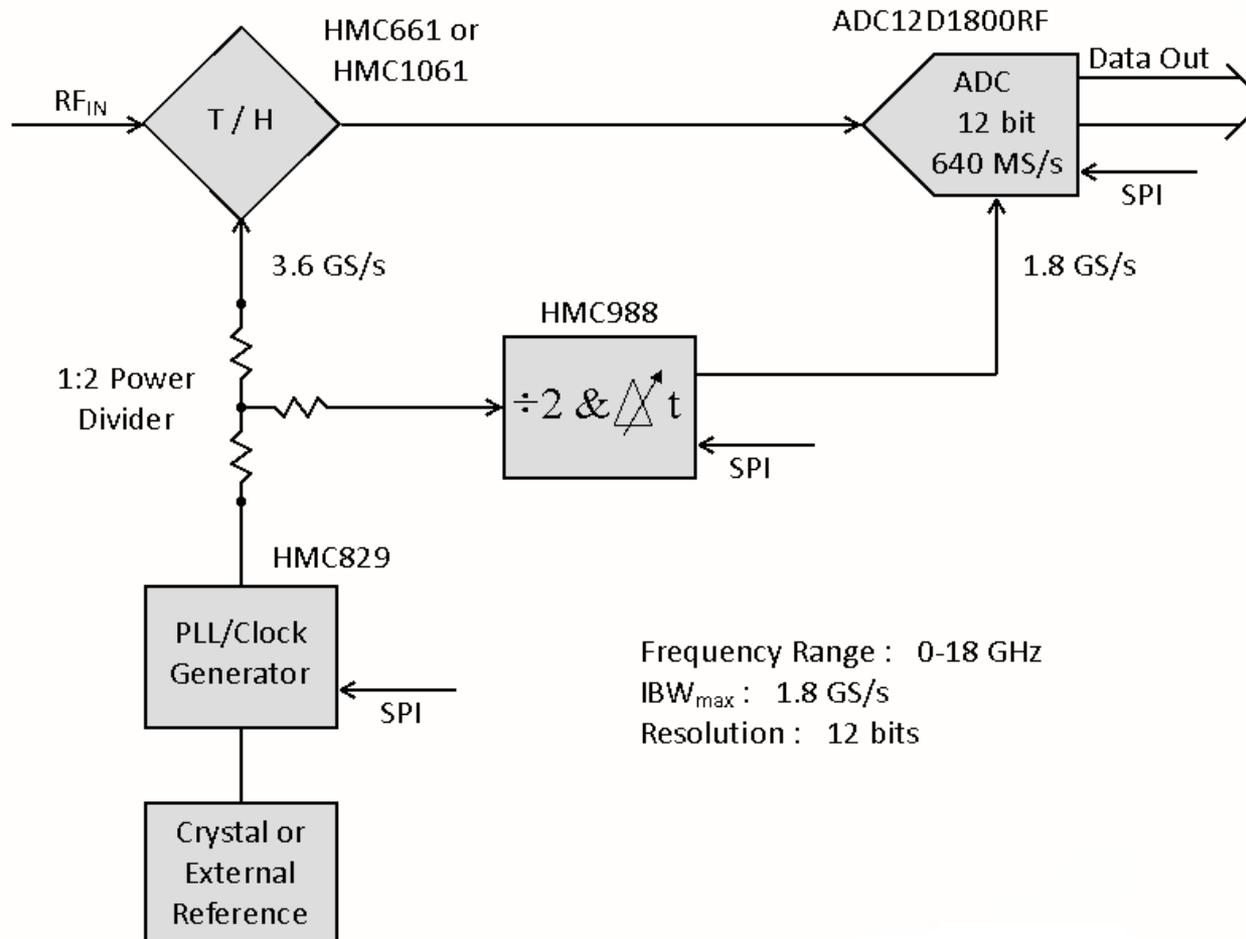
Sampling-Aperture Bandwidth



Wide-BW Direct Down Converter

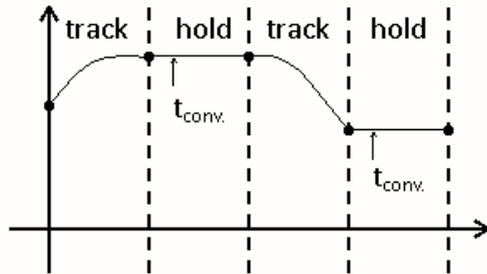


Wider-BW Direct Down Converter

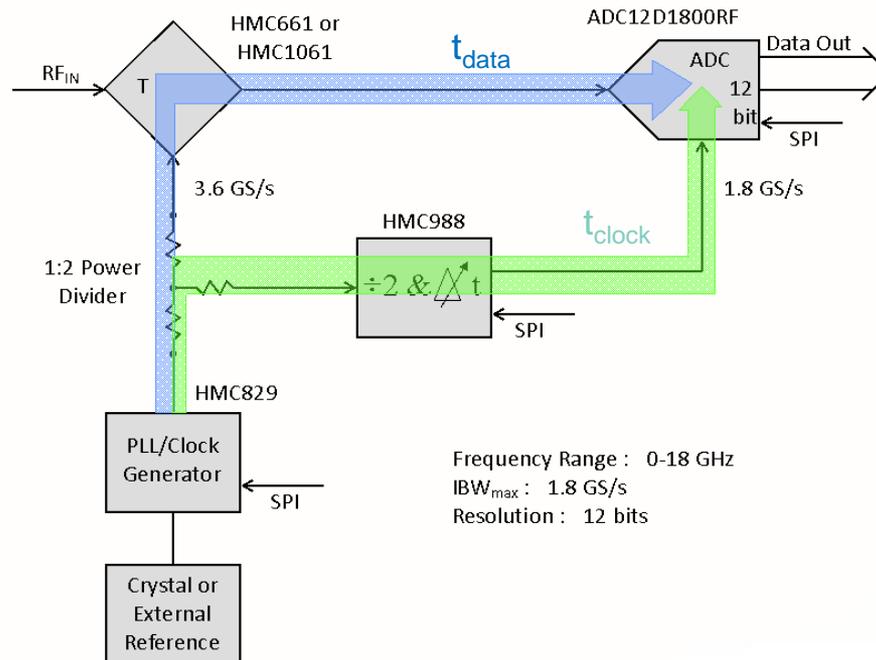


Frequency Range : 0-18 GHz
 IBW_{max} : 1.8 GS/s
 Resolution : 12 bits

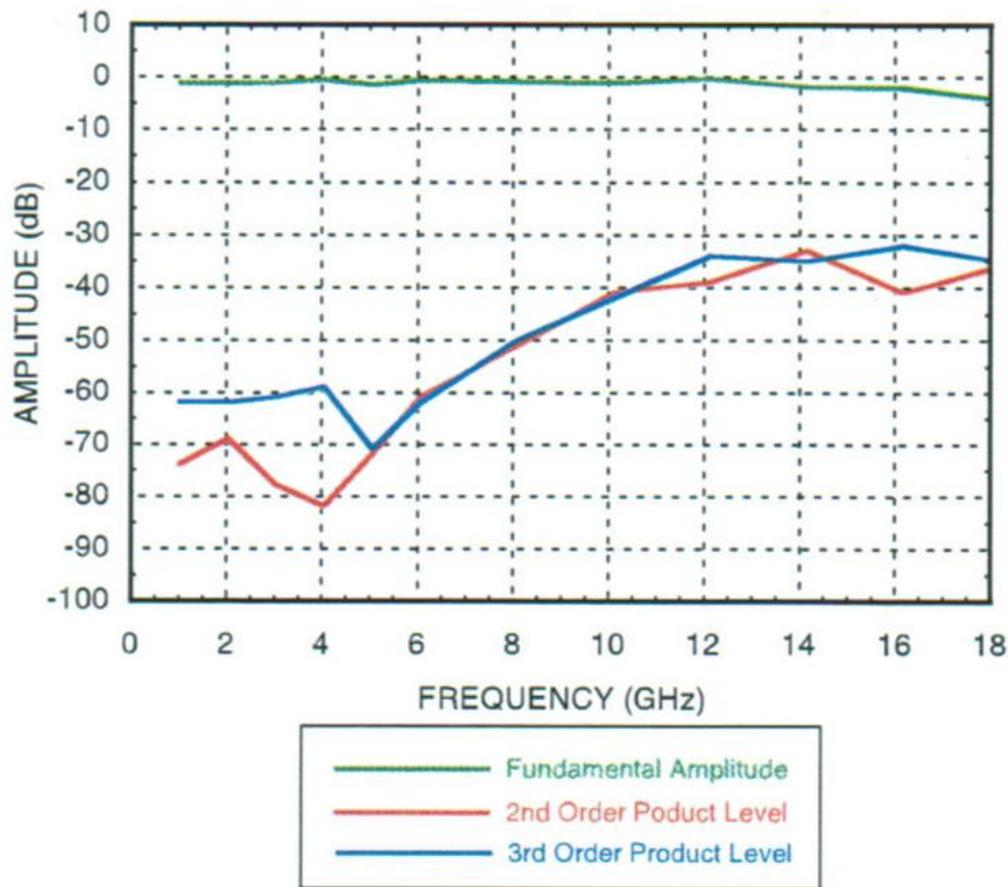
Timing Criteria



$t_{clock} = t_{data} + \Delta t_{data}$
such that $t_{convert}$
is stable regardless of f_s



Down Conversion Performance



- Hittite HMC 1061LC5 T/H
- TI ADC12D1600 ADC
- Clocked at 1 GS/s
- Data includes both harmonic distortion *and* intermodulation distortion
- 3rd-order intermodulation products are in-band

From "HMC1061LC5" Data Sheet,
Hittite Microwave

Mixer + LO versus Track/Hold

➤ Mixer + LO

- Narrow Converted Bandwidth
- Higher Linearity in Narrow Bandwidth
- Lower Noise
 - Integrated over pass band
- Requires LO + ADC Clock
- Produces mixer products
 - Can alias if not filtered before ADC
- Complex frequency change
 - Change LO frequency
 - Change mixer *analog* filters
 - Limited number of filters
 - Switching filter can cause glitches
 - Multiple filters are bulky and expensive
 - May drift with time, temperature

➤ Track/Hold

- Wide Converted Bandwidth
- Modest Linearity over Wide Bandwidth
- Higher Noise
 - Integrated over full T/H bandwidth
- Requires only the ADC Clock
- Produces aliases of signal
 - Requires anti-aliasing filter before T/H
- Simple frequency change
 - No change, or
 - Change band-select filter
 - Acquire wide frequency band, then filter *digitally*
 - Flexible, programmable
 - Small and inexpensive
 - Stable



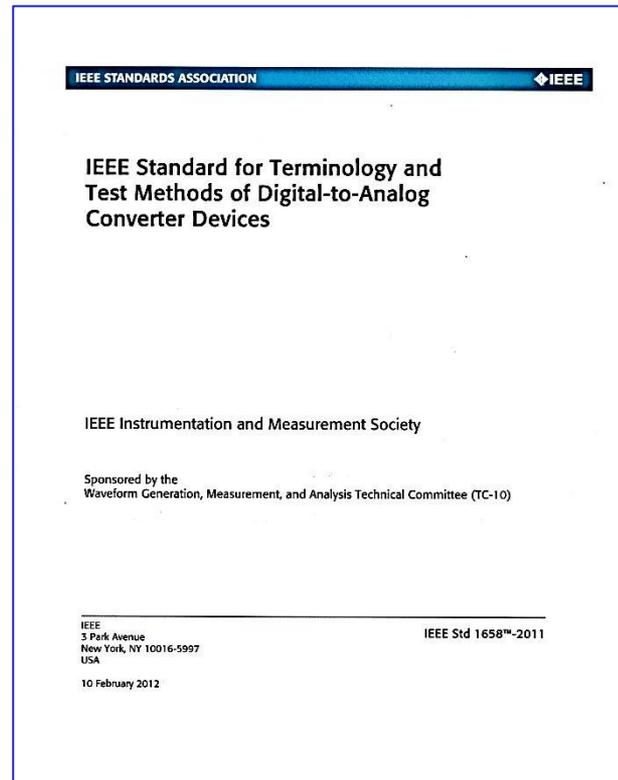
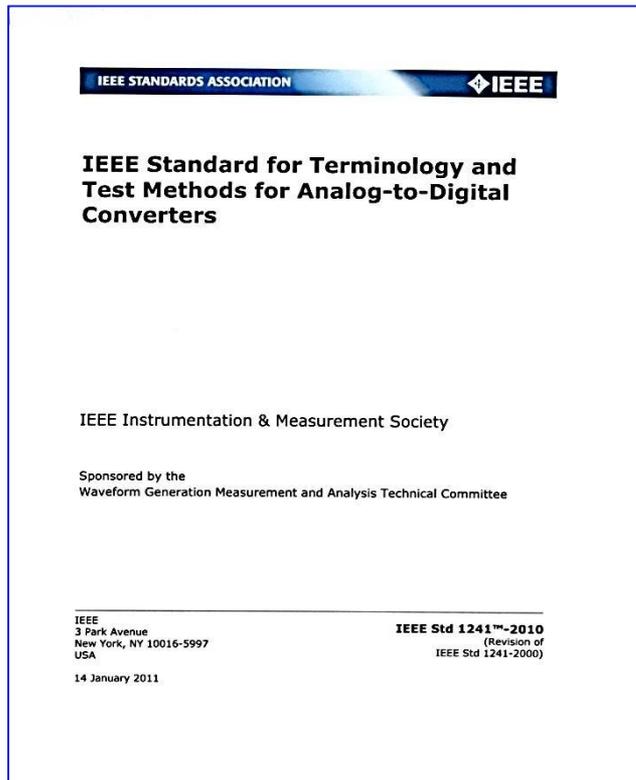
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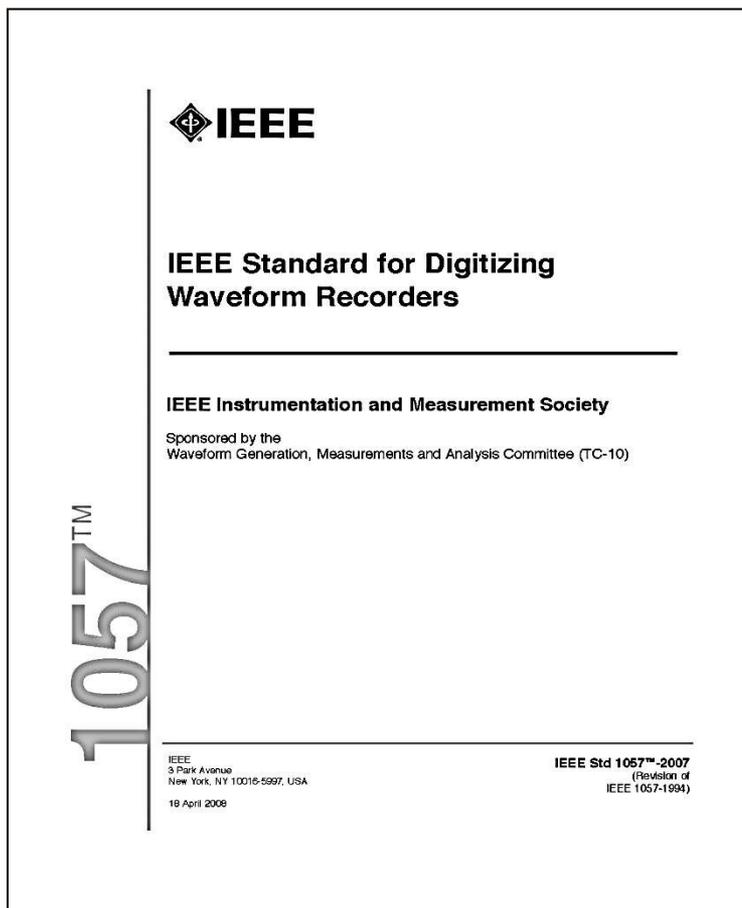
PERFORMANCE MEASURES

IEEE Standards for ADC and DAC Terminology and Test Methods

- IEEE Std 1241-2010 for ADCs
- IEEE Std 1658-2011 for DACs



IEEE Standard for Digitizing Waveform Recorders



- Last revised in 2007
- New revision in progress now
 - Incorporate terms and test methods from latest ADC standard
 - Develop and incorporate new material
 - **We could use your help!**

Proposed IEEE Standard on Jitter

- Impact on mixed-signal circuits
(e.g., ADC, DAC, etc.)
- Impact on digital data communications
- **We could use your help!**

The logo for TEQnovations, LLC features the word "TEQ" in a large, bold, blue sans-serif font, followed by "novations, LLC" in a smaller, grey sans-serif font. Below the logo is the tagline "Innovation in Electronics" in a grey sans-serif font. The background of the slide is a complex, abstract digital graphic with blue and teal tones, featuring circuit-like lines, glowing nodes, and circular patterns that suggest a high-tech or electronic theme.

TEQnovations, LLC

Innovation in Electronics

SUMMARY

Summary

- **Data Sheet and Reference Design Information**
 - Use to your advantage
- **Power and Ground Strategies**
 - Use planes; bypass/decouple carefully
- **Analog/RF Signal/Data Paths**
 - Design for real RF content; manage return currents
- **Sampling Clock Considerations**
 - Consider local generation; manage jitter
- **Direct Conversion Considerations**
 - Use to simplify system if performance is adequate
- **Performance Measures**
 - Use IEEE standards for terms and test methods

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TEQnovations, LLC

Innovation in Electronics

QUESTIONS ?



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