eRD25: Silicon Tracking and Vertexing Consortium

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What is this about? A continuation and next phase in our participation in the nationally administered EIC generic detector R&D program.

Current goal? Develop a well-integrated and large-acceptance EIC vertex and tracking detector concept, based on Monolithic Active Pixel Sensor (MAPS) at the 65 nm node.

Brief history:

eRD25 grew out of eRD16 (LBL) and eRD18 (Birmingham) over the past ~6 months:

The former eRD16 initially focused mostly on forward/backward charged particle tracking with disks using MAPS - much of the work was done by B.Jacak, Y.S.Lai, E.S. with UCB undergraduates,

The former eRD18 initially focused on central vertexing with MAPS barrels, and sensor development (Depleted MAPS)

eRD16 and eRD18 increasingly worked together over the years; barrel and disks are closely related, mutual technical interests,

- For example, Håkan Wennlöf (eRD18) was first to study the optimal positioning of the innermost disk w.r.t. the innermost barrel vertex layers,
- Yue-Shi Lai and E.S. originated the first EIC all-silicon tracking concept,
- Leo Greiner (eRD16) initiated the group's effort with ITS3 sensor R&D

Both groups studied integrated tracking and vertexing concepts, hybrid TPC+silicon, as well as the first all-silicon concepts for EIC.

Progress Report and Proposal (paraphrased):

eRD16 and eRD18 see their previously proposed work as substantially complete, have are integrated in the ongoing EICUG Yellow-Report effort; **ready for the next stage: eRD25.**

Goal: Develop a well-integrated and large-acceptance EIC vertex and tracking detector concept, based on Monolithic Active Pixel Sensor (MAPS) at the 65 nm node.

The **Motivation** for a high-resolution, low-mass, large-acceptance charged particle tracker remains as ever: EIC science requires it.

Context: our prior work, reflected e.g. in the EIC detector R&D handbook, shows that none of the existing MAPS sensors appear to meet all EIC needs at once. The development of a Monolithic Active Pixel Sensor specifically for EIC is thus highly desirable if not imperative. These conclusions met with consensus during the recent EICUG-YR Temple workshop.

FY21 eRD25 **proposal** to join and work within the ALICE ITS3 R&D collaboration to develop a new generation MAPS sensors in 65 nm CMOS imaging technology for EIC.

Previous eRD18 work had identified a recent development of a 180nm CMOS imaging process as a viable candidate for the design of an EIC MAPS with a number of “buts” and “ifs”.

ITS3 sensor development offers an attractive path going forward. They include:

- ~openness to parties outside of the ALICE collaboration or research scope,
- (large R&D) scale,
- 65 nm and process availability,
- improved performance,

Large overlap and significant differences, most notably size; the design of a wafer-scale sensor is (very) different from the design of a reticle-size sensor for the same specifications - the EIC development will need to fork off.

Proposal aims at laying the groundwork for this effort, e.g. through

- participation in the first submissions, starting (already) this Fall,
- performance characterization of the 1st submission at the 88” and the MC40,
- development of one or more complex intellectual property blocks,
- updated conceptual design and evaluation of (new) trade-offs, including svcs,
- physics simulation of DIS production of open-charm, combining electron measurement and displaced vertexing

From the close-out:

Since the time of the January review there has been considerable re-organization, convergences of activities, and the formation of new alliances and collaborations. All of this is very positive and the Committee acknowledges all these developments with enthusiasm.

Findings:

eRD25 has formed out of the union of eRD16 and eRD18. eRD25 is also advocating the formation of a larger EIC silicon consortium. New collaborations are being integrated.
…

eRD25 is joining with the ALICE ITS3 group to develop a new sensor based upon the 65nm TJ process. While many fundamental specifications for the ITS3 device meet or exceed those of the EIC, ITS3 targets specifically vertex layer and wafer scale devices. This matches with the EIC vertexing needs but there will also have to be an EIC specific development aimed at more traditional stave and disk layers at larger distances from the beamline.

eRD25 proposes to collaborate with ITS3 but also branch, in parallel, after the first test device fabrication run, to address EIC specific needs. …
…

An important part of the performance studies are now focusing on understanding, parametrizing, and simulating realistic services in the EIC tracker
…

Recommendations:

As activities develop, over the coming year, assess whether the planned EIC specific 65nm branch remains appropriate. This proposal should be funded at the appropriate level funding permitted and is enthusiastically supported by the Committee.

Waiting for the written report.