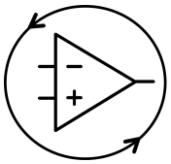

Cryogenic DAQs and FPGAs for Magnet Diagnostics

DIAGNOSTICS WORK GROUP
MEETING #4

Marcos Turqueti

06/12/2020

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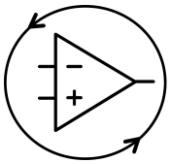

LBNL Activities

ATAP, Nuclear Sciences and Engineering

- Active Cryogenic Electronic Envelope (2013)
  U.S. Patent No. 10,240,875 (Supercon)
- Commercial off-the-shelf cryogenic components (4k-77k)
  ADCs, Amplifiers, Diodes, FPGAs, Laser Diodes, Optical Isolators , Voltage Regulators, Transistors and Passives
- Field Programmable Gate Array (FPGA) on Cryogenic Environments (first board 2015)
- FPGA operating with COTS ADC (LTC2418)
- FPGA based ADC
- Cryogenic Magnetic Sensors
  Acoustic Sensors (Maxim)
  Electron Beam Sensor (LDRD)
- 160nm Cryogenic ASIC (2018)
  16 channels 12b 10MSPS ADC, 1 MSPS 10b ADC, Charge Amplifier, Voltage Regulator, Strain Gauge, Sea-of-Transistors, Memory (C.Grace, D.Gnani)
- 3th Gen FPGA Test Board (2018)
- 4th Gen FPGA/DAQ (2019-2020) – LBNL –Fermilab/CD

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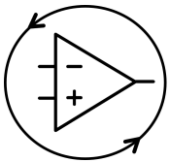

Motivation

Instrumentation of Cryogenic Experiments

- Data interface fully digital
- Simplification of cryostat feedthrough
- Noise reduction
- System simplification (no long analog cables present)
- Flexibility
- Cost reduction
- Increase time of oxide breakdown

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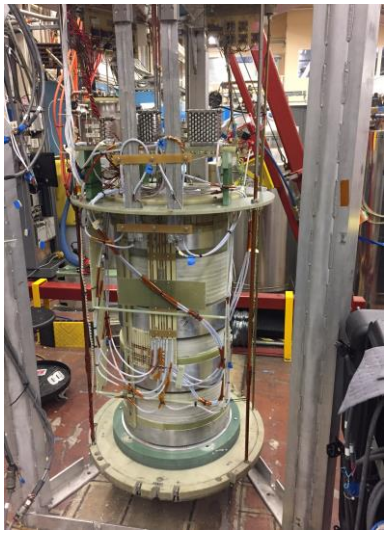
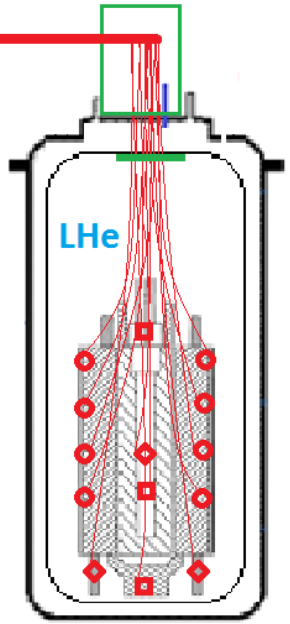
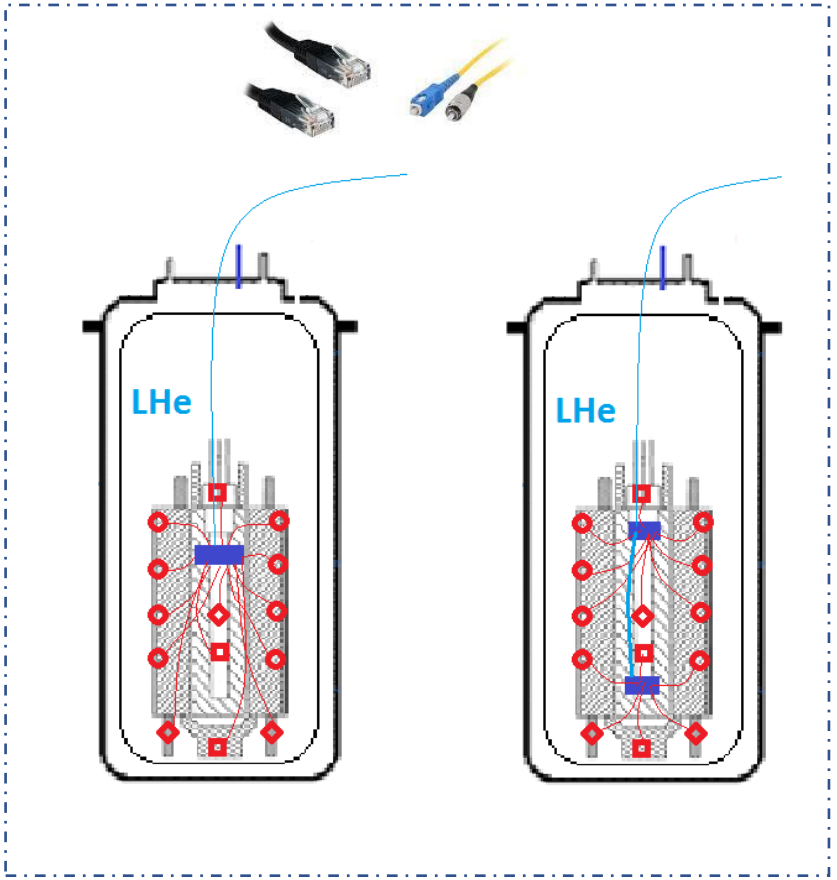
Data Acquisition for Magnet Diagnostics







- Strain Gauge
- Voltage Taps
- Temperature Sensor

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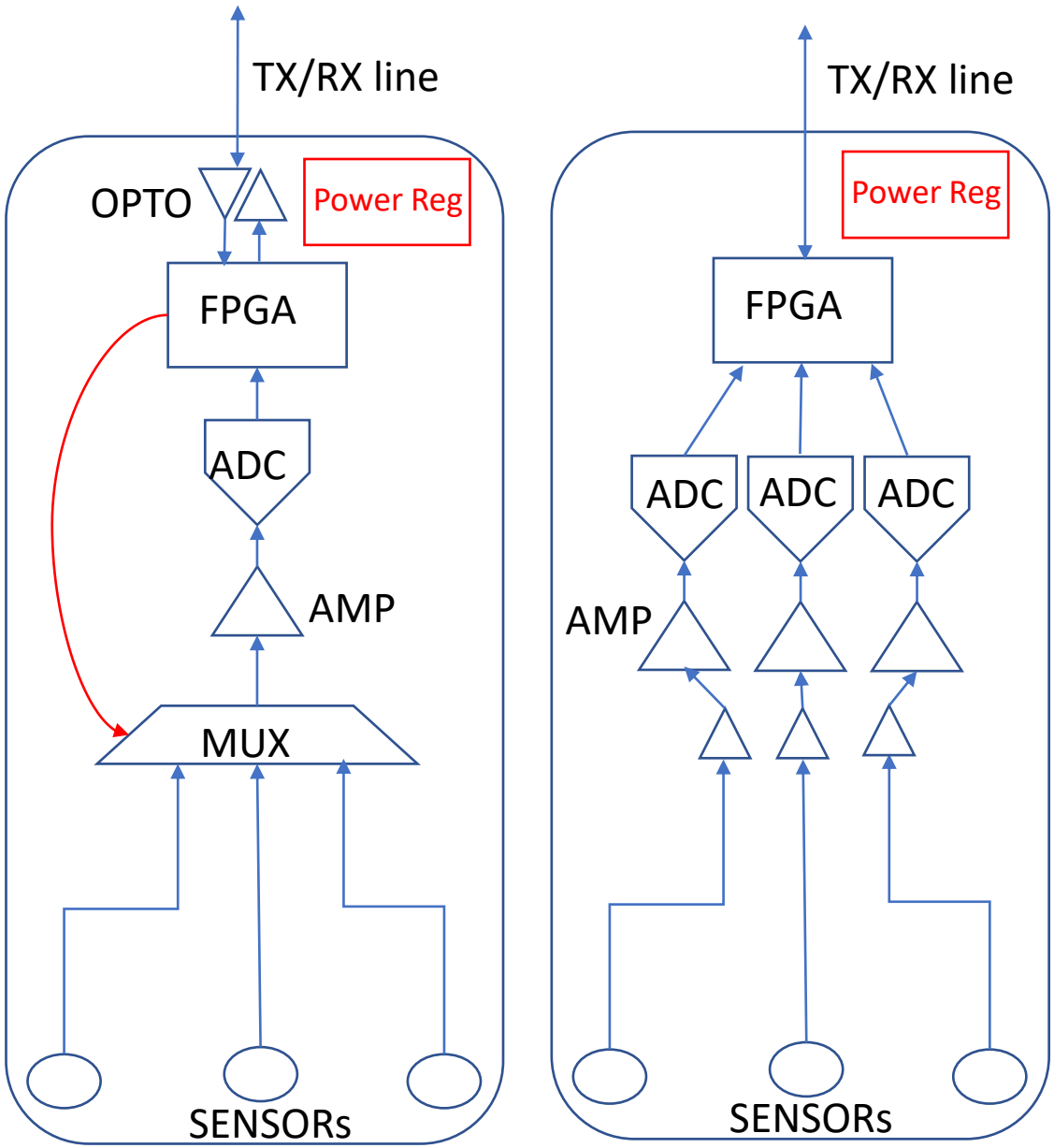
Architectures for cryogenic DAQ



Power:

- Switched Capacitor+LDO
- Power over Fiber
- LED supply

Communications:

- JESD
- LVDS
- CMOS
- Ethernet (PHY?)

Over copper or fiber
Single or multiple lanes.
Typically one lane provides 300Mbps

Isolation:

Opto or capacitive

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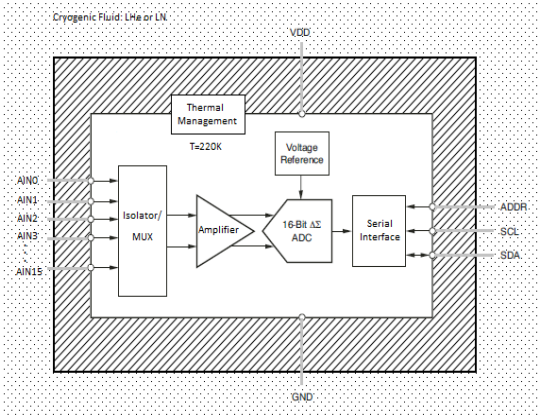
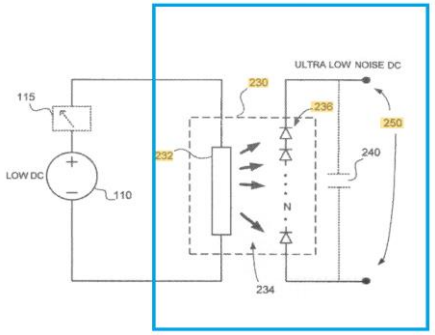
Bypassing the Problem

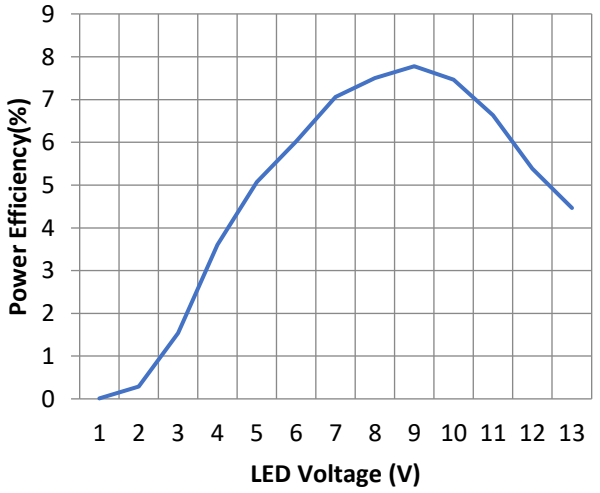
ACEe - Active Cryogenic Electronic Envelope (Gen 1)





Alternative: Power Over Fiber

- For LHe Operation
- Internal Temperature (70k to 100k)
- 16 analog channels
- 3000V input multiplexed isolation
- 16 bit ADC providing 1 MSPS per channel
- Low noise ADC, SFDR >100dB
- 3 wires digital interface
- Automatic temperature control
- Internal voltage reference
- 250mW maximum power dissipation
- Non-magnetic components



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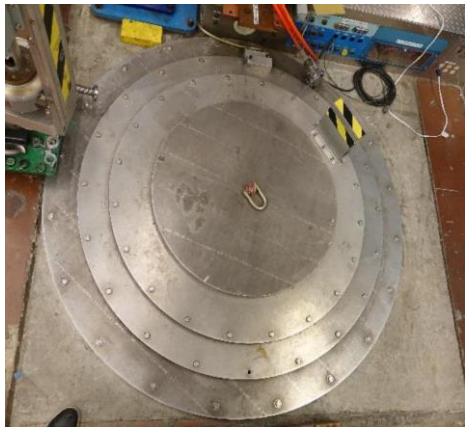
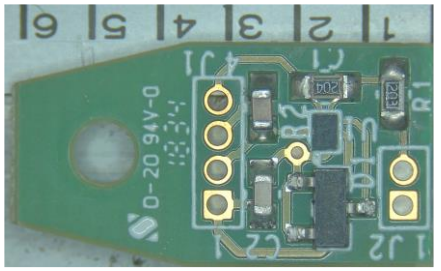
Systems with COTS cryogenic components

LN Test

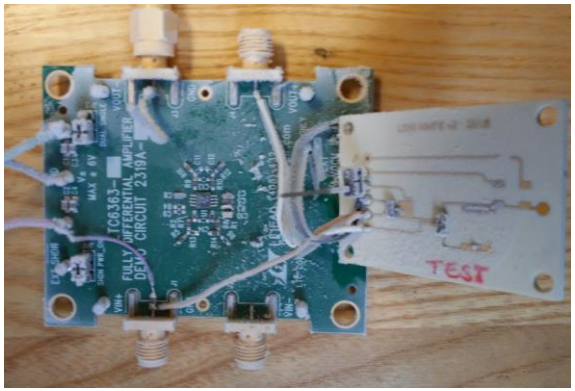
LHe Test



- **ADCs**
  - 24b / 20kSPS
  - 12b / 10MSPS
  - 4b / 500MSPS
- **Amplifiers** (up to 500MHz)
- **Diodes** (HV protection 1A)
- **FPGAs** (28nm- 45nm)
- **Laser Diodes Optical Isolators**
- **Voltage Regulators**
  - LDO and SW capacitor
- **Transistors**
  - JFET
  - HEMT
  - MOSFET
- **Passives**
  - Capacitors and resistors



Slow Amplifier
(Acoustic Instrumentation)



Fast Amplifier -500MHz

Basic COTS component

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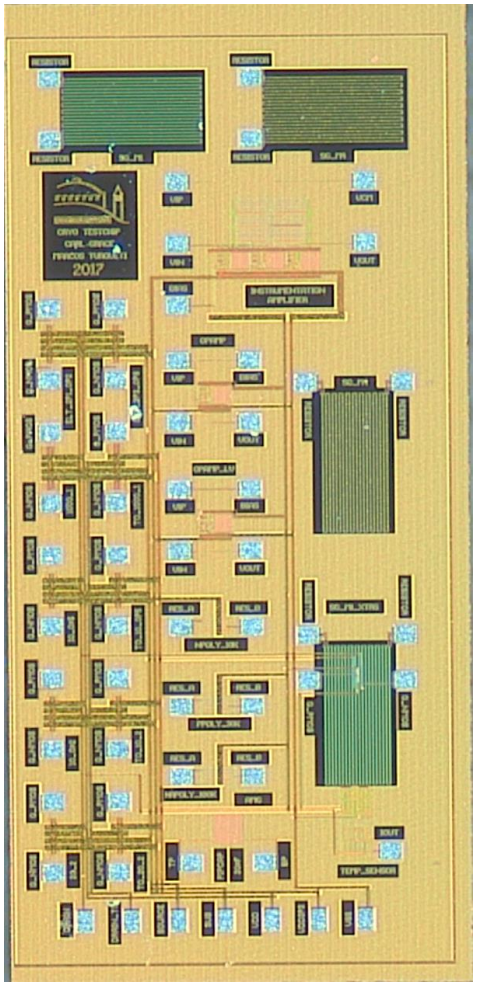
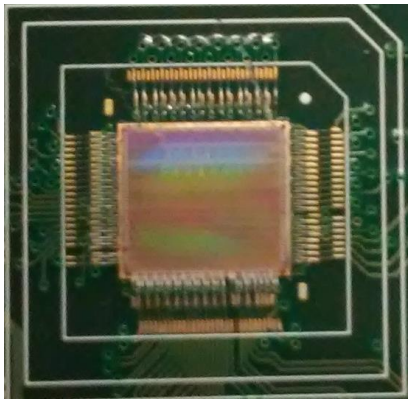
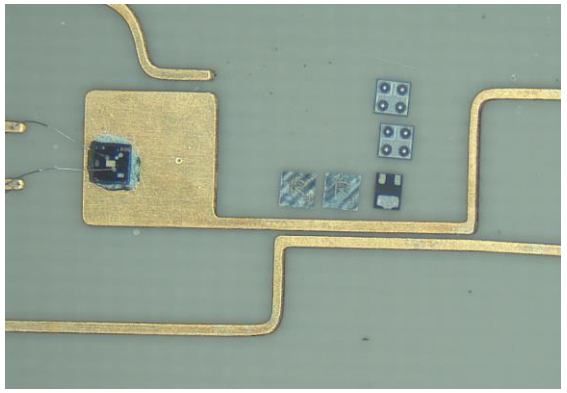
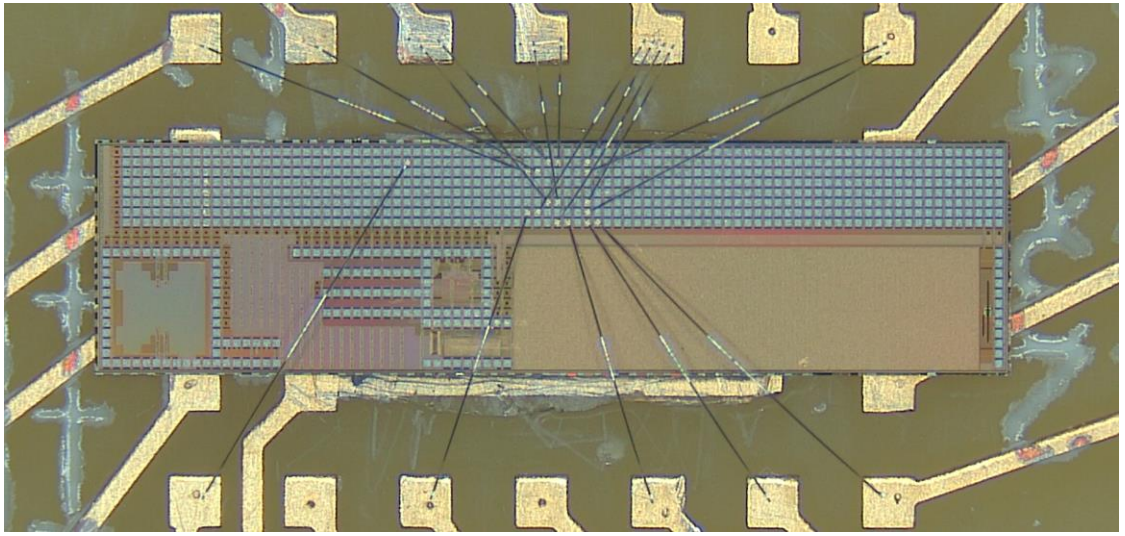
ASICs for Cryogenics









$$!,Development time, Not Flexible

Application Specific, Low Power

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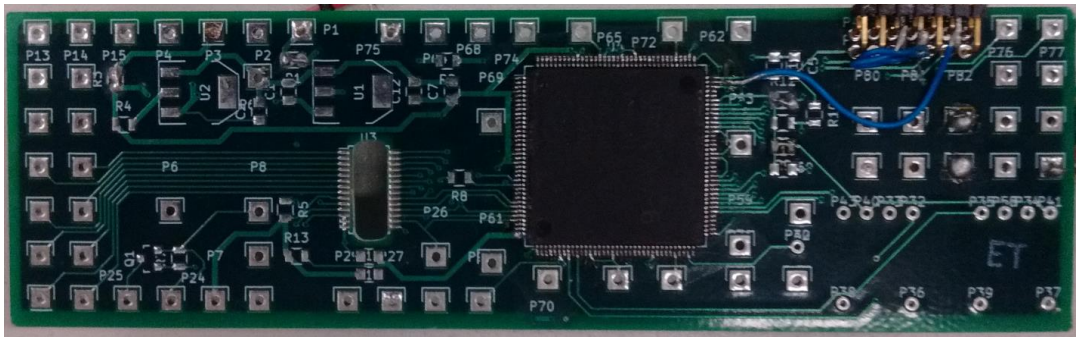
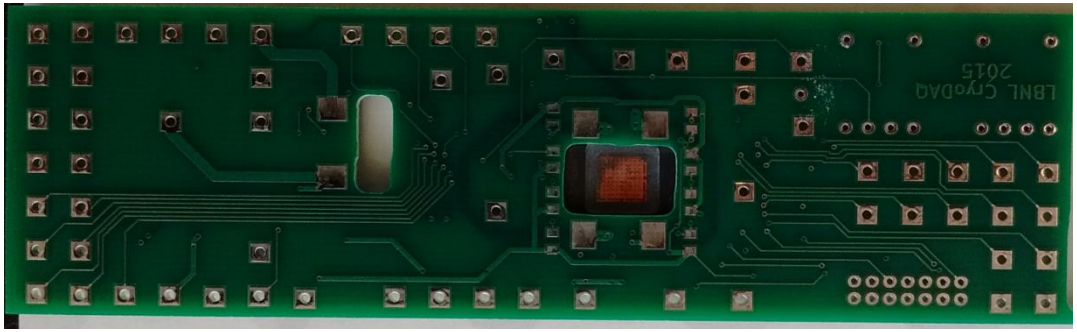
CryoDAQ

- Current versions are capable of dealing with 32 analog channels
- Data is transmitted fully digital
- System resides inside the cryostat and is capable of operating at 4.2k
- Tests were already performed with strain gauges
- Two existing versions:
  - Strain Gauge (SG) version: 20 SPS per channel
  - Voltage Taps (VT) version: 200kSPS per channel

Leaded Part



TOP



BOTTOM

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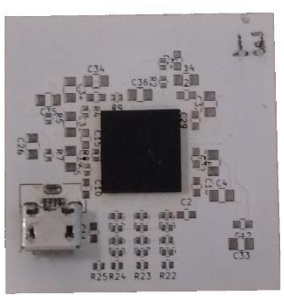
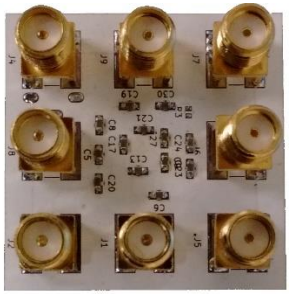
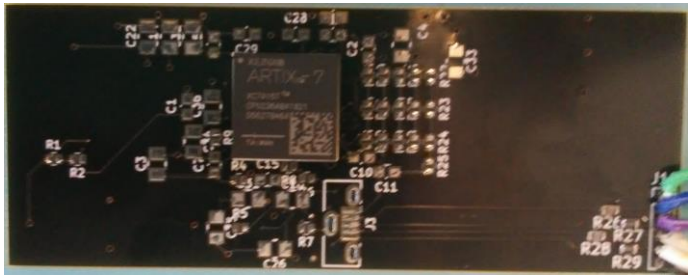
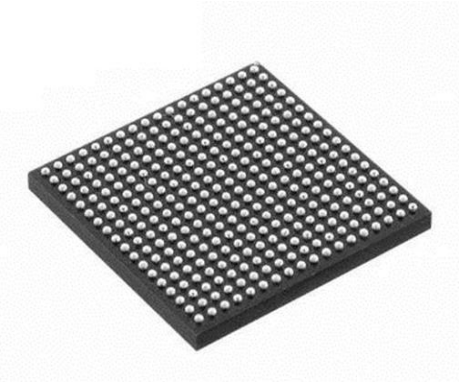
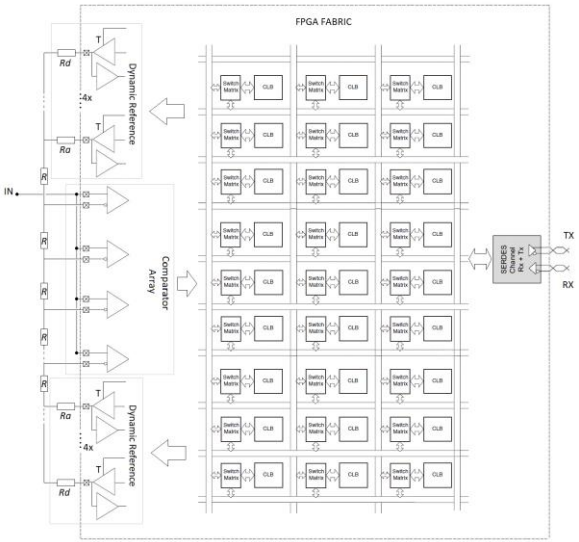
FPGA Based n-bit Analog to Digital Converter

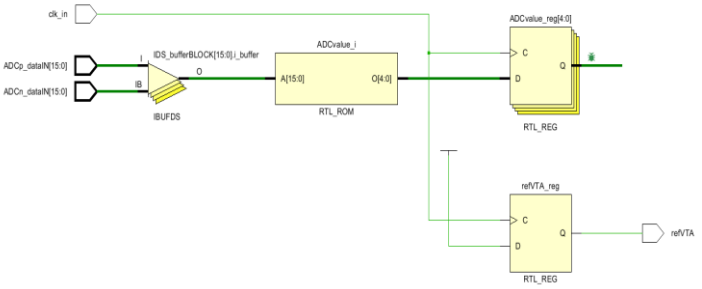


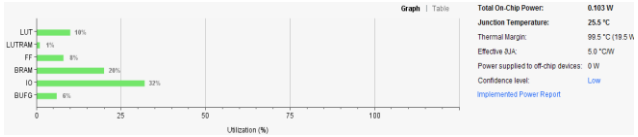












Reconfigurable Flash Folding Architecture. With this architecture it is possible to change the ADC resolution on the fly.

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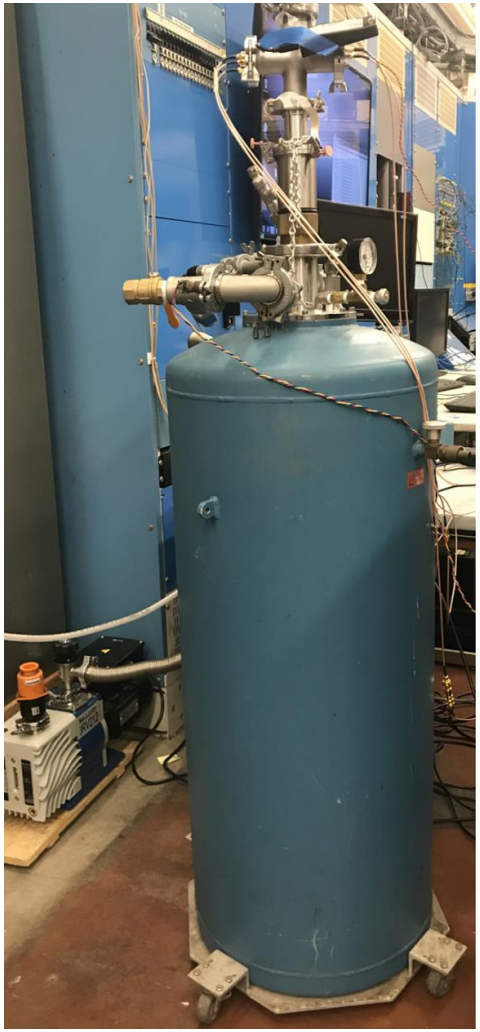
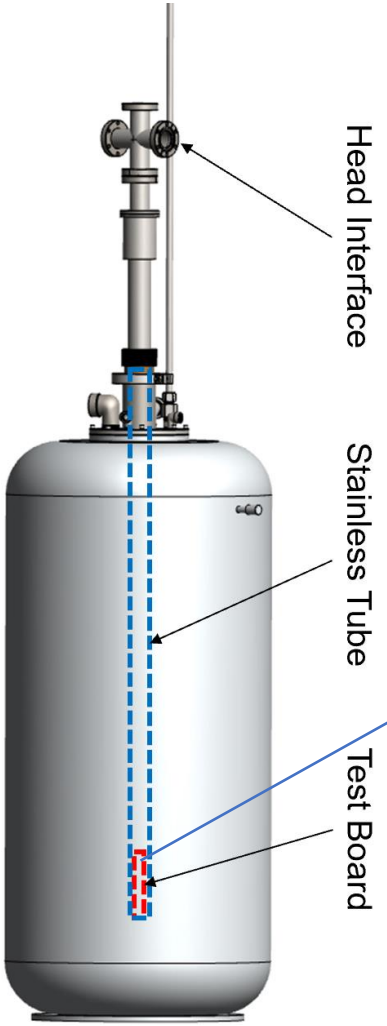
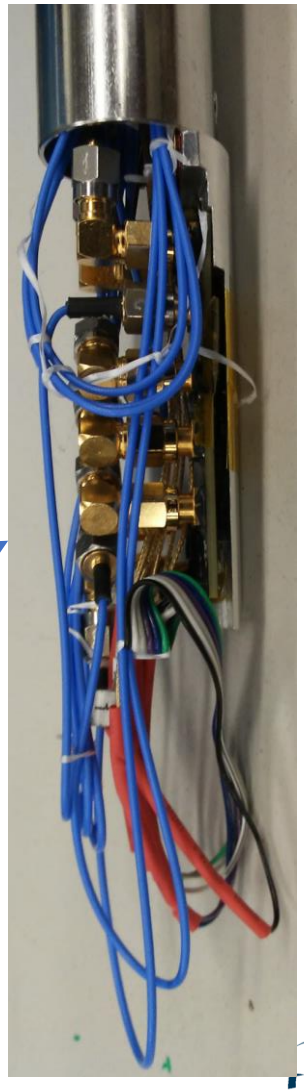
Test Setup at LBNL







*Maxim +Bleximo

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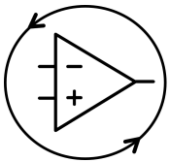

Threshold (Vth)

For an n-channel enhancement mode MOS transistor, the formula for threshold voltage is

$$V_{\mathrm{Th}} = V_{\mathrm{FB}} + 2\phi_{\mathrm{F}} + \frac{\sqrt{2\varepsilon_0\varepsilon_{\mathrm{s}} q N_{\mathrm{A}} (2\phi_{\mathrm{F}} + V_{\mathrm{SB}})}}{C_{\mathrm{ox}}},$$

where V_{FB} = flat-band voltage, ϕ_{F} = bulk potential, ε_0 = free-space permittivity, ε_{s} = dielectric constant of silicon, q = electronic charge, N_{A} = acceptor doping concentration, V_{SB} = substrate bias and C_{ox} = oxide capacitance per unit area. Also,

$$V_{\mathrm{FB}} = \phi_{\mathrm{ms}} - \frac{Q_{\mathrm{f}}}{C_{\mathrm{ox}}} - \frac{1}{\varepsilon_0\varepsilon_{\mathrm{ox}}} \int_0^{t_{\mathrm{ox}}} \rho_{\mathrm{ox}}(x) x \mathrm{d}x,$$

where ϕ_{ms} is the metal–semiconductor work function, Q_{f} is the fixed charge in the oxide, $\varepsilon_{\mathrm{ox}}$ is the relative permittivity of silicon dioxide, $\rho_{\mathrm{ox}}(x)$ is the charge density in an oxide of thickness t_{ox} varying with distance x in the oxide. For an n-type polysilicon gate (STMicroelectronics 2006)

$$\phi_{\mathrm{ms}} = -\left(\frac{k_{\mathrm{B}}T}{q}\right) \ln\left(\frac{N_{\mathrm{D(g)}} N_{\mathrm{A}}}{n_{\mathrm{i}}^2}\right),$$

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Threshold Voltage

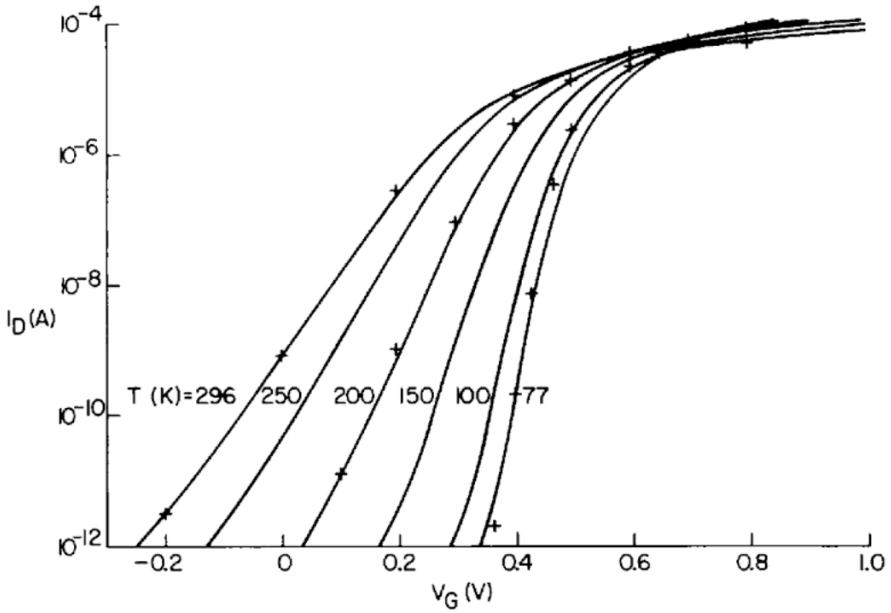

Fig. 16. Subthreshold current of MOSFET as a function of temperature from 77 to 296 K. (After Gaensslen *et al.* [43].) (Parameters: $L = 9\ \mu$m; $W = 87\ \mu$m; $V_d = 0.1$ V; $V_{s-sub} = 0$ V. Values, calculated by using two-dimensional model: +. Slope $= (q/2.3\ kT)[C_{ox}/(C_{ox} + C_{Si} + C_{FS})]$.)

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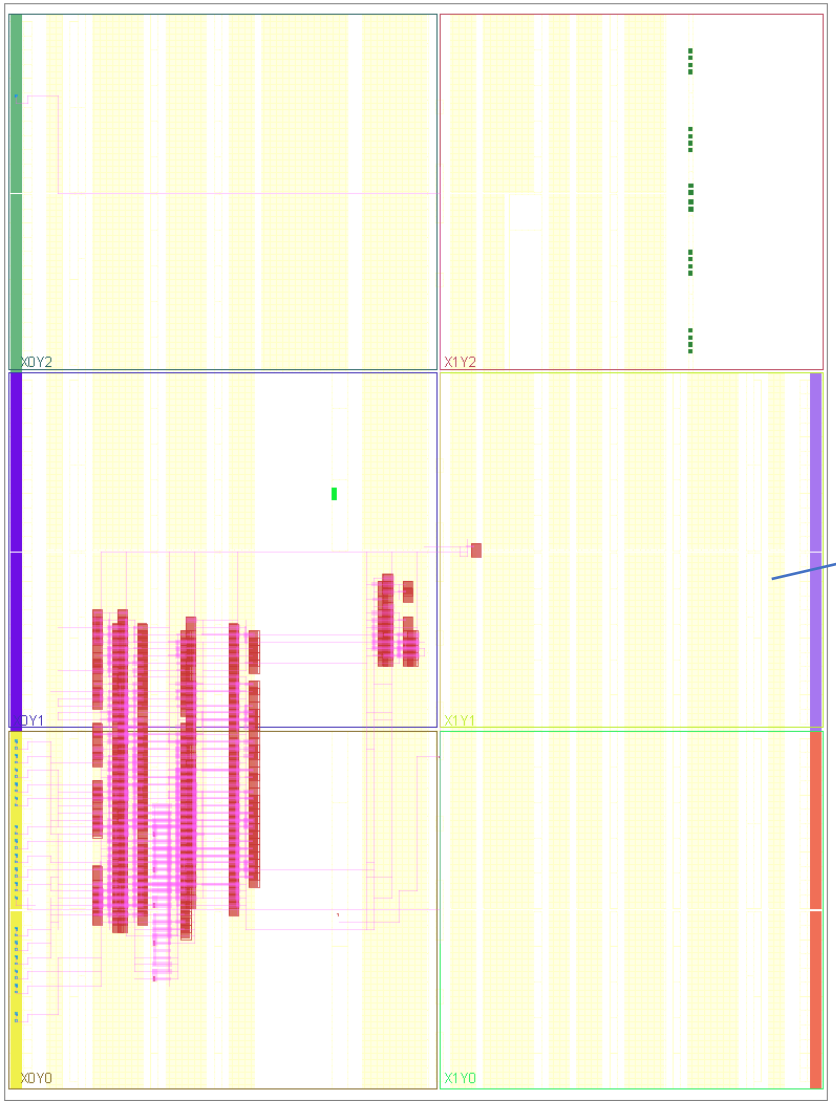
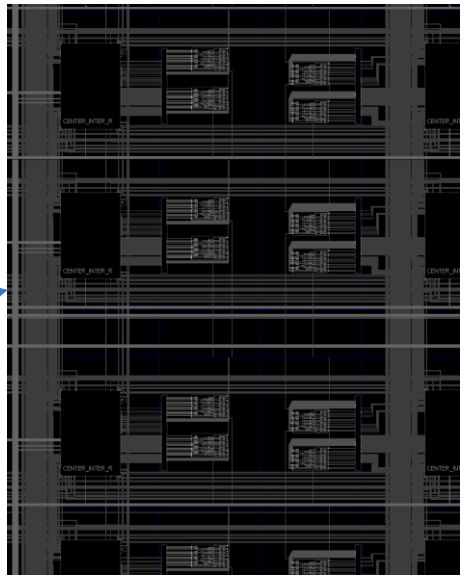
Artix 7 – FPGA (~1x1 cm)

XC7A15T





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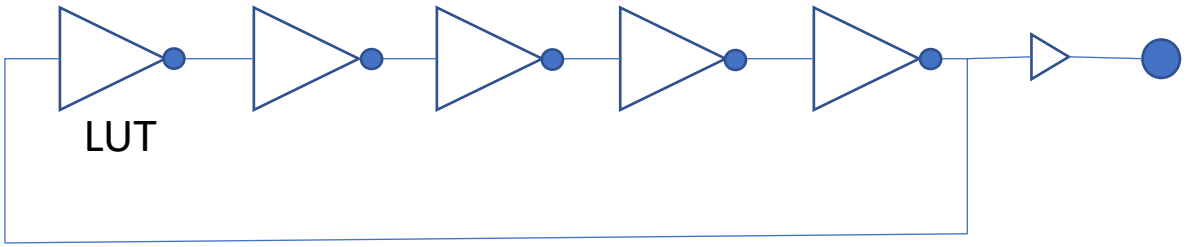
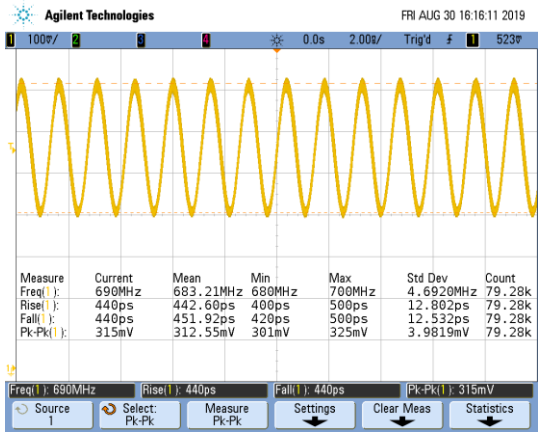
Test Circuits

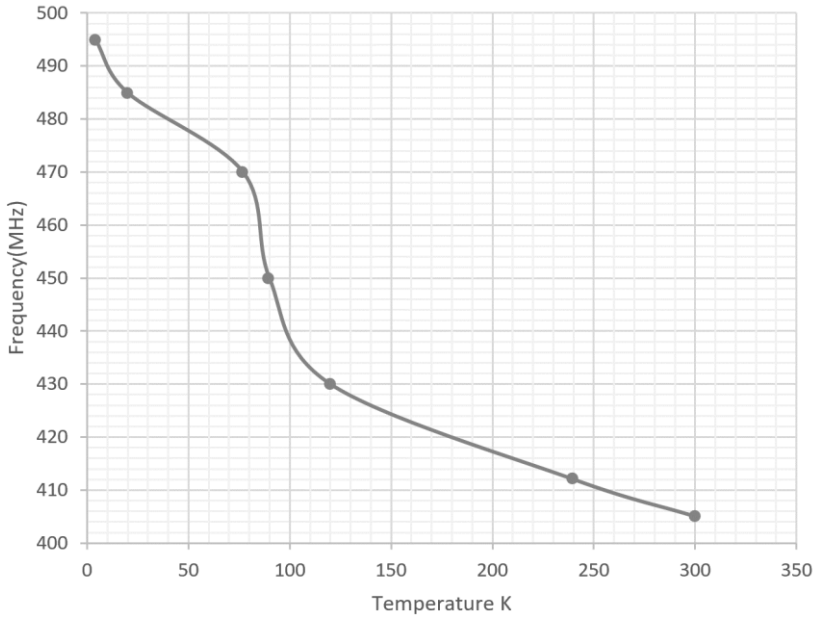
Five stage ring oscillator





VCCint = 2.1V
VCCO = 2.8V
VCCAUX = 2.8V

Frequency increase with temperature. Parasitic capacitance decreases



Frequency of the ring oscillator with five stages at different temperatures.

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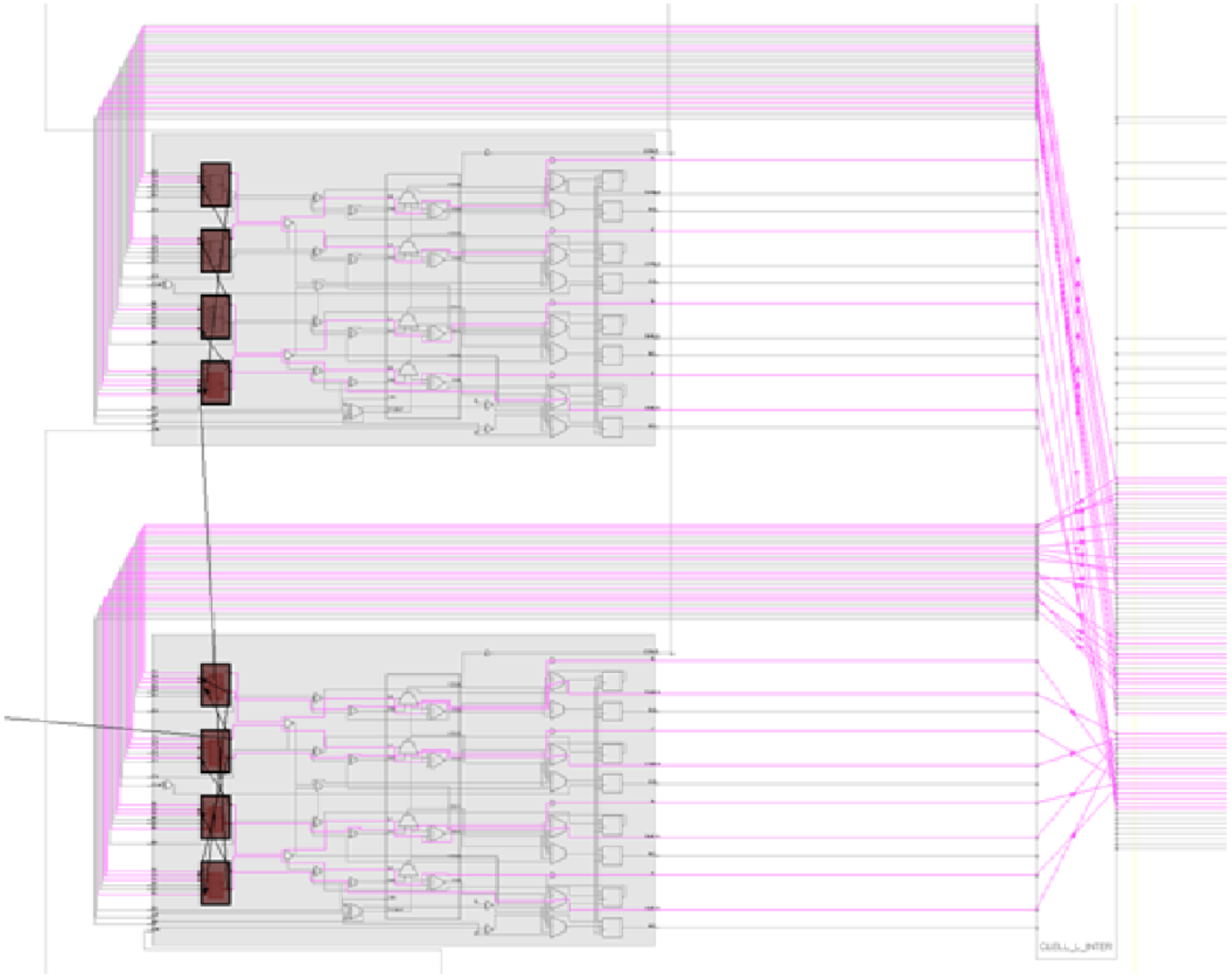
Artix 7 – Seven stages ring oscillator



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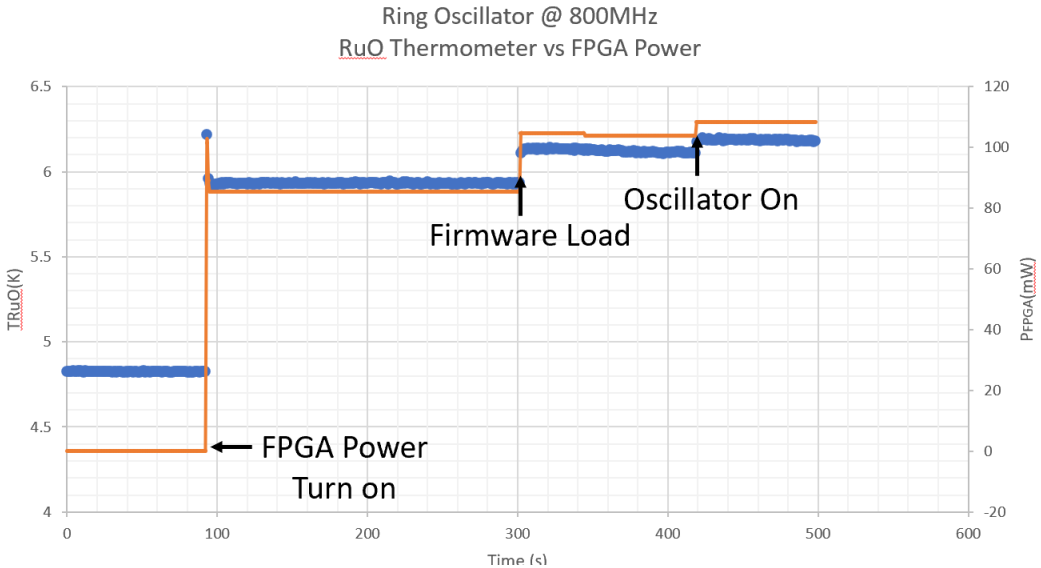
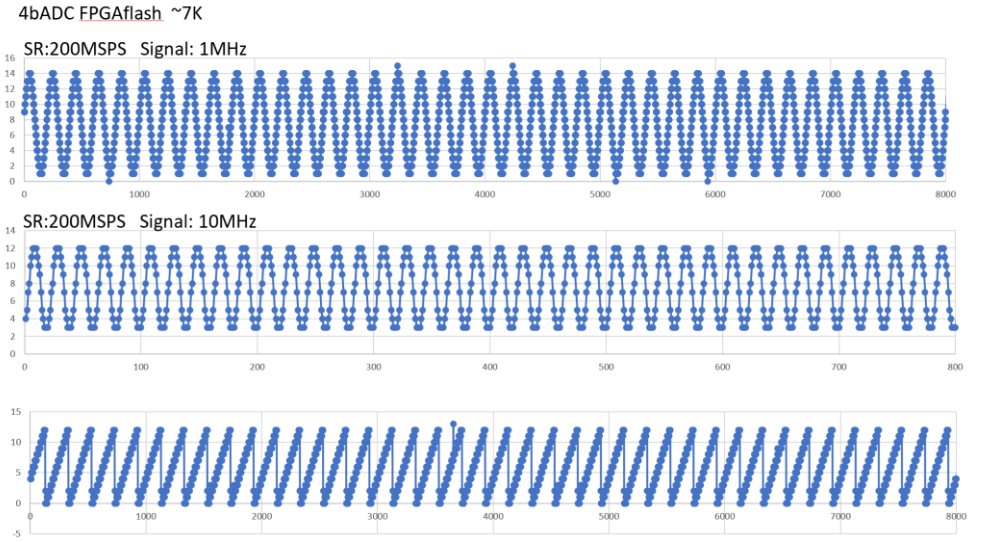
FPGA Performance Highlights





SR:20MSPS Signal: 500kHzCode error here. Still calculating code error rate. Design not optimize to minimize code error.

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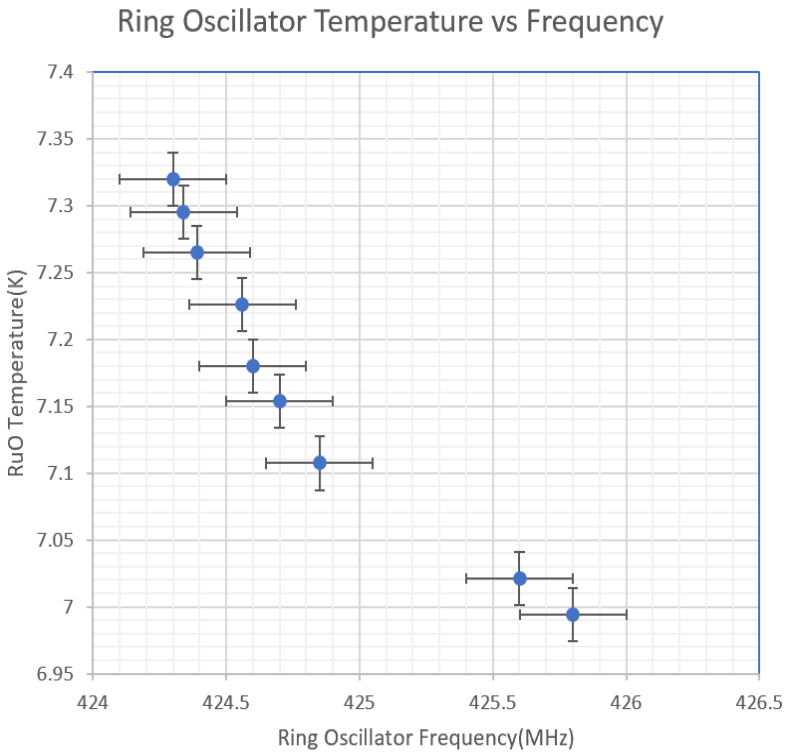
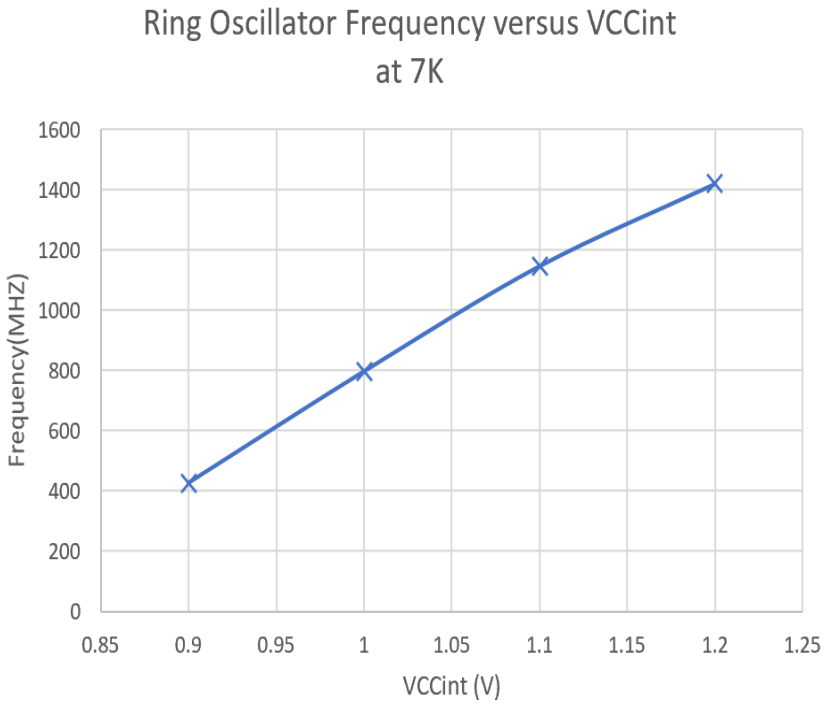
FPGA Performance Highlights





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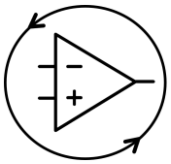

FPGA Performance Highlights

- Operates at 4.2K reliably both in Liquid Helium and on cold finger (at ~4.2K). Over 28 thermal cycles and 700 hours cold (~4K). No degradation detected. Even when submitted to thermal shock (dipping in LN);

- 60 mW power consumption with 3 stage ring oscillator +XADC running at 400MHz;

- 150 mW power consumption with 3 stage ring oscillator +XADC running at 1000MHz;

- 550 mW power consumption with 3 stage ring oscillator +XADC running at 1400MHz (max achieved clock) LVCMOS 1.8;
- Most of the power (80% for the 1.4GHz) is dissipated at the IO driver with 50 Ohms termination, temperature at the FPGA went up to 10K;

- For the 4bit ADC at 200MSPS power consumption was 300mW with Chipscope in. Estimated to be around 140 mW without Chipscope;

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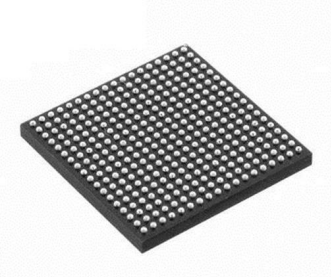
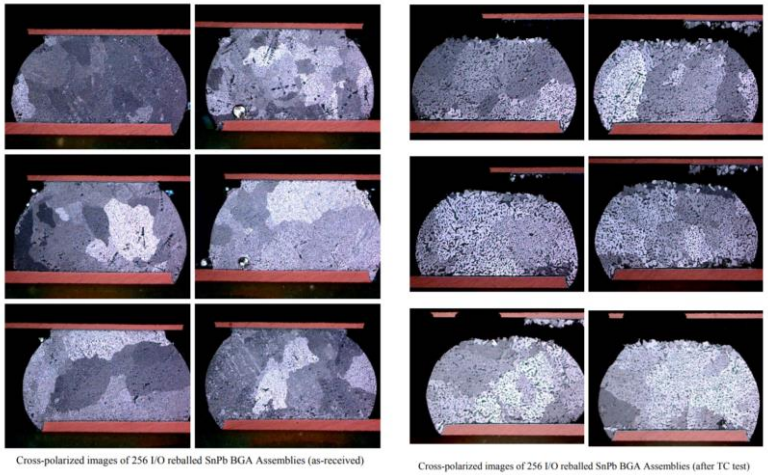
BGA Reliability

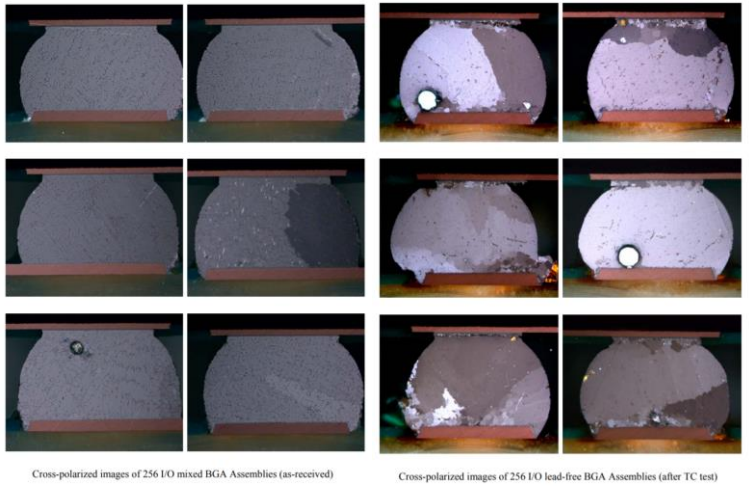




Cross-polarized images of 256 I/O reballed SnPb BGA Assemblies (as-received)

Cross-polarized images of 256 I/O reballed SnPb BGA Assemblies (after TC test)

Sn/Pb



Cross-polarized images of 256 I/O mixed BGA Assemblies (as-received)

Cross-polarized images of 256 I/O lead-free BGA Assemblies (after TC test)

Lead Free

*TEMPERATURE CYCLING RELIABILITY OF REBALLED AND REWORKED BALL GRID ARRAY PACKAGES IN SNPB AND SAC ASSEMBLY Lei Nie, Doctor of Philosophy (Ph.D.), 2010

*Indium balls are even better

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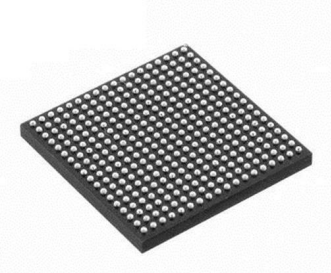
BGA Reliability



Cycle Type	Number of Cycles	Typical Cooldown Time(s)	Typical Warmup Time(s)	Total Number of Hours Cold(Hs)
LN Submersion	14	5	300	~5
LHe Submersion	6	7000	200000	~360
LHe Cold Finger (290K to 4.2K)	8	3000	170000	~400

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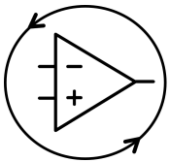

Artix 7 Series

Artix-7 FPGA Product Table

XC7A12T | XC7A15T | XC7A25T | XC7A35T | XC7A50T | XC7A75T | XC7A100T | XC7A200T

COMPARE | Reset

	XC7A12T	XC7A15T	XC7A25T	XC7A35T	XC7A50T
Logic Cells	12,800	16,640	23,360	33,280	52,160
DSP Slices	40	45	80	90	120
Memory (kb)	720	900	1,620	1,800	2,700
GTP 6.6Gb/s Transceivers	2	4	4	4	4
I/O Pins	150	250	150	250	250

Artix-7 FPGA Product Table

XC7A12T | XC7A15T | XC7A25T | XC7A35T | XC7A50T | XC7A75T | XC7A100T | XC7A200T

COMPARE | Reset

	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Cells	33,280	52,160	75,520	101,440	215,360
DSP Slices	90	120	180	240	740
Memory (kb)	1,800	2,700	3,780	4,860	13,140
GTP 6.6Gb/s Transceivers	4	4	8	8	16
I/O Pins	250	250	300	300	500

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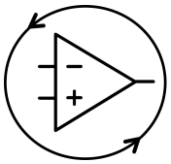

Implemented test structures

- LUT
- I/O (LVCMOS25 operating at 2.8V, 4mA)
- Ring Oscillator
- Counters (8/16 bits)
- Shift register (16 bits)
- LVDS tx/rx communications
- ADC

Evaluated at 290K,77K*,4.2K*
*immersed

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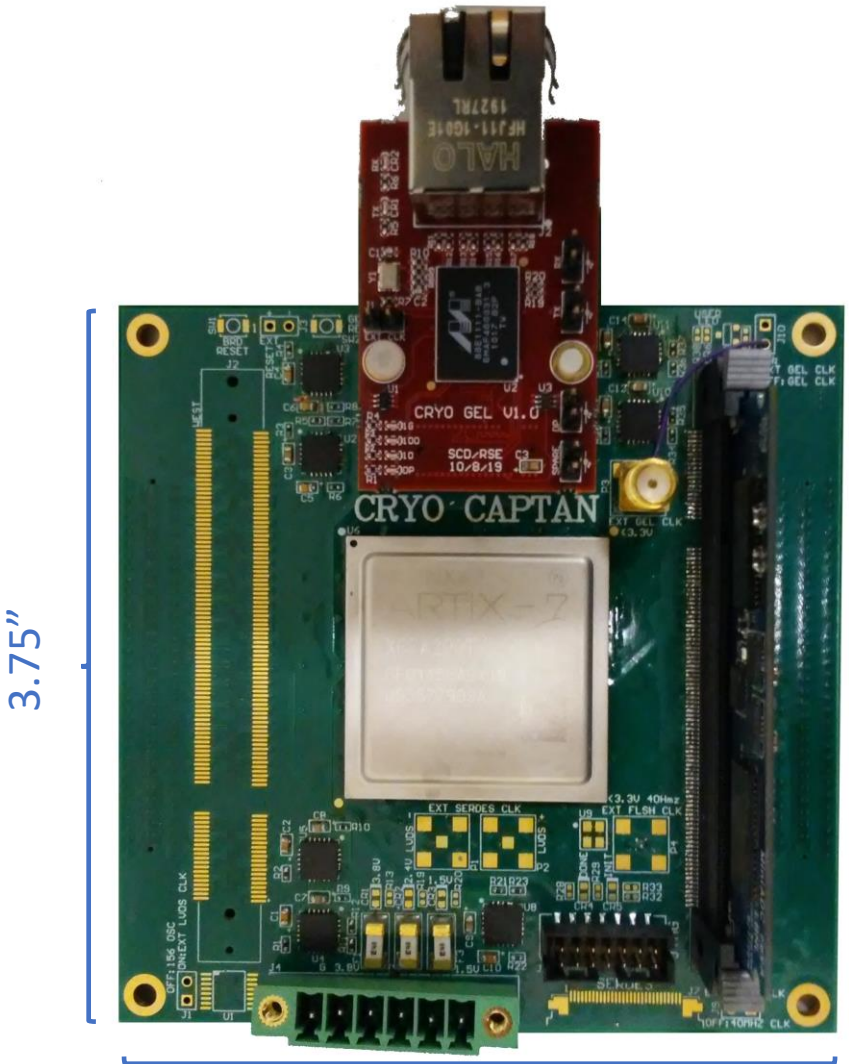
Gen4 CryoDAQ – LBNL-Fermilab

- Large Artix FPGA (28nm)
- 64 Analog channels
- External Clock
- Laser Driver for communications
- LDO’s
- External Clock
- Max operational clock 1GHz
- Expected around 1 W of power dissipation



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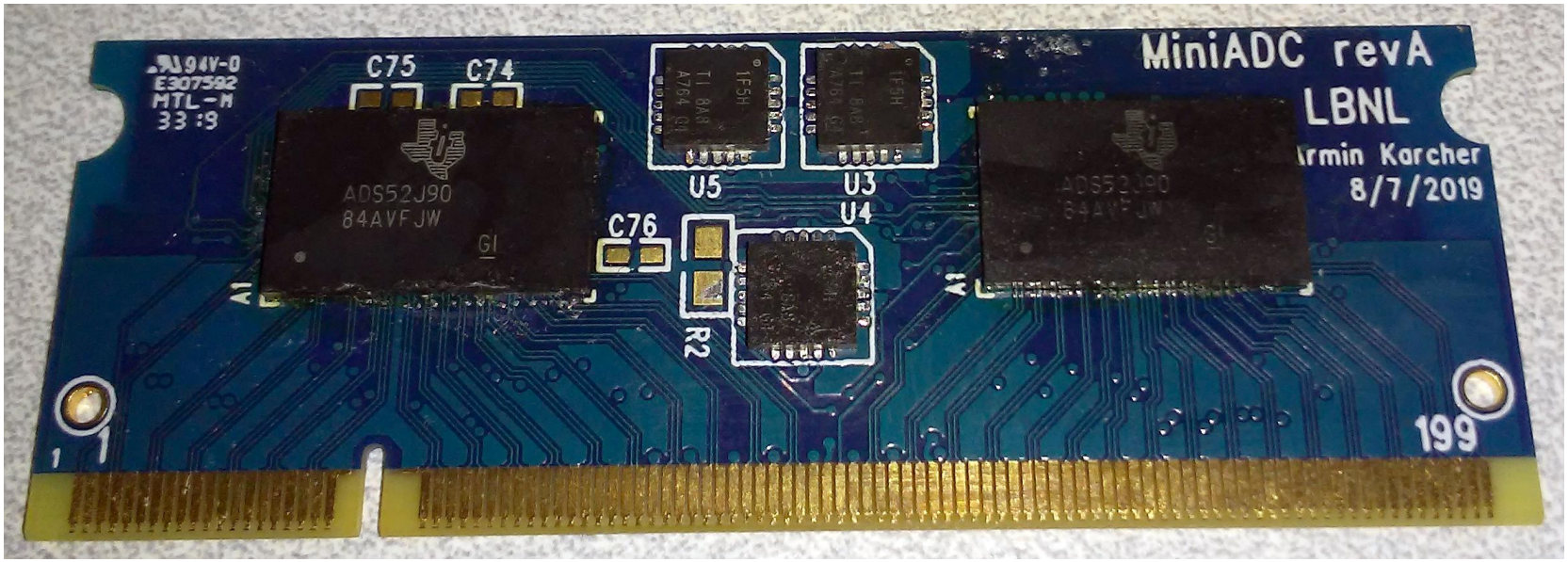
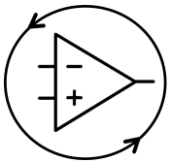
ADC board

- 32 ADCs
- Sampling rate up to 100MSPS (50MHz signals)
- 14bits
- Not tested cold yet





Possible Issues

- PLL, SERDES,iDelay, XADC (dedicated hardware)
- Asynchronous circuits timing uncertainty
- I/O threshold fluctuation
- Increased power consumption (+40% from room temp at 4.2K)
- Bump bond detachment with thermal cycles
- Difficult access (inside the cryostat)
- Power consumption

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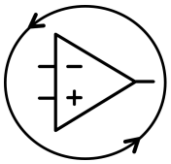

Conclusions

- Many options available for cryogenic data acquisition
- COTS components can be used
- Growing number of Applications Specific Integrated Circuits (ASICs) available
- Software developed needed
- More collaboration needed between potential users

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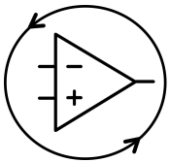

To ADD

- Digital Magnet
- Ethernet PHY
- Materials SiGe, GaN …
- Bump bond (Indium)
- Simulations/Characterization

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