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Revision History

Revision	Date Released	Description of Change
R0	6/23/2014	Original Release.

1 Purpose

This document describes the physics requirements for the LCLS-II master oscillator and phase reference system. This system will also serve as the master source for LCLS-I as operation of the two accelerators needs to be synchronized.

2 Definitions

Allan Variance	A measure of the RMS frequency error of a source measured over the specified time interval
Fiducial	A marker on the RF signals which allows receiving devices to be synchronized to within one RF cycle.
Pattern	A bit pattern sent on the timing system that describes the state of the accelerator for each beam pulse (see timing PRD)
1300MHz	The RF frequency of the cavities, 1300MHz +/- 1ppb
325MHz	The reference 1300MHz / 4
71KHz	71.42857… KHz = reference 1300MHz / 18200
476MHz	476.0 MHz +/- 1ppb = reference 1300MHz * (6664 / 18200)

3 References

LCLSII-2.7-PR-0066	Controls System Requirements PRD
LCLSII-2.7-PR-0067	Timing System PRD
TBD	Bunch Arrival Time Monitor PRD

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4 Responsibilities

Jose Chan	Accelerator System Manager
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5 System Configuration

The phase reference system contains several subsystems, each described in more detail later in this document or in other PRDs:

5.1 Master Source

The master source contains a high stability frequency reference and provides the timing reference for LCLS-II and LCLS-I.

5.2 Timing Transmitter

The timing transmitter for LCLS provides the pattern data and timing clock for subsystems. It is described in PRD (TBD).

5.3 Phase Reference Line / Phase Receiver

The phase reference line provides high stability, low noise RF to the LLRF stations over the 700M LINAC.

5.4 Long Haul Transmitter / Receiver

This system transmits the RF phase and fiducial from the end of the LINAC to the undulator hall approximately 4 kilometers away.

6 Frequencies

Certain frequencies are set by the design of the accelerator. Note that in this document, the display of these frequencies is truncated to a few digits for clarity, but they are required to be the exact values shown here.

LCLS-II SCRF frequency	1300 MHz
LCLS-I Main Drive Line	476 MHz
LCLS-I Damping Ring Frequency	8.5MHz
LCLS-II Gun frequency	=185.7142857 MHz (1300/7)
Highest common LCLS-I / LCLS-II frequency	71.428571428KHz = 1300MHz/18200

The frequency used for RF phase transmission is not a physics requirement.

7 Design Assumptions

The following are not requirements, but are assumed in the discussion for clarity, and to provide a context for the specifications. If these assumptions are changed, the impact on the performance of all the associated sub-systems needs to addressed.

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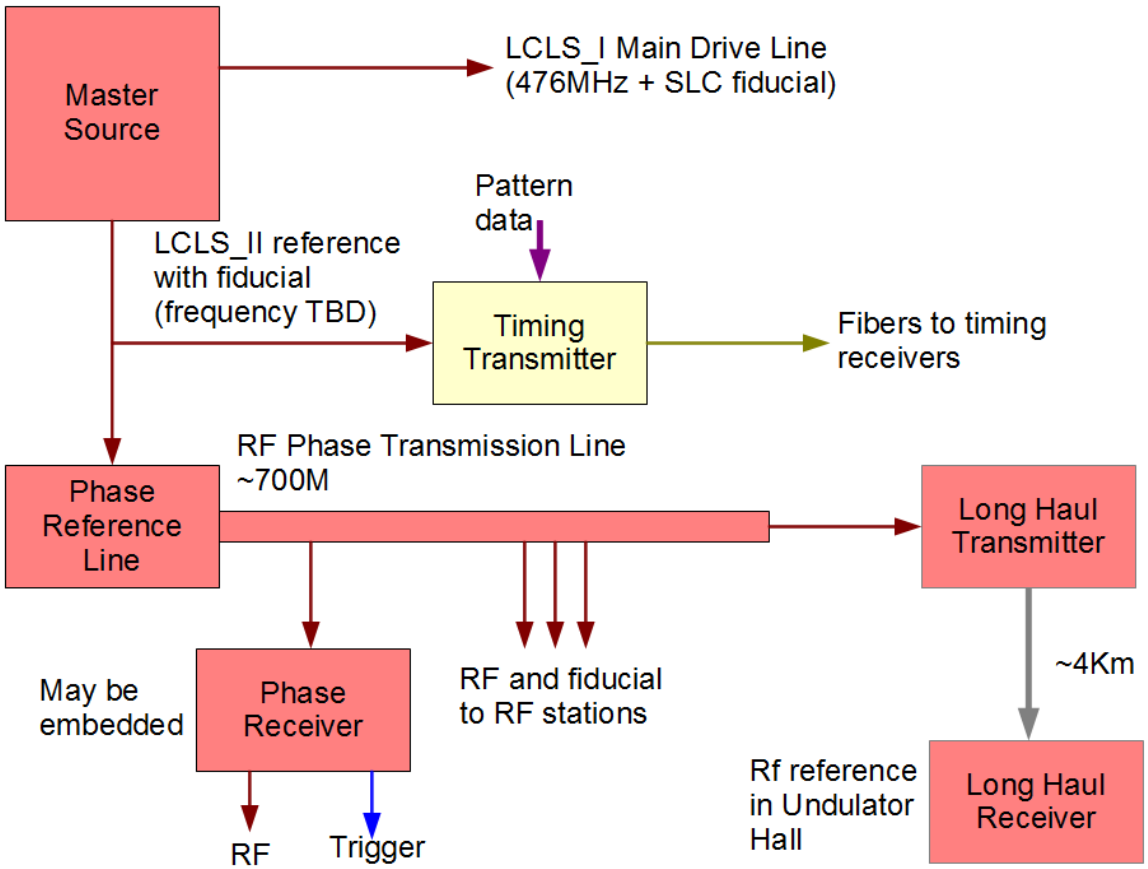
- Location of specifications: All phase specifications are measured at the end of a cable in the accelerator housing.
- Reference system hardware: All phase transmission is assumed to be done by a cable or waveguide located in the accelerator housing.
- Frequencies: The phase transmission is assumed to be performed at 325MHz. This is not a requirement and other frequencies could be used.
- Fiducials: Fiducials are assumed to be 60Hz line locked and transmitted at 360Hz. The same fiducials are assumed to be used for LCLS-I and LCLS-II. Line locked fiducials are not a requirement; however, the capability for 60Hz line locked operation of the accelerator is a requirement.
- Fiducial type: The fiducial is assumed to be a phase modulation designed to have nominally zero signal at the RF carrier, and zero time integrated phase shift.

Note that some system descriptions indicate that significant engineering or R&D is required to meet the specifications.



Phase reference system block diagram

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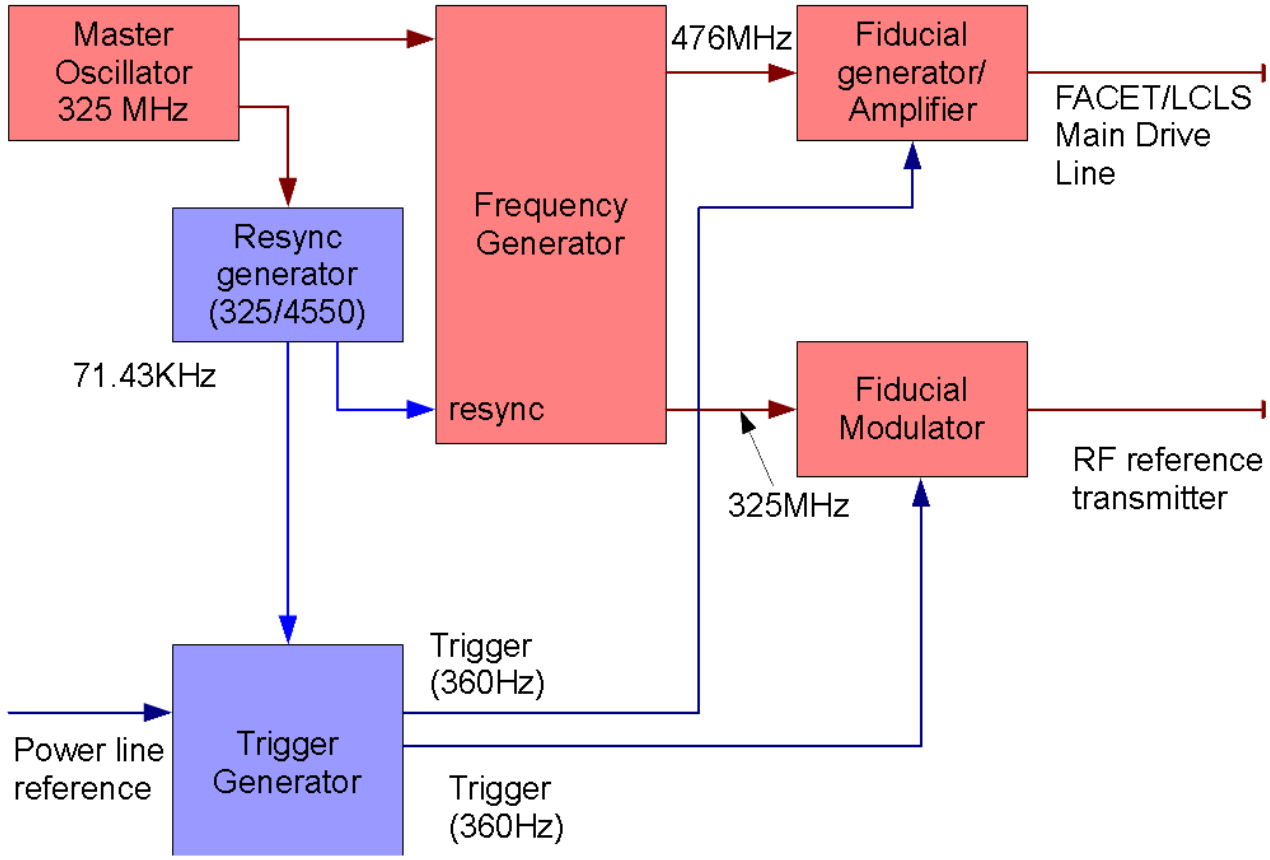
8 Master Source System

The LCLS-II accelerator operates at a frequency of 1300MHz. The master source system generates the following signals:

- An accelerator phase reference signal for LCLS-II at an integer sub-harmonic of 1300MHz with a “fiducial” modulation that allows downstream devices to identify a single cycle of RF.
- The LCLS-I / FACET Main Drive Line signal comprising a 476MHz reference signal with a “SLC style” fiducial at 360Hz.

The master source contains subsystems described below. This is a functional description, not a hardware description. The physical modules may consist of different combinations of functions than shown in the block diagram below.



Master Source System

8.1 Master Oscillator

The master source frequency needs to be an integer fraction of 1300MHz that is harmonic with a 18200 division ratio. The likely choices are 1300MHz, 650MHz, or 325MHz.

Parameter	Value	Comment
Frequency	325MHz	¼ Sub-harmonic of 1300MHz
Frequency accuracy	$<10^{-10}$ absolute accuracy	
Frequency drift	$<10^{-10}$ / month	Available with commercial Rb source
Allan Variance	$<10^{-10}$ (1 S to 1000 S)	Corresponds to 1fs at the end of the accelerator
Phase noise	<1 fs integrated 100Hz to 10KHz	See text
Output Power	>10dBm	
Output Power stability	<0.1dB	
Outputs	4, >80dB Isolation, Type N Connectors	

8.1.1 Frequency Reference

Changes in the master source frequency will cause phase changes between the electron beam and the RF phase distribution system. A 0.1 ppb stable reference will reduce this error to ~1 femtosecond. The same argument indicates a requirement for a source with an Allan Variance (frequency error over time) of 0.1ppb.

Note that Commercial GPS-locked sources with absolute stability and <1Hz Allan Variance of $< 3\times10^{-12}$ from *Quartzlock* and other vendors are well within the state of the art.

8.1.2 Phase Noise

In principal, low offset frequency phase noise will have minimal effect on the relative timing of the electron beam and the phase reference. In practice however, low bandwidth devices including mode-locked lasers and some RF systems will not follow the timing changes of an electron beam with large phase noise. Phase noise above approximately 10KHz is generally not a problem as it can be easily corrected with local phase locked loops.

At the time of this writing, the bandwidths of the experiment laser locking loops and other narrow band systems are not known. High performance quartz oscillator technology can provide approximately 1fs phase noise between 100Hz and 10 KHz and we take that as a specification.

Note that higher performance sapphire oscillators (from *Poseidon* / *Raytheon*) are available with 1fs noise integrated above 10Hz; however, they are quite expensive and should be viewed as a possible upgrade path.

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The phase noise is a technically challenging specification. There has been considerable development of low phase noise commercial oscillators, and the best approach is to use a state of the art commercial source rather than develop new technology in-house.

8.1.3 Outputs

Multiple isolated outputs are specified to allow the addition of monitoring equipment and sources for other accelerator systems.

8.2 Resync Generator

The resync generator provides a 71KHz clock where 71KHz = 1300MHz / 18,200 = 476MHz / 6664. The 476MHz reference is used for the LCLS-I and FACET systems. This 71KHz is the highest frequency that is an integer sub-harmonic of all LCLS-I and LCLS-II system frequencies.

Note that the resync pulse is available to reset all dividers in the LCLS-II and LCLS-I systems to eliminate the hidden internal state of counters. The resync generator dividers do not themselves need to be reset.

8.3 Frequency Generator

The frequency generator must generate a 476MHz reference for the LCLS-I systems with low phase drift and noise relative to the LCLS-II reference. The noise and drift specifications are the same as for the master oscillator 8.1. This noise from the frequency generator is assumed to add in quadrature with the master oscillator noise.

Note that due to the tight noise / drift specifications, this subsystem requires considerable engineering, a simple FPGA based PLL is unlikely to meet the requirements.

8.4 Trigger Generator

The Trigger Generator creates a 360Hz trigger locked to the power line frequency; then it issues an output trigger on the next cycle of the 71KHz resync clock from the resync generator. Since the power line frequency varies, the time between triggers will not be fixed, but will vary by integer numbers of cycles of 71KHz. The information on the number of 71KHz clocks before the next trigger needs to be transmitted to the timing system.

Since the timing system needs the trigger timing information at least one 360Hz cycle in advance, the trigger generator will need to predict the next resynchronized power line crossing. This can be done by assuming that the power line frequency is slowly varying. The 71KHz is low enough in frequency to allow this calculation to be done in programmable logic.

8.5 Fiducial Modulator

This provides the required time dependent phase shift on the 325MHz reference tone. A variety of types of modulation are possible. An example phase modulation scheme proposed by Larry Doolittle is shown below. Note that use of this specific shape is not a requirement.

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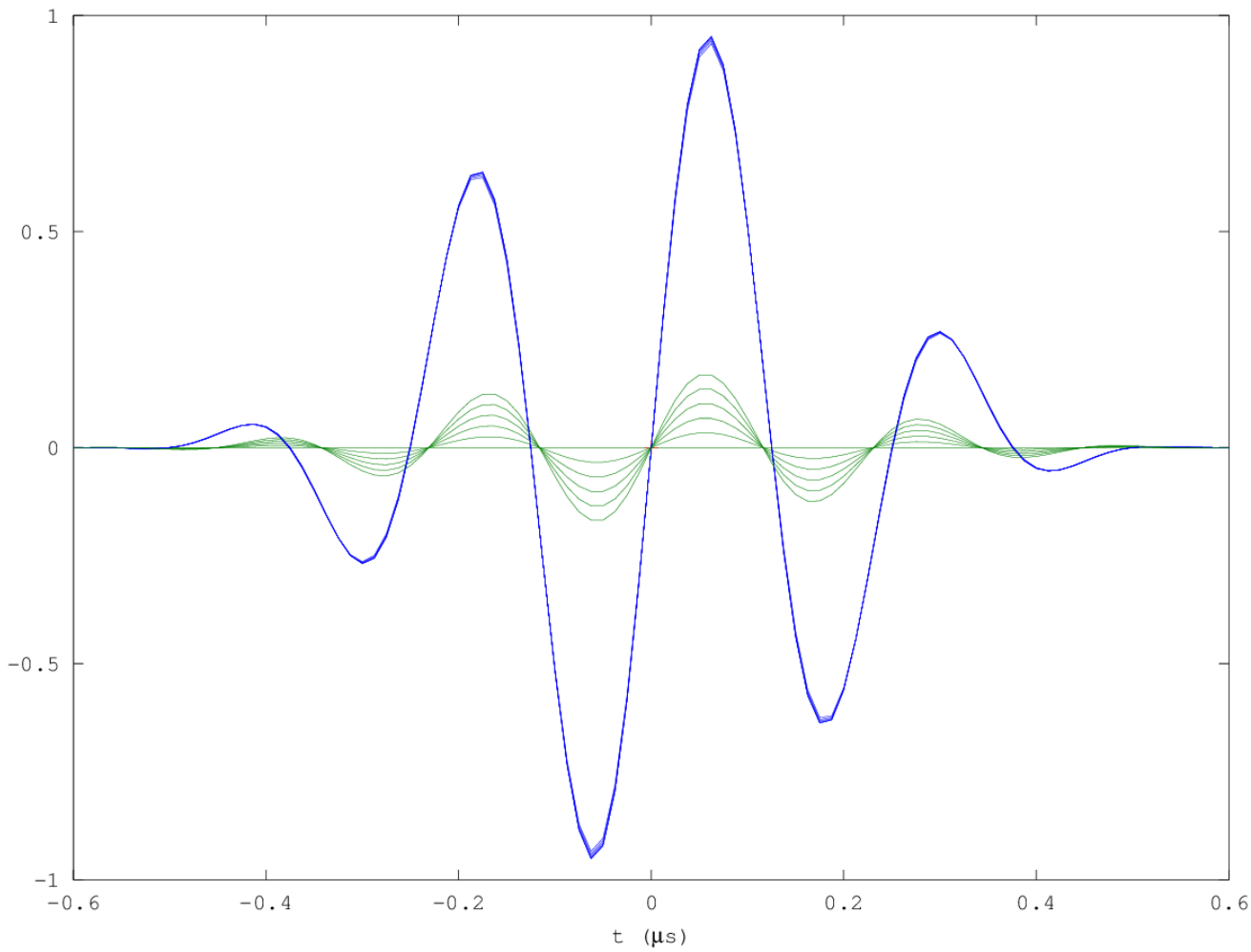

Example phase modulation scheme (vertical axis is phase in radians)

- Limited bandwidth: The maximum bandwidth allowed depends on the engineering details of the phase transmission system, <10% bandwidth is probably a reasonable guide.
- Limited power modulation: The fiducial must not require large excursions in the RF phase reference system power. Again, the limits will depend on the engineering details of the system. <0.5dB is probably a reasonable guide.
- Accuracy: The fiducial must allow an unambiguous identification of an individual 325MHz cycle in the reference system, even after any dispersion in the phase system has distorted the modulation.

8.6 Fiducial Generator / Amplifier

This provides the main driveline signal for LCLS-I and FACET. The power level and fiducial requirements need to match the existing LCLS master source and fiducial generator. The existing fiducial generator / amplifier hardware can be used, or a new amplifier / fiducial generator can be developed.

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9 Timing Transmitter

The timing transmitter takes the 325MHz reference with fiducial and fiducial timing data (section 8.4), using them as a reference for the timing system. The timing system is described in the Timing System PRD.

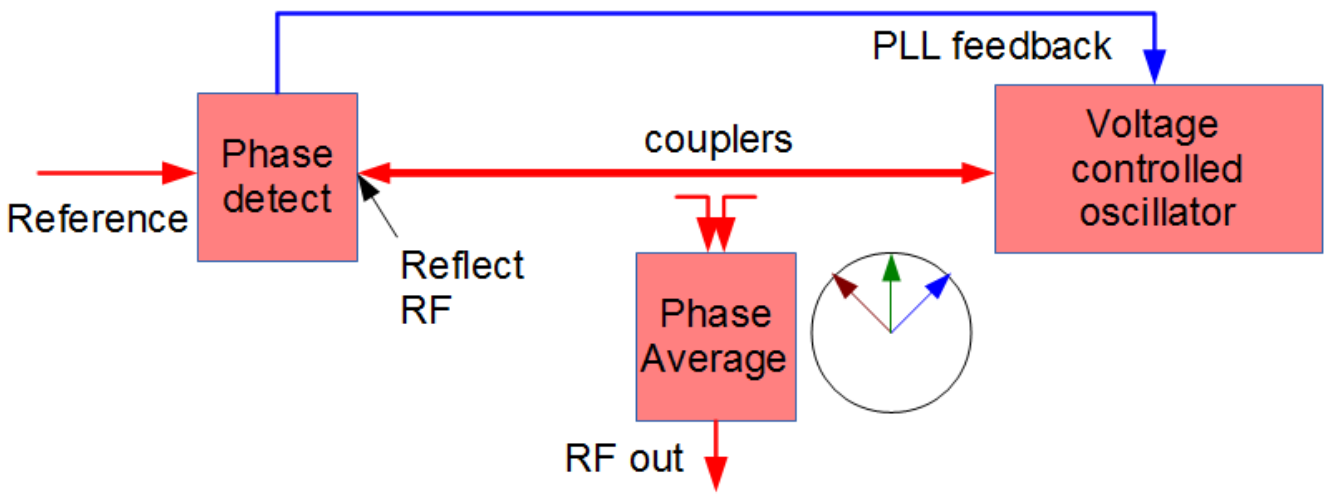
10 Phase Reference Line

The phase reference line extends for the 700M length of the superconducting accelerator. Outputs with a RF phase reference and fiducial are provided for every cryomodule.

10.1 Implementation

While not a requirement, a specific implementation is described to provide a context definition of requirements.

The phase reference line uses a RF reflectometer system similar to that described in the LCLS-II CDR chapter 13, section 2, and used for the LCLS-I experiment phase transmission.



The actual implementation may vary from this description in a number of ways:

- Use of phase shifters from a reference rather than a phase detector / VCO PLL
- Use of pulse or otherwise modulated signals to reduce the effects of interference between forward and backward signals in the phase average
- Digital phase averaging will be used in the LLRF receivers. Note that the phase average may be incorporated in the firmware of the LLRF FPGA instead of being a separate piece of hardware.

10.2 Environment

The phase distribution will be located in the accelerator housing. The temperature stability of the accelerator housing for the LCLS-II SC accelerator is not yet known, but for the purposes of this design will be assumed to be +/- 1 degree C.

10.3 Required Performance

These outputs meet the following requirements, measured with respect to the master source.

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Timing drift	<1ps/day, <5ps long term.
Timing drift rate	<1 fs / second for times longer than 1 second.
RF phase noise relative to reference	<1fs integrated 1Hz to 10KHz
Fiducial	Able to identify a single RF cycle.

11 Long Haul Phase Transmission

This system transports the RF phase reference from the end of the SC accelerator to the end of the undulator hall, a distance of approximately 4Km. The RF phase will be measured relative to the beam and drift corrected by the Bunch Arrival Time monitor system.

11.1 Required Performance

The Long Haul phase transmission system must meet the following requirements

Timing Drift	<100ps long term	Need to identify single cycle of S-band measurement cavity in BAT monitor
Timing drift rate	<1fs/second	
Phase noise	<5fs integrated from 1Hz to 100KHz	Relative to the accelerator RF reference.
Fiducial	Able to identify a single RF cycle	

11.2 Implementation

The specific implementation of the long haul phase transmission system is not a requirement, but an example is provided for reference. Other implementations must meet the requirements of section 11.1 and verify compatibility with other sub-systems.

The phase can be transmitted as 325MHz with the fiducial described in 8.5 on low loss RF cable (Heliax or similar) in the accelerator housing. At the receive end in the undulator hall, a low bandwidth PLL is used to remove any noise added by acoustic or other effects in the cable. This is the scheme currently used in LCLS-I

Note that it may be possible to use diplexers to add the 325MHz to the existing cable used for 476MHz for LCLS-I.

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