

LCLS2 - LLRF - Latency accounting

- 50 ns input analog BPF
- 60 ns ADC pipe (7.5 cycles at 125 MHz)
- 180 ns DSP (22 cycles at 125 MHz)
- 530 ns bandpass filter in DSP (300 kHz)
- 70 ns notch filter in DSP (800 kHz notch, see unnotch.m)
- 100 ns compute amplitude with CORDIC (12 cycles at 125 MHz)
- 100 ns PWM generation (dual 2.6 MHz)
 - 0 160 ns DSP to generate class-F drive vector
 - 0 20 ns DAC
 - 0 20 ns sideband selection filter
 - 0 70 ns L-band analog gain stages
- 240 ns class S modulator analog (see class_s/design.txt)
- 100 ns high-power RF cavity filter (1.6 MHz bandwidth)
- 50 ns cables and waveguides
- 80 ns contingency
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- 1560 ns total, can sustain 64 kHz closed loop bandwidth

slightly obsolete because we think the amplifier will be "conventional" instead of class F+S, Chris Adolphson quoted 300 ns for the LCLS-II SSA in a PRD.