

**Requirements for FPGA/digital board for SLAC/LCLS-II LLRF**  
DRAFT 2015-05-14 LRD

Will be used for  $1 \times$  PRC and  $2 \times$  station controller,  $1 \times$  interlock, and  $1 \times$  resonance control chassis, per each LLRF rack. That will amount to over 350 installed in the machine.

Electrically (but not mechanically), this is a dual LPC FMC carrier, using FMC standard connectors. Only LVDS/LVCMOS pins are required on the FMC connectors, not the gigabit links. A total of 136 pins are categorized as user I/O according to FMC terminology, not counting clocks and FMC-mandated housekeeping. Any bank voltage between 1.8V and 3.3V is OK from an LVCMOS perspective, but the bank voltage must be set to something compatible with LVDS input and output (2.5V for HR, 1.8V for HP).

*rationale: allows prototyping and testing of peripheral modules with existing boards, e.g., BMB7 and KC705. At least one of the daughter cards designed for it will not conform to the mechanical part of the FMC standard. 136 pins are enough to cover all the LLRF daughter card needs.*

Two QSFP cages, fully routed to eight FPGA GT\* ports, each supporting at least 4 Gbaud. Direct or indirect attachment of QSFP I2C management interface to FPGA.

*rationale: basis for rack architecture. Functions could almost be accomplished with one cage, but need two Xilinx GT\* quads to provide enough clocking resources for feedback, timing, and global controls (see below). Optical power readouts are essential to show proper fiber installation.*

Option, alternative to above requirement:  $1 \times$  QSFP,  $2 \times$  SFP.

*rationale: could give more flexibility for attachment to long-haul fibers. Six fibers cover known use cases.*

Clock signals provided to GT\* reference pins must include:

- FMC CLK0\_M2C (nominally 188.6 MHz) to support 3.771 Gbaud
- On-board low jitter clock(s) supporting 3.714 Gbaud and 1.25 Gbaud

*rationale: LLRF feedback, timing, and Ethernet, respectively. Ethernet is one option for connection to Global Controls.*

One 8P8C gigabit Ethernet, RGMII or GMII PHY, directly attached to the FPGA fabric.

*rationale: ease of bench testing, quick attachment to laptop.*

At least 2 LEDs, directly mapped to individual FPGA pins, visible from the panel edge. Color unspecified, can be chosen to match typical SLAC practice. LEDs embedded in the 8P8C connector can be used to meet that requirement, if such a connector fits the mechanical envelope. Light pipes associated with the QSFP modules probably won't fit the mechanical envelope.

*rationale: to be used for heartbeat or other locally interesting status readout, especially when installing a chassis in the rack.*

Two dual-row Pmod interfaces, 16 user I/O total.

*rationale: flexibility of attachment of ancillary devices, like front-panel LEDs, or thermal control/monitoring.*

JTAG interface for board bring-up, 14-pin 2 mm Xilinx header.

*rationale: compatibility with Xilinx and 3rd party programming tools.*

7-series FPGA: XC7A100T, KC7K160T, or larger.

*rationale: test builds of Ethernet+controller+simulator+waveform acquisition, brainlessly doubled for a two-cavity controller, take 47% of the XC7A100T fabric, and 49% of its multipliers, close to the usual 50% mark for the prototyping phase. We can wildly guess that the known missing features (e.g., timing client, output upconverter, quench detector) are roughly compensated by duplication of shared features (e.g., the Ethernet stack and digital LO generation).*

Limit power dissipation to 12 W, including  $2 \times$  QSFP at 1.5 W each, running production code with six GT\* lanes configured and running. To be conduction cooled from the FMC connector side, see drawing. Board and heat spreader assembly to attach to chassis cold plate with four M3 bolts. The air surrounding the board is still, and fans are not allowed.

*rationale: thermal management in the chassis has to account for 16 W of analog gear spread out over  $0.12 \text{ m}^2$ . Allocating 12 W to  $0.02 \text{ m}^2$  is already somewhat of a mismatch. Existence proof (BMB7) that a board meeting these goals can be built with today's technology. Fans would introduce reliability, maintenance, and vibration concerns.*

Power input is +12V; a simple FET switch can connect this to the FMC 12P0V pins supplying the daughter card(s). On-board monitoring of voltages, currents, and temperature (Xilinx 7-series chips have internal temperature readout). Must read out at least voltage present at +12V input, total current drawn from +12V input, and FPGA core current. The board must enter a low-power state ( $< 100 \text{ mW}$ , daughter card 12P0V turned off) if an over-temperature condition is detected.

*rationale: verify thermal environment, prevent damage, and characterize bitfile-dependent dissipation.*

All on-board switching regulators must be synchronizable by an FPGA I/O pin. Best practices should be used to minimize their radiation of harmonic energy to the analog board attached to the FMC connector.

*rationale: this board is mounted close to, and electrically connected to, an analog board sensitive to attowatts of interference. An interference line that is pinned to the ADC clock can in principle be filtered out digitally.*

Dimensions: 140 mm wide (matches dual FMC form factor), length negotiable in 120 mm to 160 mm range (but that needs to be decided early, to allow progress on chassis design). No more than 4.0 mm overhang beyond FMC connectors.

*rationale: leave enough space in standard 19" chassis for RF and analog gear. Small overhang allows access to test points on DAQ daughter board. Measured overhangs: SP605=1.3 mm, AC701=1.1 mm, ZC706=1.5 mm, KC705=1.7 mm.*

Power entry (+12V, see above): two connectors, electrically paralleled. Rear panel, 2.5 mm barrel-type for wall-wart. Interior MTA-156 for in-chassis wiring to filtered distribution.

*rationale: barrel connector makes testing easy. Interior connector is negotiable, but MTA-156 is rugged, readily available, and consistent with production of a chassis wiring harness.*

Self-booting from on-board Flash memory in less than 3.0 seconds. Un-brickable mechanism for remote (fiber or 8P8C) bitfile update (Flash erase+write) in less than 60 seconds.

*rationale: don't want servers hammered with 350 boot requests after a power outage; scope of programming is beyond what can be fully specified and validated before hardware installation; nobody wants to walk the linac with a JTAG cable after a summer student makes a stupid mistake at 3am.*

Prefer, but do not require, an FPGA that is supported by WebPACK: any Artix, or Kintex '160T and smaller.

*rationale: one less license file to worry about; but production bitfiles could be generated on a central server.*

Mechanical: FMC board-board spacing is 10.0 mm (not 8.5 mm), determined by daughter board FMC connector choice. The FMC standard refers to the carrier board side with this connector as side 1. Component height on side 2 is limited to 12 mm. With a heat spreader attached to side 1, the heat spreader mating surface that will transfer heat to the chassis cold plate must be 12.0 mm from the side 1 surface. See drawing.

*rationale: keep the chassis mechanical design simple and as non-specific as possible, just a flat aluminum plate with mounting holes.*

Early documentation required:

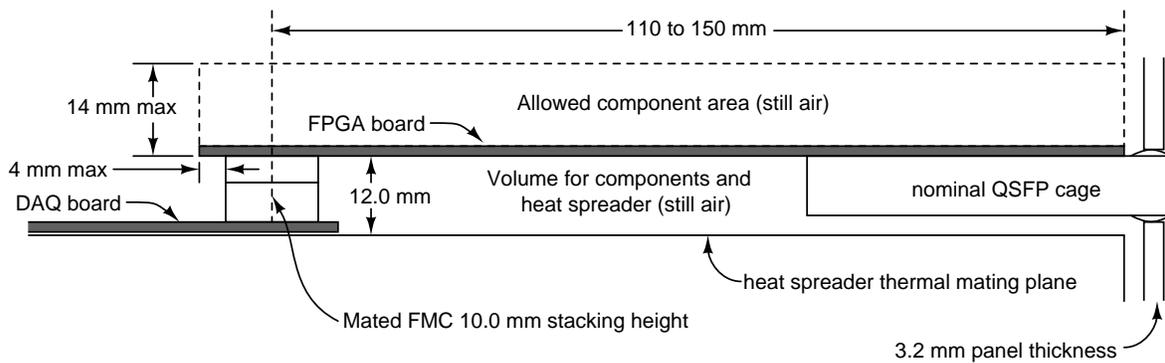
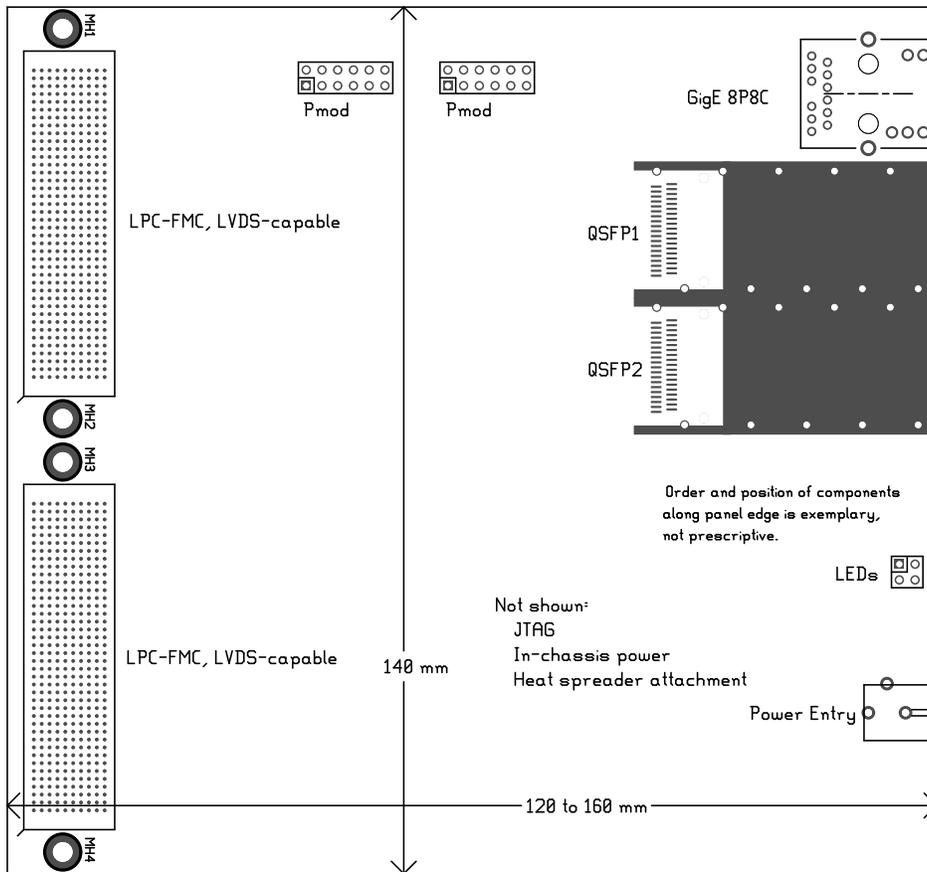
- Overall dimensions relative to FMC connector, including heat spreader
- FMC pin mapping

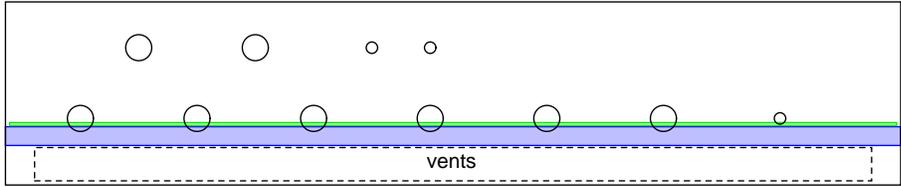
Mid documentation required:

- Connector placement
- Full pin mapping
- Mounting bolt pattern (attachment of assembly to chassis cold plate)

Not addressed here: support for hard and soft core CPUs, off-chip RAM.

*rationale: those features are not essential for supporting the feedback loops, internal diagnostics, setup, or analog performance of the chassis. They can be added, if desired, staying within the above constraints.*

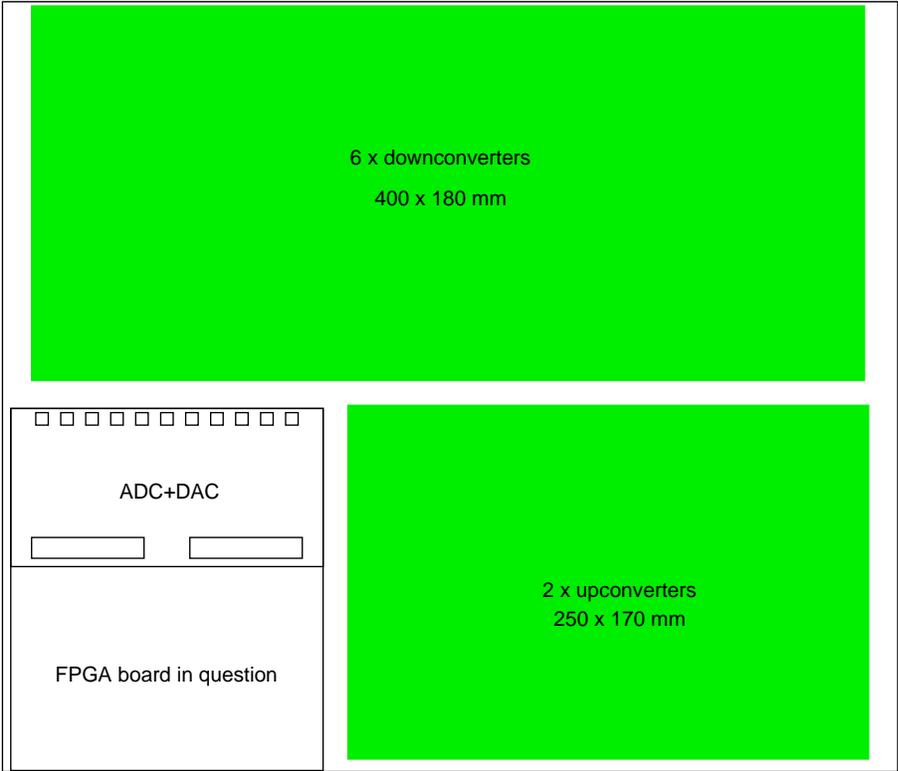




2 x SSA out, 2 x loopback out

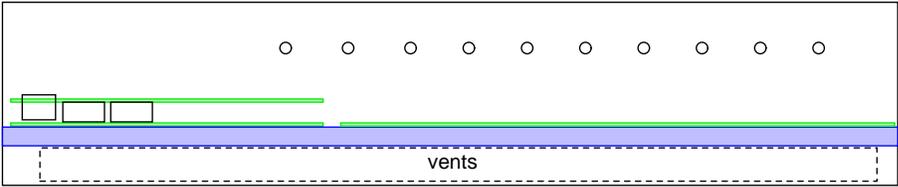
6 x RF in, 1 x LO

"Back"



2U chassis  
430 x 370 mm

"Front"



8 x RF monitor, 2 x spare IF in

1 x 8P8C, 2 x QSFP

← 4 kg aluminum plate

Chassis-level context for this board; RF station configuration