U.S. MAGNET DEVELOPMENT PROGRAM

# Electronics Developments

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**For Lawrence Berkeley National Laboratory, Superconducting Magnet Group**

# Related Diagnostics Milestones

AIIId-M04 – Test of a large-scale Hall array and imaging current distribution HTS tape stacks and coils

AIIId-M07 – Development of multi-element and flexible quench antennas and localization of quenches in using flexible quench antenna arrays

AIIId-M09 – Development and test of a standalone acoustic quench detection and localization FPGA-based system

AIIId-M11 – Demonstration of programmable fully-cryogenic FPGA “smart” sensor core with digital readout and analog front-end (SQUID) amplifiers

# Cryogenic DAQ Elements

**Integration**
- Digital C&C
  - Microprocessor
  - FPGA
- Power
  - External Lines
  - Local
    - Optical
    - Linear Regulation
    - Capacitive Pump
- Substrate
  - Ceramic
  - FR4
  - Polimide
- Traces
  - Copper
  - Aluminum

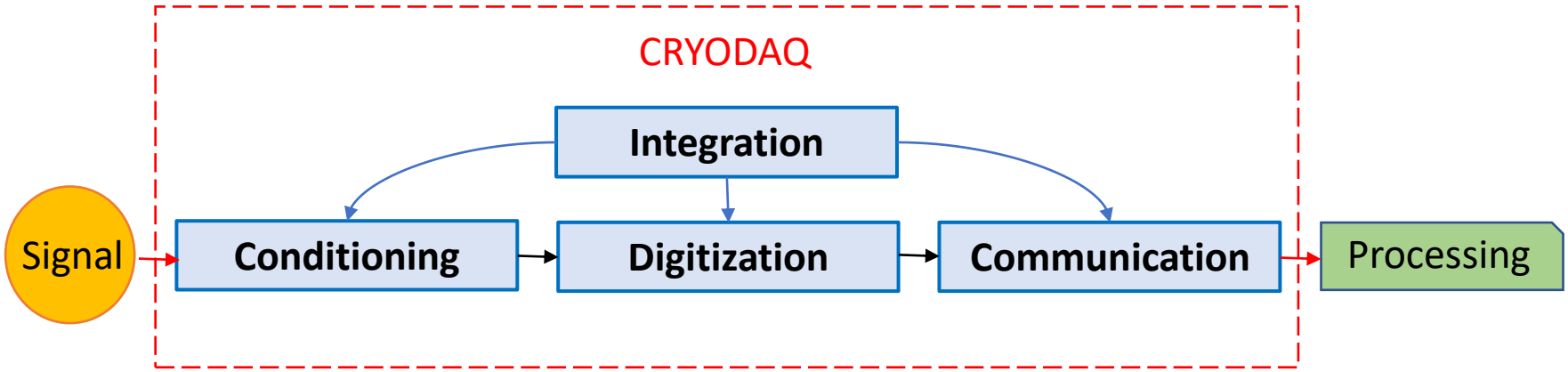
**Conditioning**
- Impedance match
- HV Isolation
- Gain
  - Fix
  - Adjustable
- Filter
  - Passive
  - Active

**Digitization**
- Resolution
  - Low (6-8 bits)
  - Medium (10-16 bits)
  - High (24-32 bits)
- Sample Rate
  - High (500-5000 MSPS)
  - Medium (10-200MSPS)
  - Low (1SPS-1MSPS)

**Communication**
- Architecture
  - Serial
  - Parallel
- Physical Level
  - Wire
  - Optical
- HV Isolation

* In red DAQ characteristics currently pursued by LBNL for first prototype

# Cryogenic DAQ Architecture




Characteristics of the DAQ, specially conditioning and digitization are very dependent on the application. Typical sources of signals in a magnet test are;

- Strain Gauges, Temperature: ADC (Low Sample Rate, High Resolution)
- Acoustic Sensors: ADC (Medium Sample Rate , Medium Resolution)
- Voltage Taps: ADC (Medium Sample Rate , Medium Resolution) + Optical Isolation

Another very important consideration is number of channels. This together with the ADC sample rate will determine the requirements for the communication module.

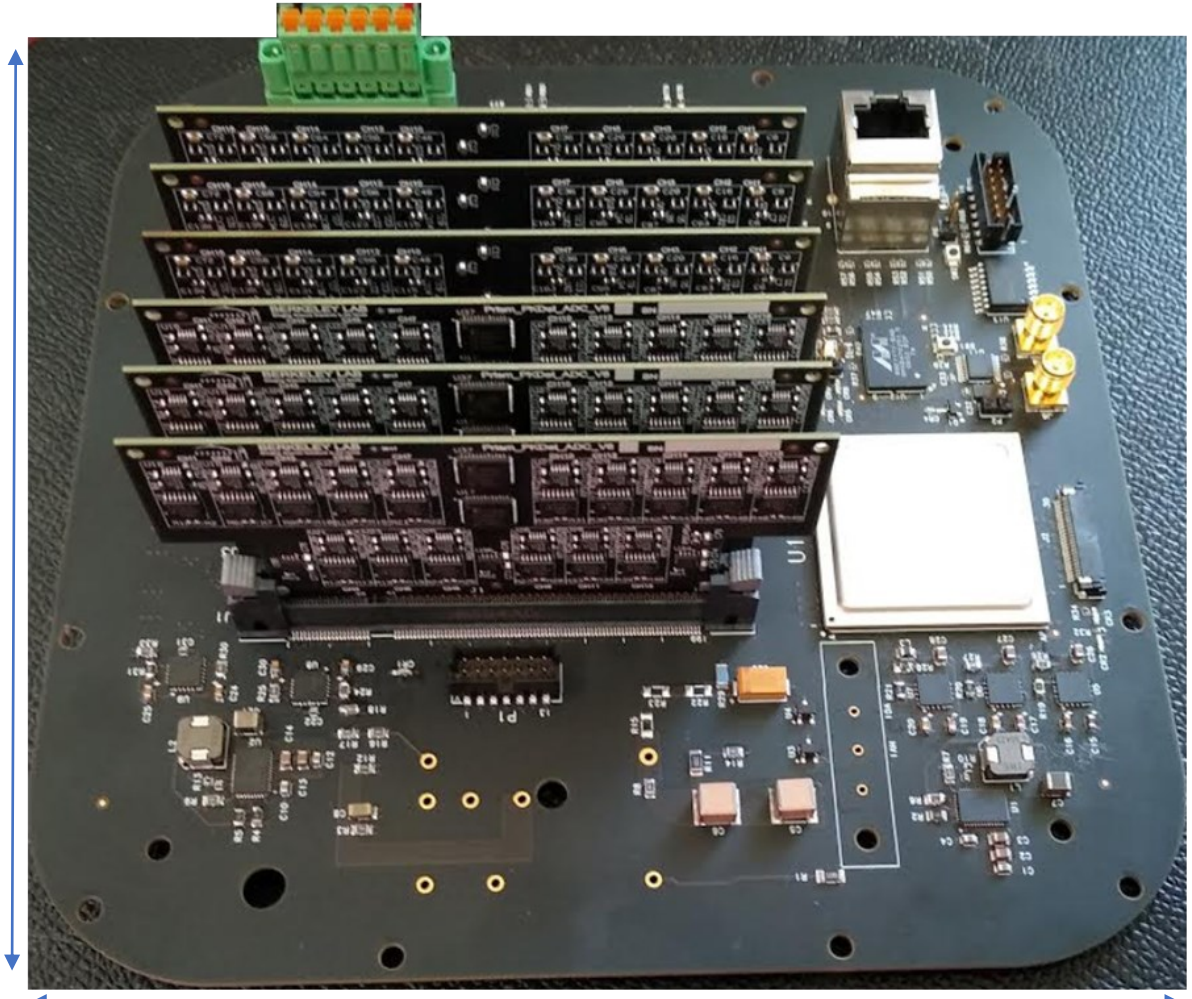
# DAQ Hardware Under Development

At LBNL we currently have three systems under development

- 192 channels multipurpose room temperature DAQ
  - FPGA based + 6 daughter cards
  - Current version 3 MSPS, 14b per channel
  - 1GB/s link Ethernet Link
  - 1MB cache Memory
- 64 channels room/cryogenic DAQ
  - FPGA based + 2 daughter cards
  - Current version 65 MSPS, 14b per channel
  - 1GB/s link Ethernet Link (Warm) / 6.6Gb/s GTP (Cryogenic)
  - 1MB cache Memory
- 8 channels cryogenic DAQ
  - 1 MSPS, 16b per channel
  - 6.6Gb/s GTP (Cryogenic)
  - 100kB cache Memory

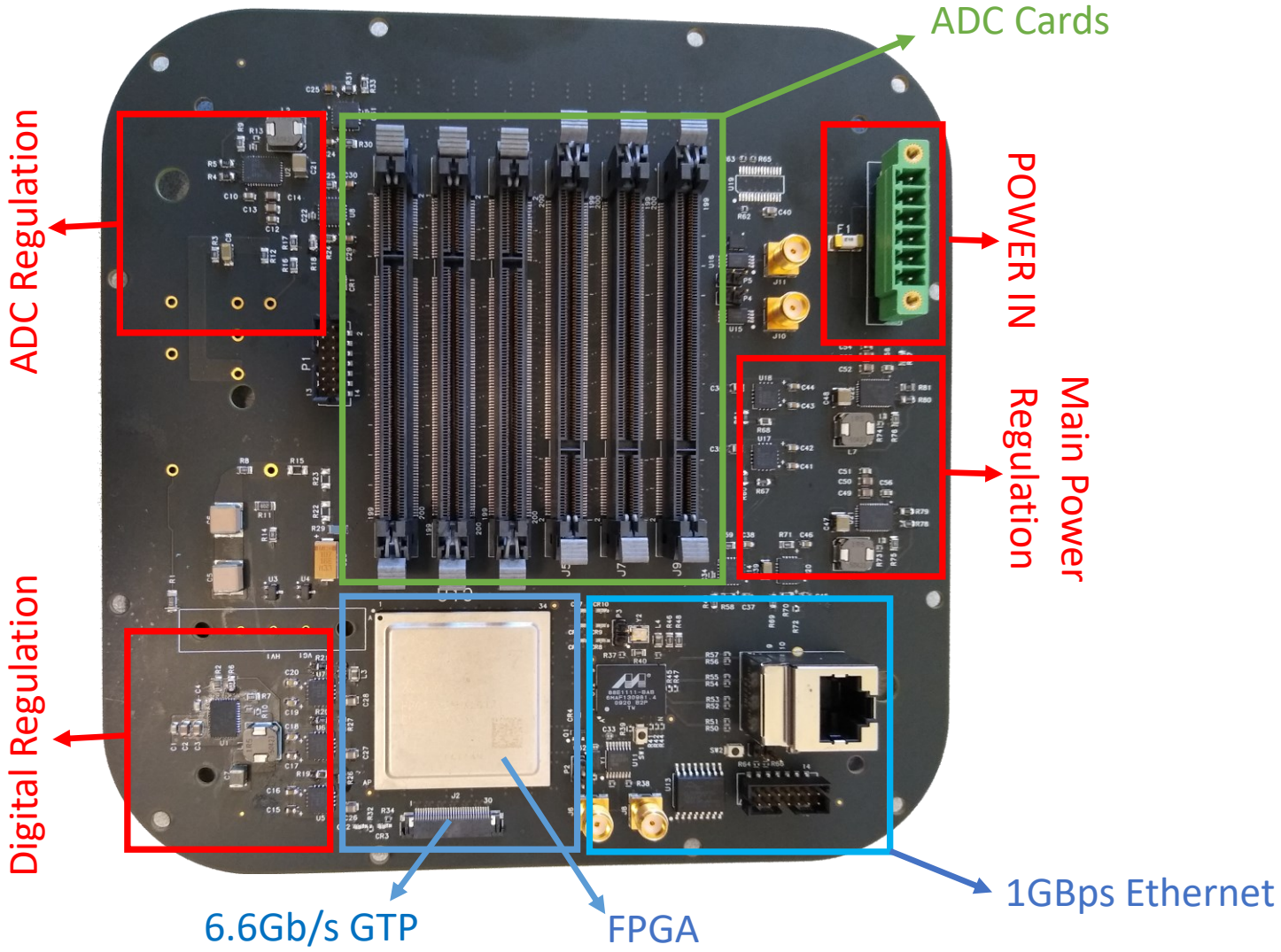
# Multipurpose room temperature DAQ

LBNL (Supercon and Nuclear Science)



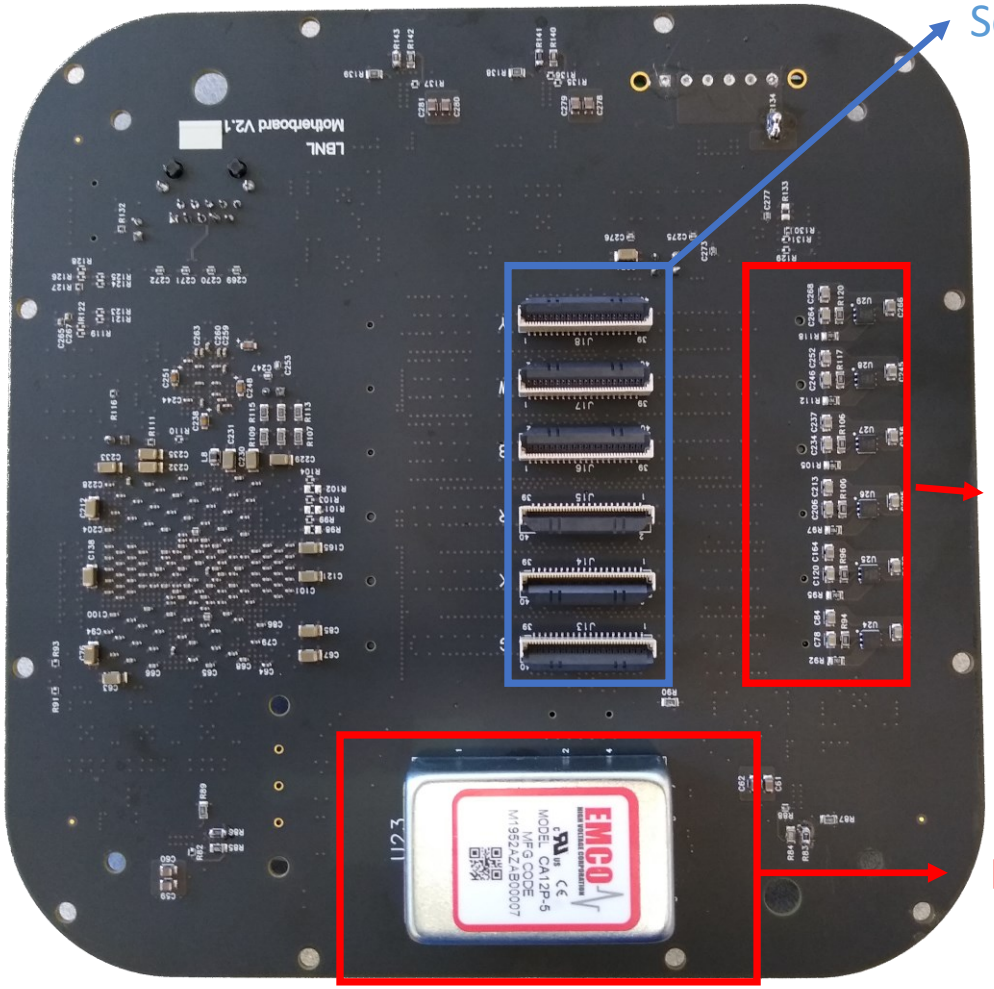
# Multipurpose room temperature DAQ

**TOP**



# Multipurpose room temperature DAQ

**BOTTOM**

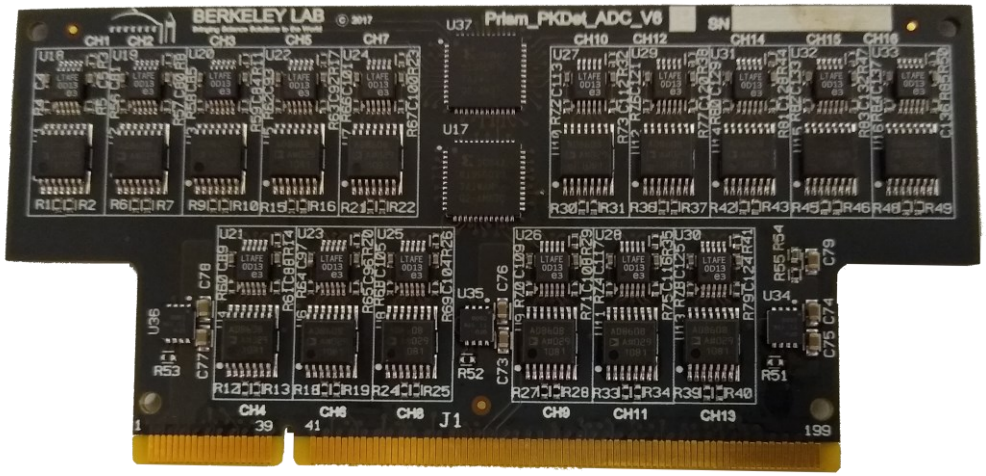


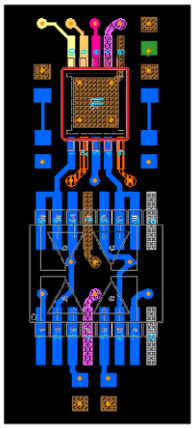

Sensor Interface

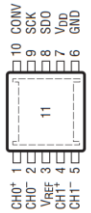
Detector Power Regulation

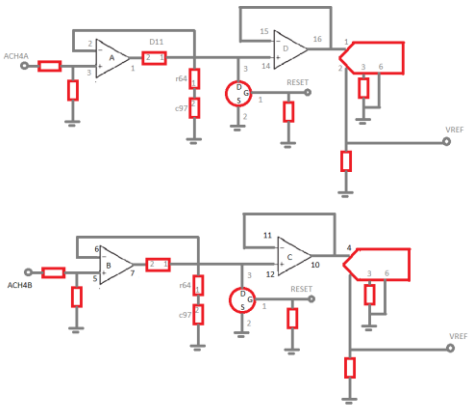
High Voltage Bias

# Daughter Card type AAPh



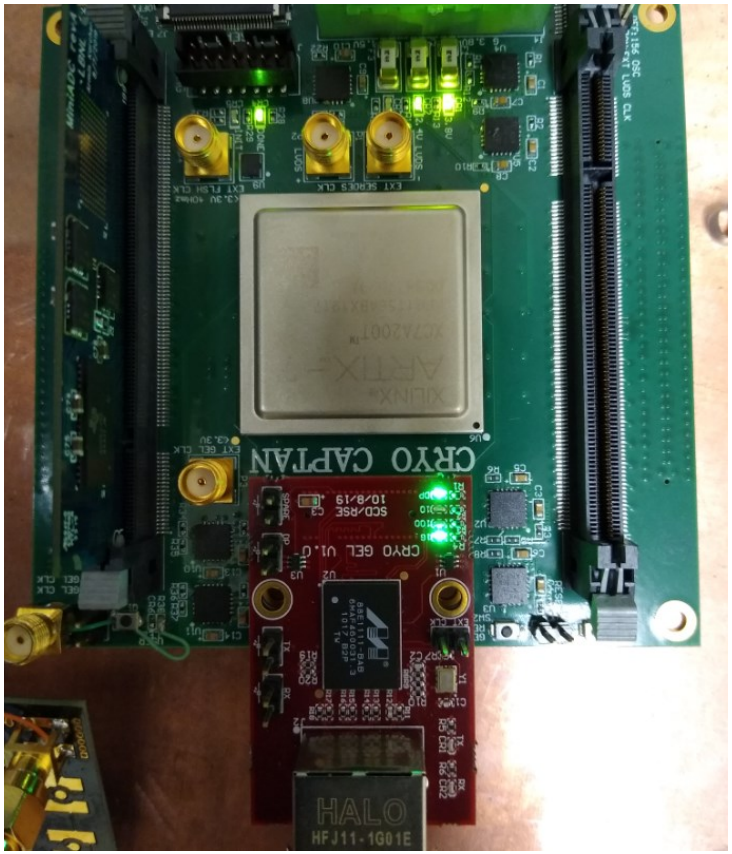



- 32 channels
  - 3 MSPS, 14b per channel
  - Peak Hold Capability
  - Amplifier circuit with gain up to 100x
  - 0V to 2.5V Unipolar Input Range

# Cryogenic DAQ Prototype

LBNL / FERMILAB COLLABORATION



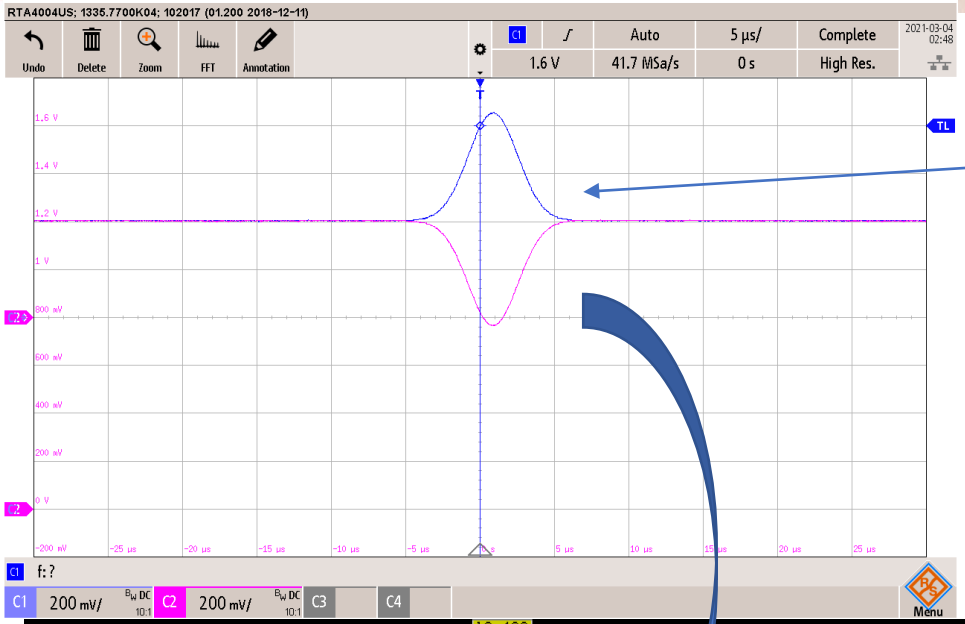

- 3.75” x 3.75”

- Currently a technology demonstrator platform.
- Testing FPGA, LDO (Linear Regulator), and communications;

- FPGA already proven to work in LHe.;
- 6.6Gb/s GTP (Cryogenic) on copper

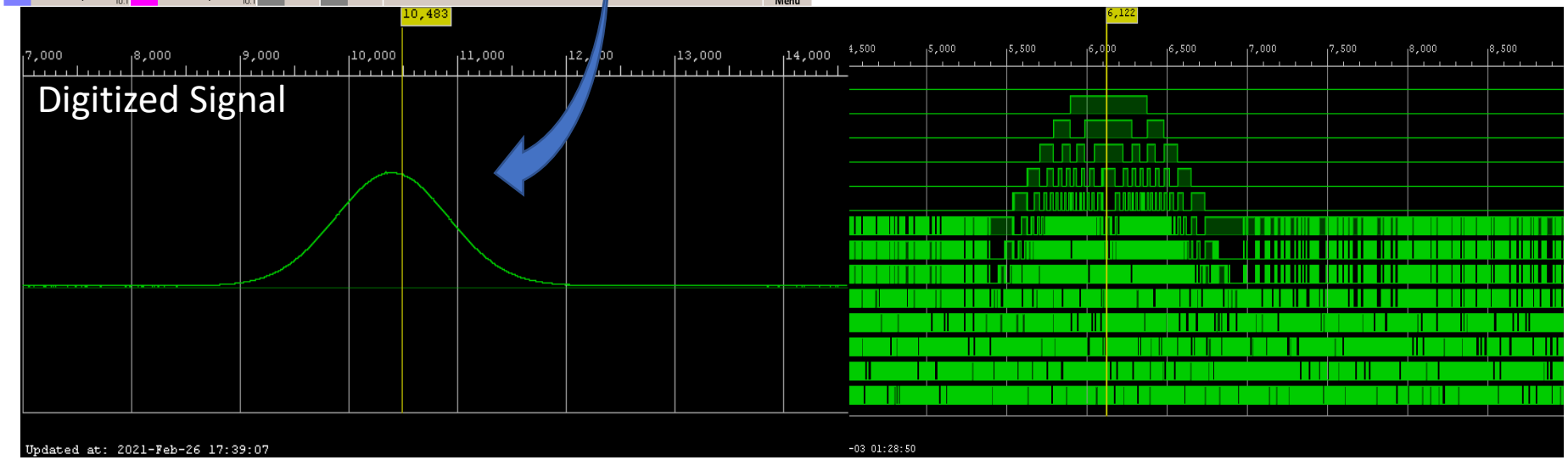
- 64 channels
  - 100 MSPS in 10-Bit Mode
  - 80 MSPS in 12-Bit Mode
  - 65 MSPS in 14-Bit Mode

# Cryogenic DAQ Evaluation



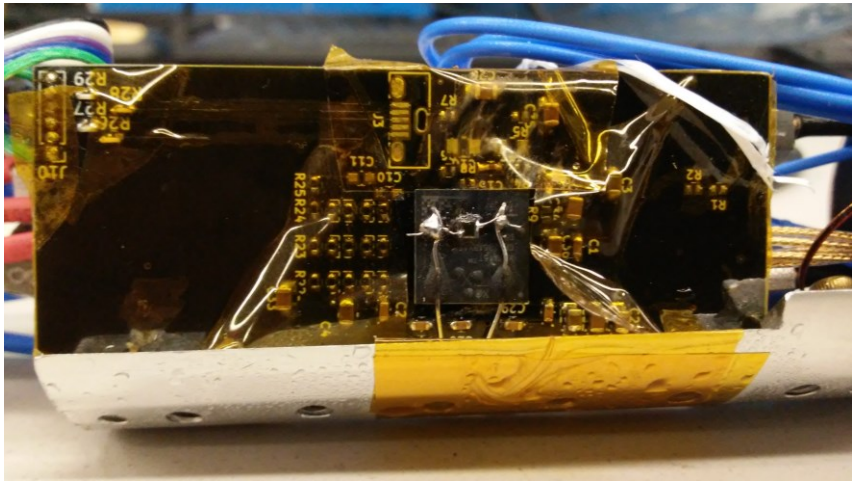

Analog differential Gaussian signal (Oscilloscope Capture)

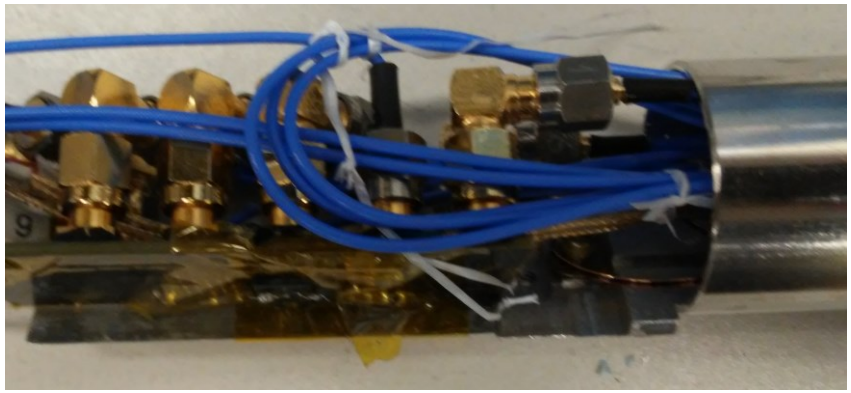
Test Performed at 62.5MSPS/14 bits



# Cryogenic DAQ Prototype

LBNL / BLEXIMO





Developed to characterize the FPGA performance at deep cryogenic temperatures;

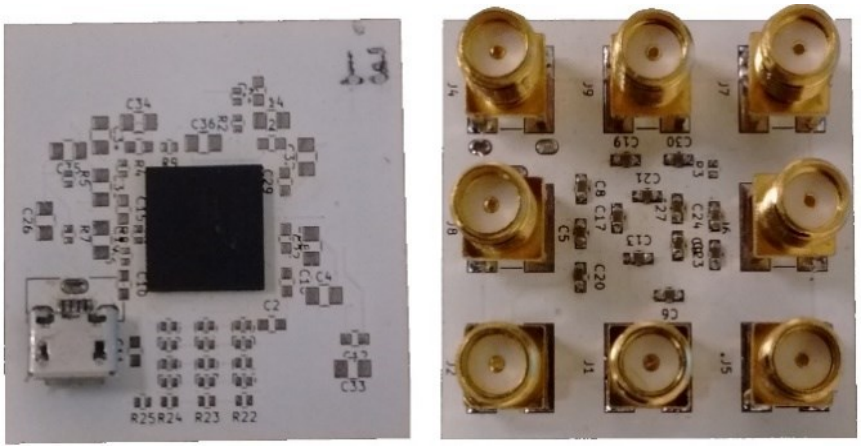
Target FPGA already tested and proven to work in LHe and at temperatures in the range of 4.2K to 20K.

Current board thermal cycled from room temperature to under 20K more than 20 times including LHe submersion.

Hybrid 4bits flash ADC also successfully tested with this board.

***Maxim Marchevsky Test Platform with Bleximo support**

# Cryogenic DAQ Prototype



Current capability

- 8 channels at 125 kSPS
- 12 bits

Or

- 1 channel at 500 MSPS
- 4 bits

New Board

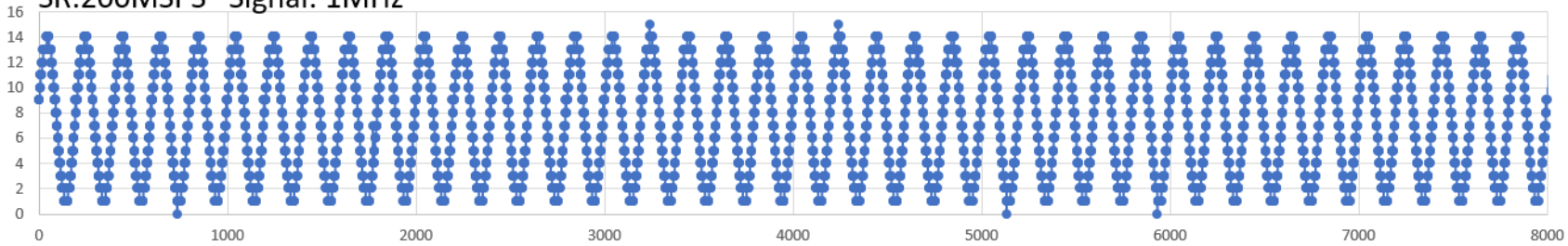
- 8 channels at 1 MSPS
- 16 bits
- Isolated Front end
- 6.6 Gbps copper link

*Will be presented at IEEE 14th Workshop on low Temperature Electronics April 12-15 2021

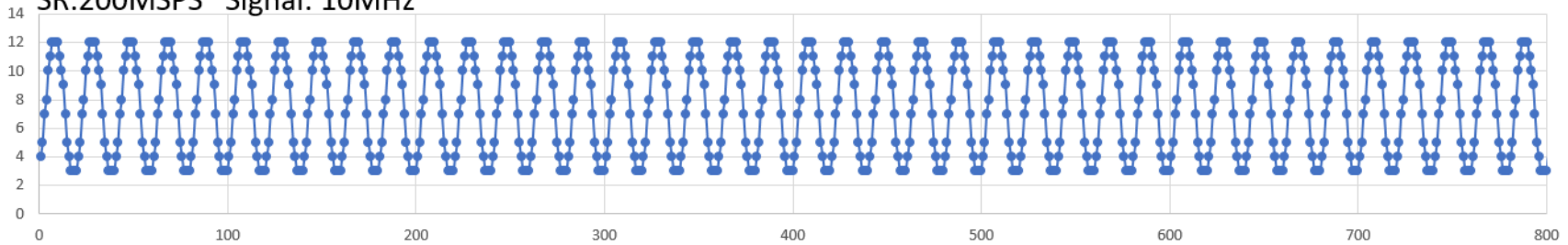
# Cryogenic DAQ Results

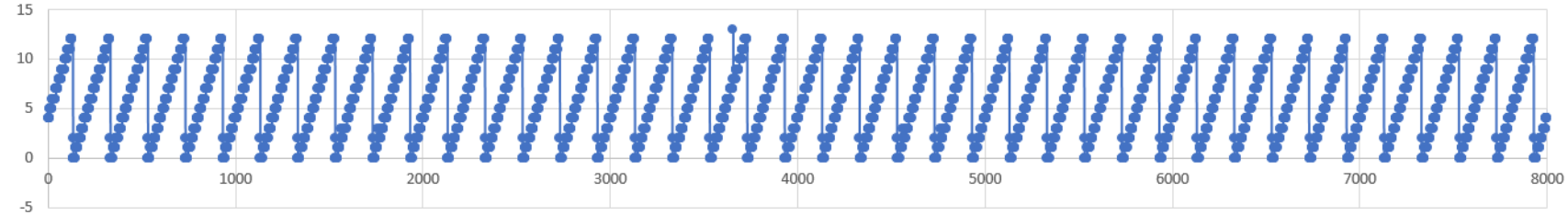
4bADC FPGAflash ~7K

SR:200MSPS Signal: 1MHz



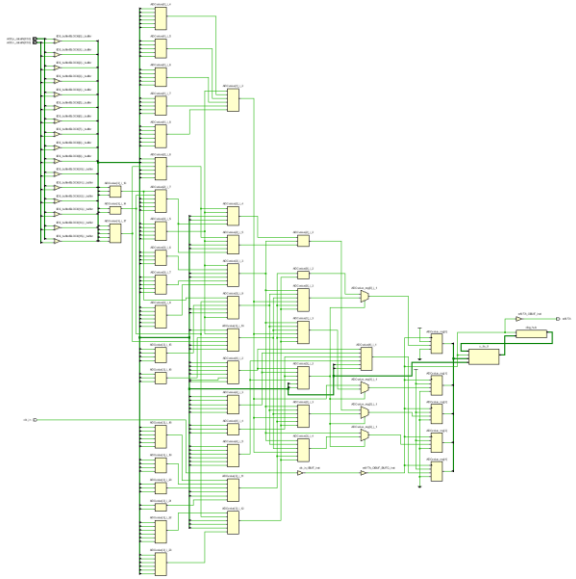

SR:200MSPS Signal: 10MHz



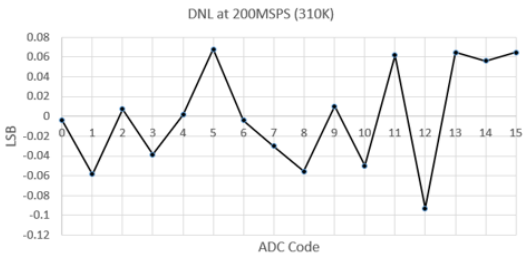



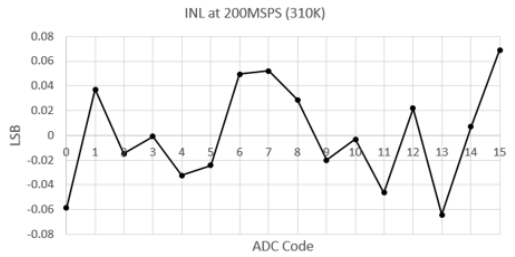

SR:20MSPS Signal: 500kHzCode error here. Still calculating code error rate. Design not optimize to minimize code error.

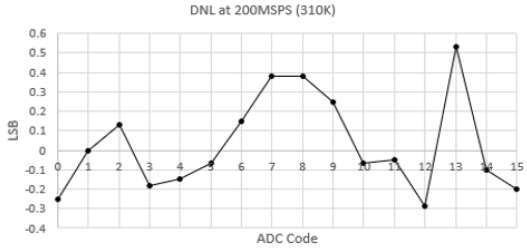
# 4b ADC FPGAflash

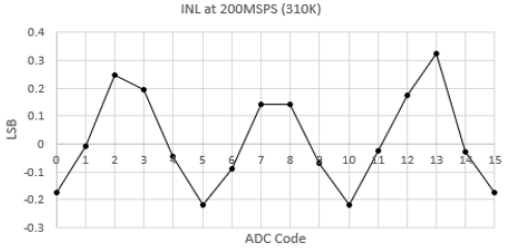


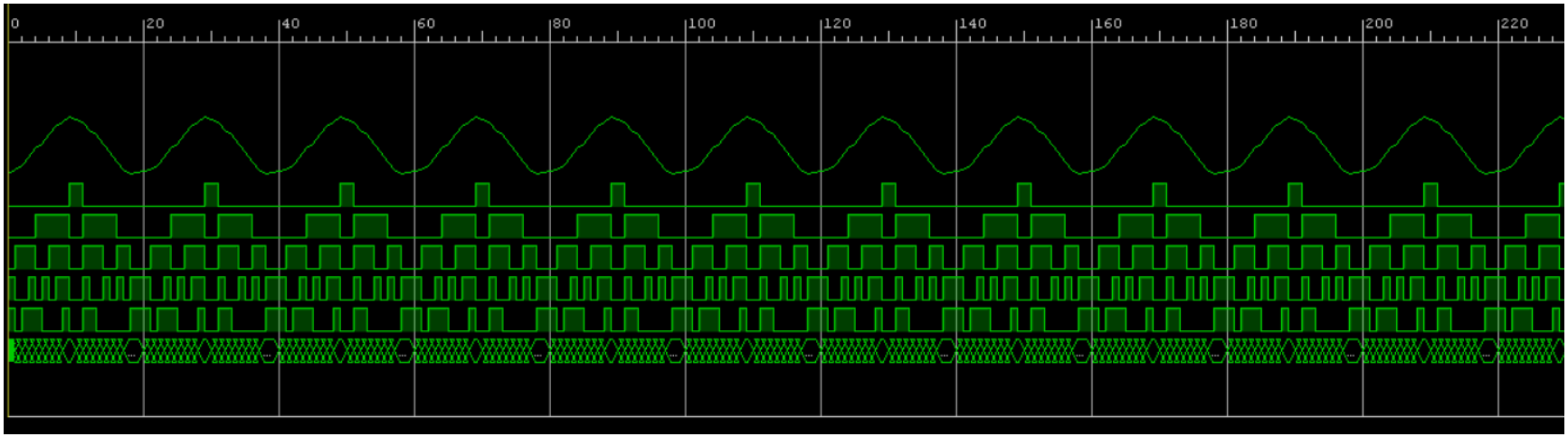
## Noise Performance



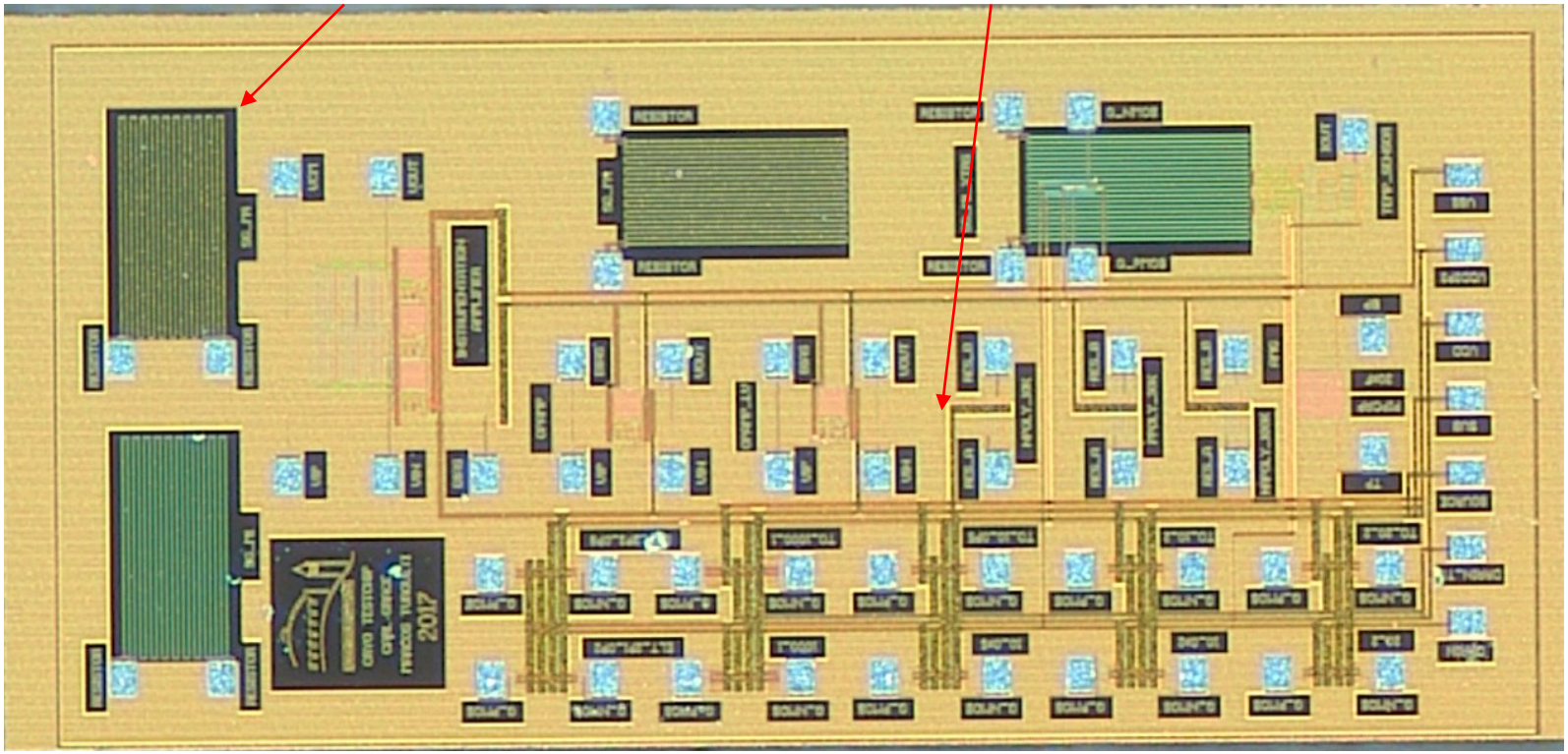



# Cryogenic Integrated Circuits

Strain Gauge

Amplifier



*Carl Grace / Marcos Turqueti test ASIC

Also available for LHe testing:

- 16 channels ADC
- Operational Amplifier

# Conclusion

- Many options available for cryogenic data acquisition
- COTS components can be used after rigorous evaluation
- Growing number of Applications Specific Integrated Circuits (ASICs) available
- Software developed needed
- More collaboration needed between potential users

# Collaborators

**Fermilab**

Ryan Rivera (Computing Division)
Lorenzo Uplegger (Computing Division)

**LBNL**

Maxim Marchevsky (Supercon)
Carl Grace (Engineering Division)
Paul Barton (Nuclear Science Division)
Josh Cato (Nuclear Science Division)

**Bleximo**

Private partner through Cyclotron Road