RNC Instrumentation

Large Instrumentation Projects:

Silicon MAPS based vertex detectors in the RNC group

Outline

- MAPS sensors
- STAR HFT detector
- ALICE ITS Upgrade
- Future applications

What are MAPS sensors?

Charged particle tracking detectors at large experiments rely on silicon pixel sensors to provide high resolution hit points for pointing and vertex determination.

Standard planar hybrid pixels

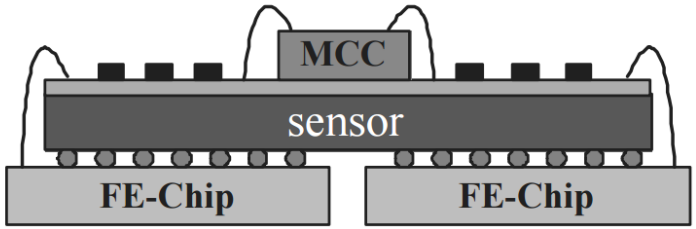
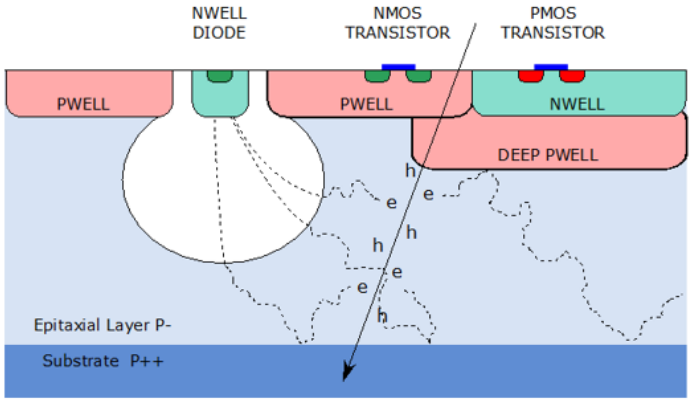


Fig. 1
CROSS-SECTION OF AN ATLAS PIXEL MODULE.

- Signal generated in detector silicon.
- Signals processed by front end chips bump bonded to detector silicon.
- Typical thickness total ~300 µm.
- Pixel size typical 50 µm x 400 µm.
- Radiation tolerance ~50 Mrad.
- Radiation length (per layer) ~2.5% (includes support structure and cooling).

Monolithic Active Pixel Sensors



- Detector and processing integrated into one silicon wafer.
- Signal generated in epi layer.
- Signals processed in circuitry integrated into matrix and on wafer.
- Can be thinned to 50 µm.
- Pixel size as small as 10 µm x 10 µm.
- Radiation tolerance ~3 Mrad.
- Radiation length (per layer) ~0.3-0.4% (includes support structure and cooling).

STAR PXL Detector

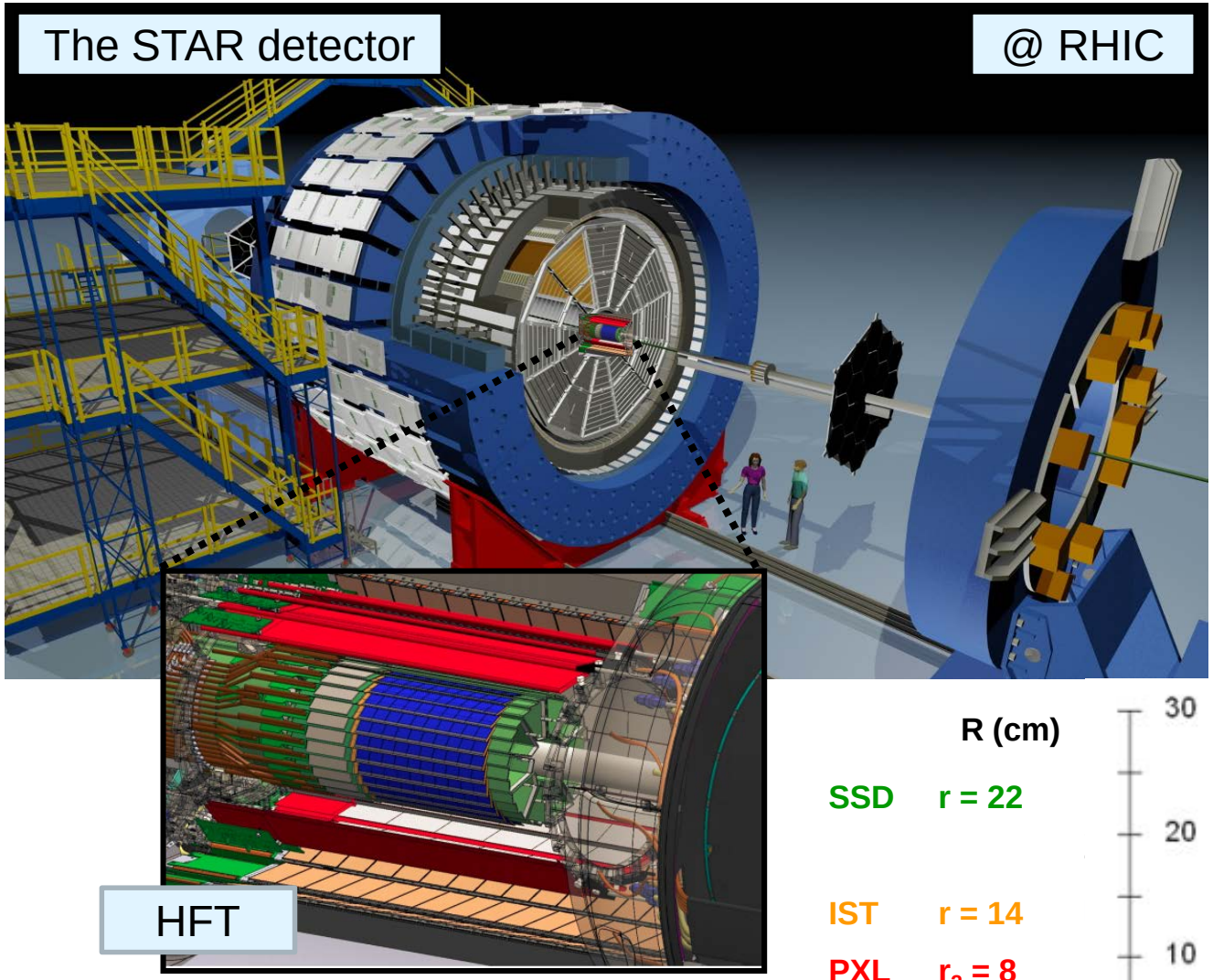
First vertex detector at a collider experiment based on ***Monolithic Active Pixel Sensor*** technology

- Conceived by Howard Wieman and the RNC group.
- Developed and constructed at LBNL.
- Project completed on time and under budget (2014) meeting all CD-4 parameters.
- The HFT upgrade took physics data in 2014, 2015, 2016 and has now completed the physics program.
- First results were shown in QM15 – see talk by Xin.

STAR HFT Upgrade

Extend the measurement capabilities in the *heavy flavor* domain, good probe to QGP:

- Direct topological reconstruction of charm hadrons (e.g. $D^0 \rightarrow K\ \pi$, $c\tau \sim 120\ \mu m$)



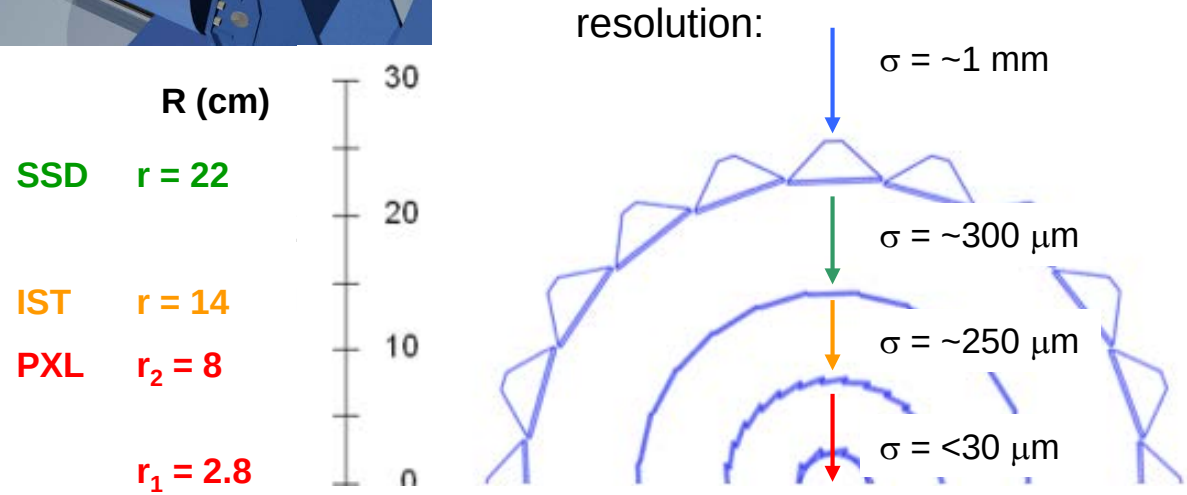
Need to resolve displaced vertices in a high multiplicity environment

TPC – Time Projection Chamber (main tracking detector in STAR)

HFT – Heavy Flavor Tracker

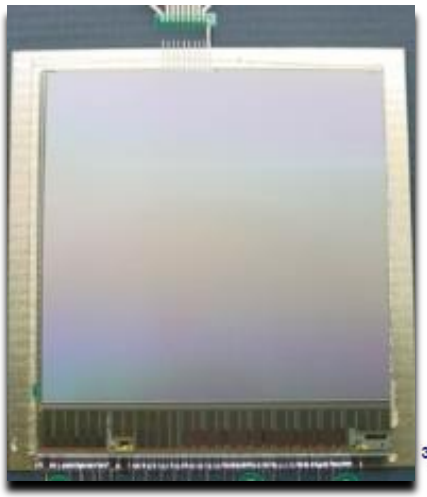
- **SSD – Silicon Strip Detector**
- **IST – Intermediate Silicon Tracker**
- **PXL – Pixel Detector**

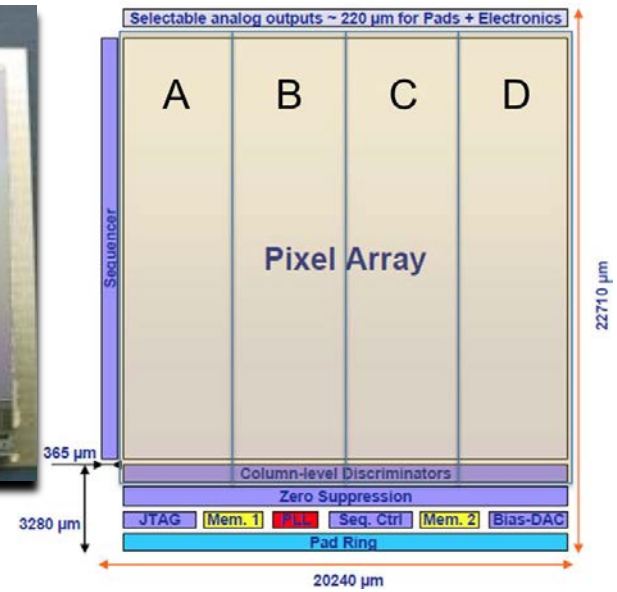
Tracking inwards with gradually improved resolution:

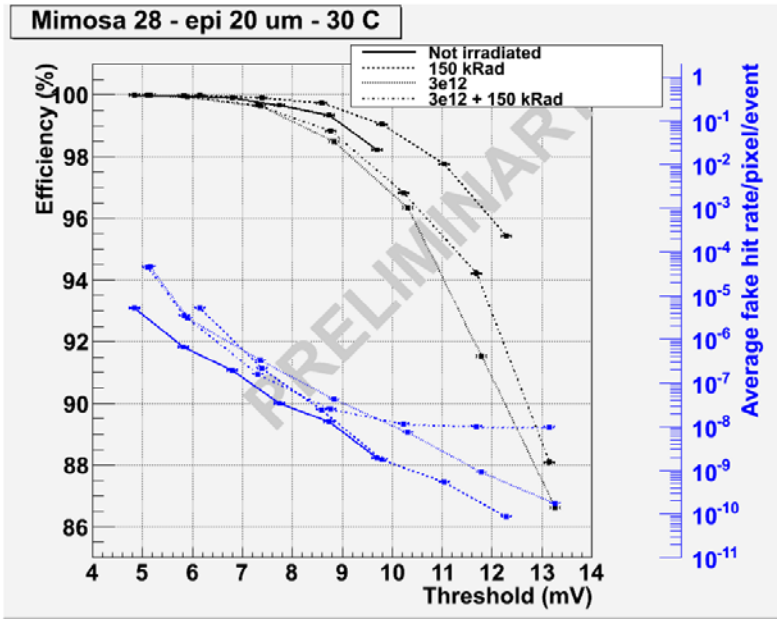


PXL detector Ultimate-2 Sensor

- Reticle size (~ 4 cm²)
  - Pixel pitch 20.7 µm
  - 928 x 960 array ~890 k pixels
- Power dissipation ~170 mW/cm² @ 3.3V (air cooling)
- Short integration time 185.6 µs
- In pixel CDS
- Discriminators at the end of each column (each row processed in parallel) – **Binary Output**
- 2 LVDS data outputs @ 160 MHz
- Zero suppression and run length encoding on rows with up to 9 hits/row.
- Ping-pong memory for frame readout (~1500 hits deep)
- 4 sub-arrays to help with process variation
- JTAG configuration of many internal parameters.
- Individual discriminator disable, etc.
- Built in automated testing routines for sensor probe testing and characterization.
- High Res Si option – significantly increases S/N and radiation tolerance.
- **Sensors thinned to 50 µm.**







Optimized for the STAR environment

Developed by PICSEL group of IPHC-Strasbourg

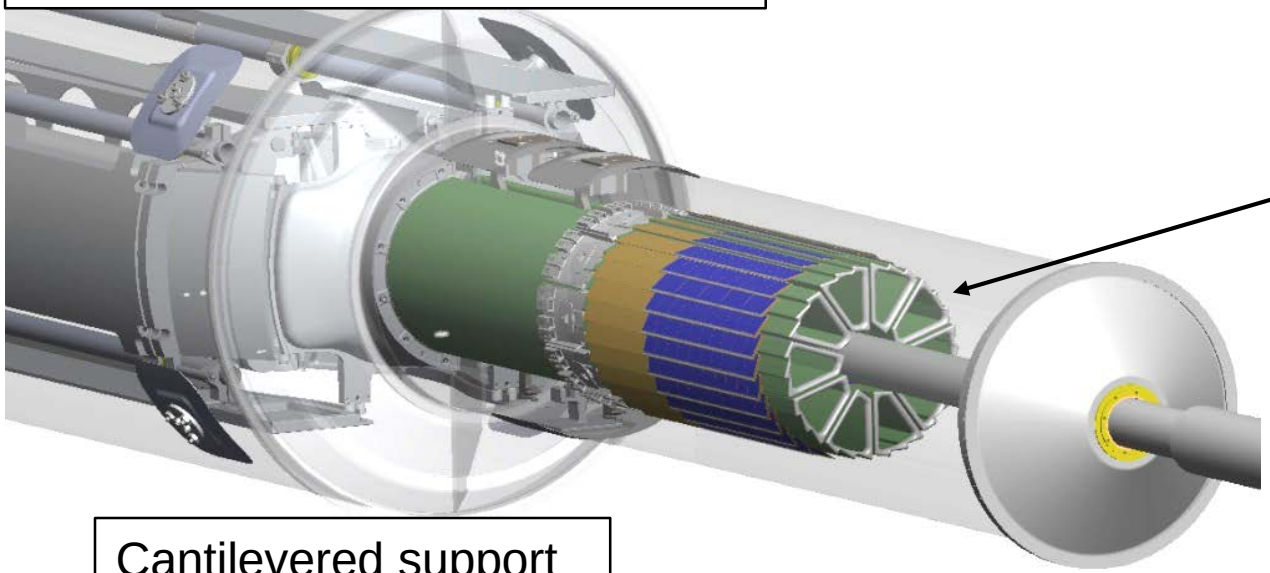
STAR PXL structure

Basic Detector Element

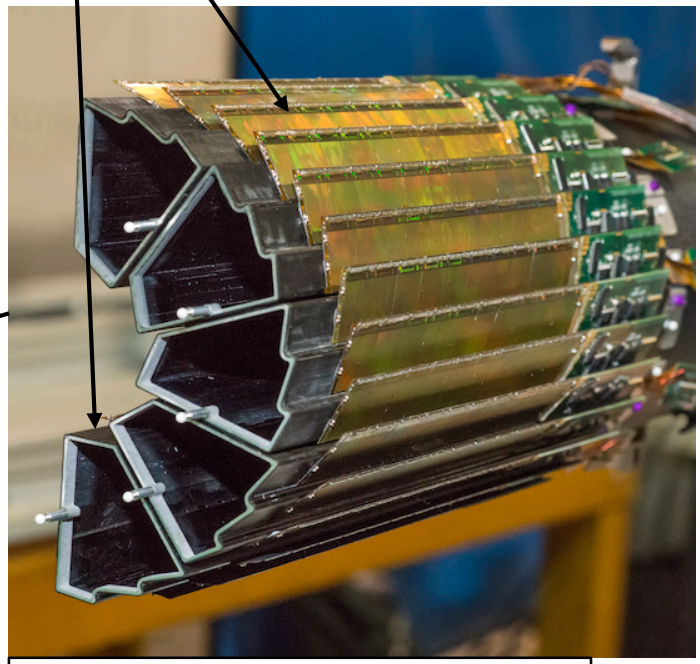
Ladder with 10 MAPS sensors (~ 2×2 cm each)

10 sensors / ladder
4 ladders / sector
5 sectors / half
10 sectors total

Mechanical support with kinematic mounts (insertion side)



Cantilevered support

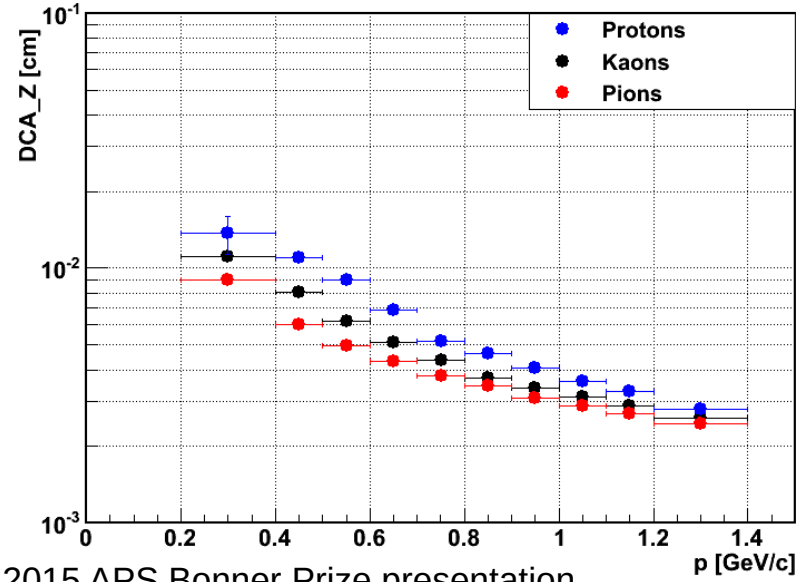


carbon fiber sector tubes (~ 200 µm thick)

HFT Performance from 2014 data

DCA pointing resolution

- Design requirement exceeded: 46 µm for 750 MeV/c Kaons for the **2 sectors** equipped **with aluminum cables on inner layer**
- ~ 30 µm for p > 1 GeV/c pions
- From 2015: all sectors equipped with aluminum cables on the inner layer

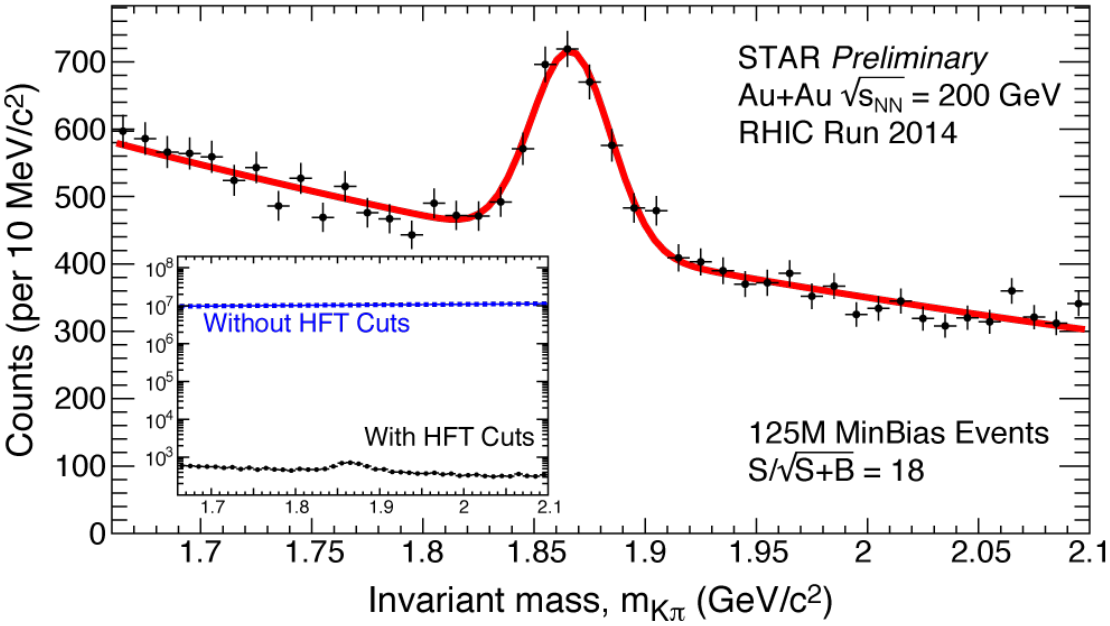


H. Wieman 2015 APS Bonner Prize presentation

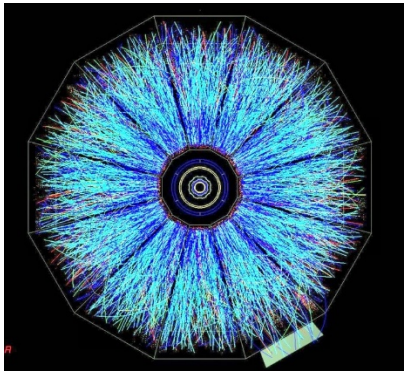
Physics of D-meson productions

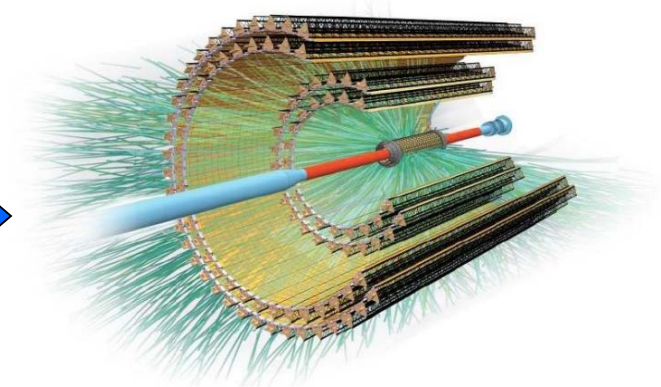
- High significance signal
- Nuclear modification factor R_{AA}
- Collective flow v_2

See first λ_c results in Xin's talk



ITS – next generation MAPS detector



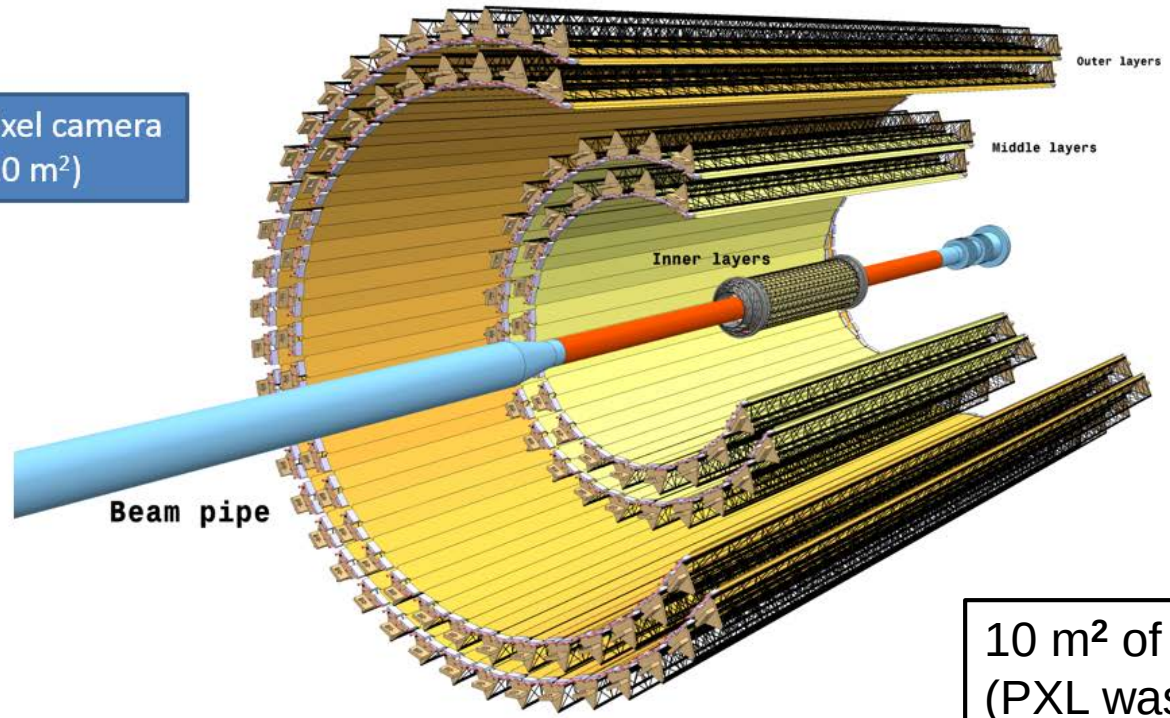


	STAR PXL	ALICE ITS
Silicon area	0.16 m^2	10 m^2
# pixels	356 M	12.5 G
# layers	2	7
Integration time	186 µs	10-20 µs
Trigger rate	~1 kHz	~100 kHz (p-p)
X/X_0 inner layer	~0.4 %	~0.3 %
RDO speed	160 MHz	1.2 GHz

ALICE ITS upgrade

New ITS Layout

12.5 G-pixel camera
(~10 m²)



10 m² of silicon
(PXL was 0.16 m²)

7-layer barrel geometry based on MAPS

r coverage: 23 – 400 mm

η coverage: $|\eta| \leq 1.22$
for tracks from 90% most luminous region

The ITS is composed of:
7 layers; 3 (IL), 2 (ML), 2(OL) –
192 staves; 48 (IL), 54 (ML), 90 (OL)

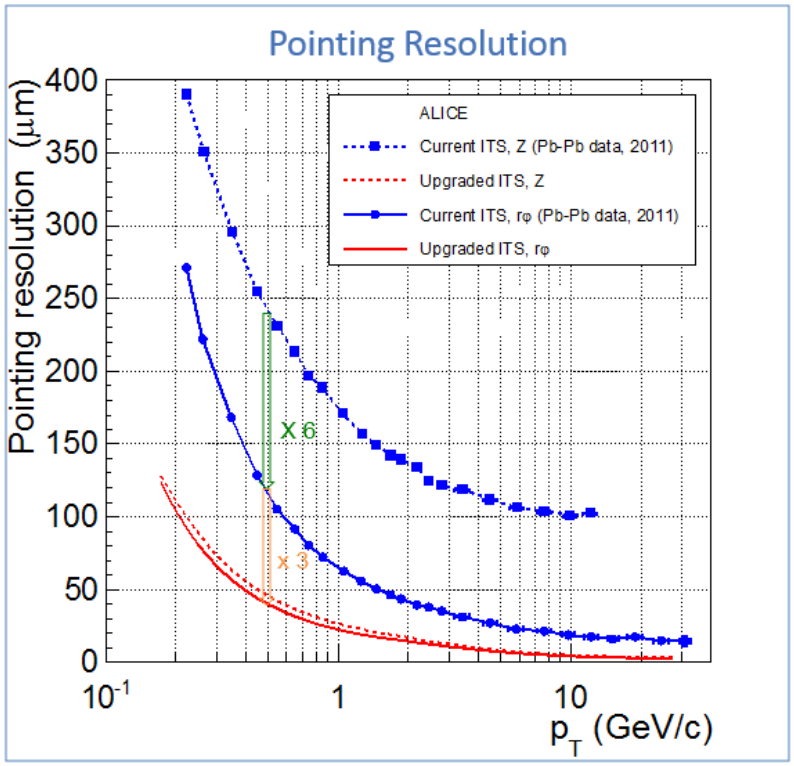
Material /layer : 0.3% X_0 (IB), 1% X_0 (OB)

ALICE ITS Upgrade TDR - http://iopscience.iop.org/0954-3899/41/8/087002/

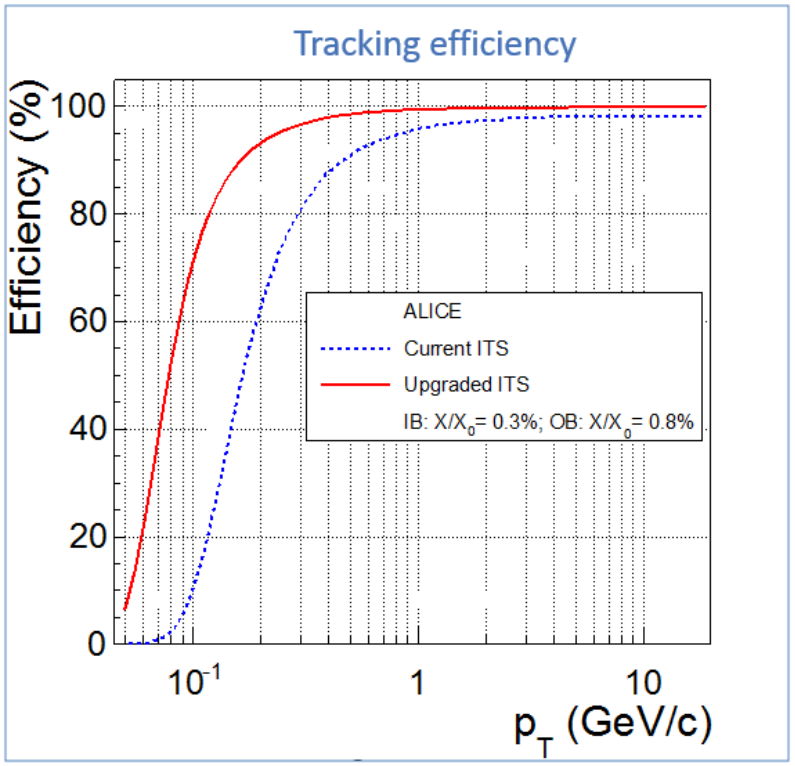
Upgraded ITS Performance

Performance of new ITS (MC simulations)

Impact parameter resolution



Tracking efficiency (ITS standalone)

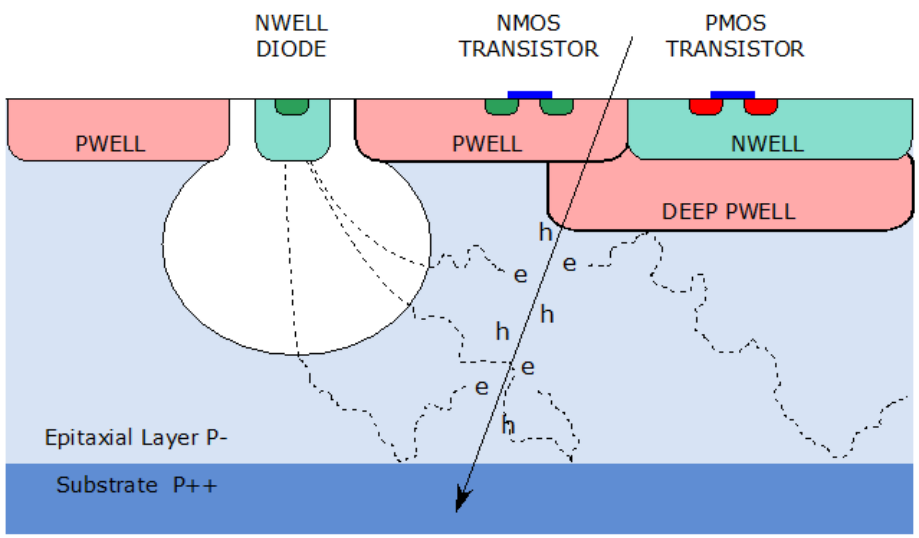


~40 μm at p_T = 500 MeV/c

All layers are MAPS sensors

ITS Pixel Chip – technology choice

CMOS Pixel Sensor using TowerJazz 0.18µm CMOS Imaging Process



Tower Jazz 0.18 µm CMOS

- feature size 180 nm
- metal layers 6

➔ Suited for high-density, low-power

- Gate oxide 3nm

➔ Circuit rad-tolerant

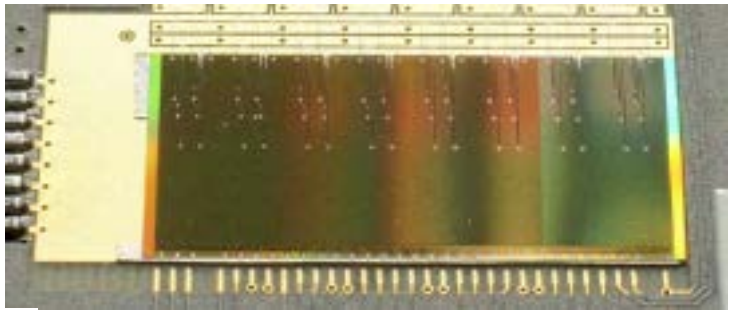
- High-resistivity (> 1kΩ cm) p-type epitaxial layer (20µm - 40µm thick) on p-type substrate
- Small n-well diode (2-3 µm diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate can be used to increase depletion zone around NWELL collection diode
- Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area

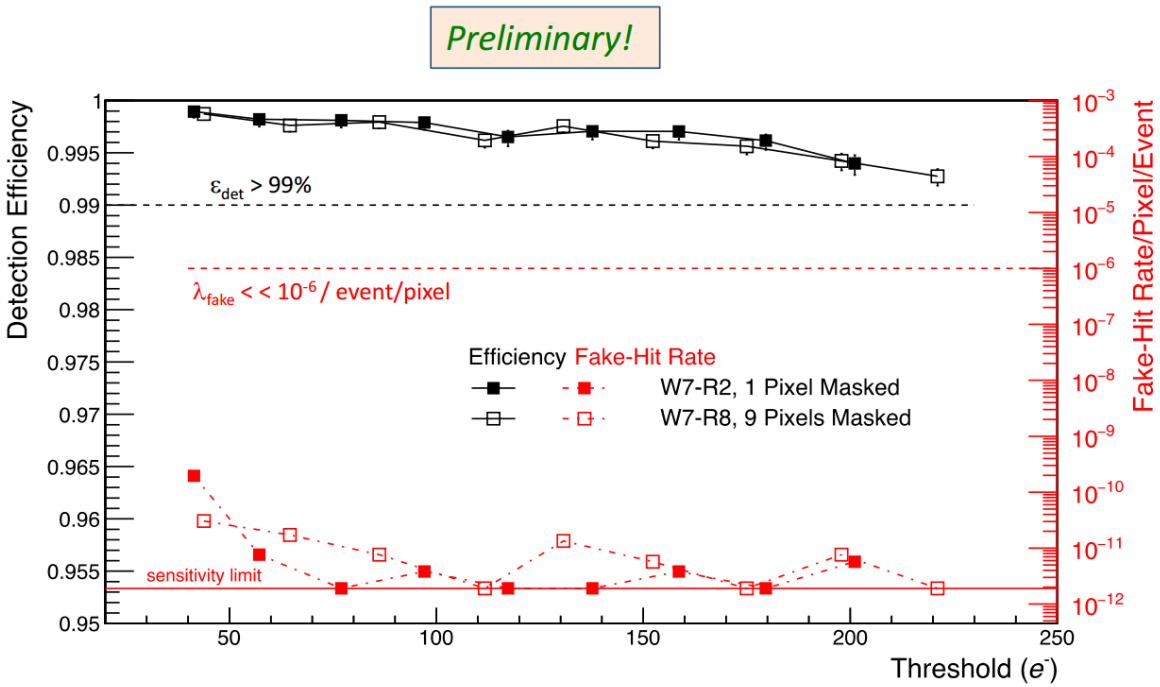
ALPIDE-4 Sensor Prototype Performance

ALPIDE-4 - Pre production prototype

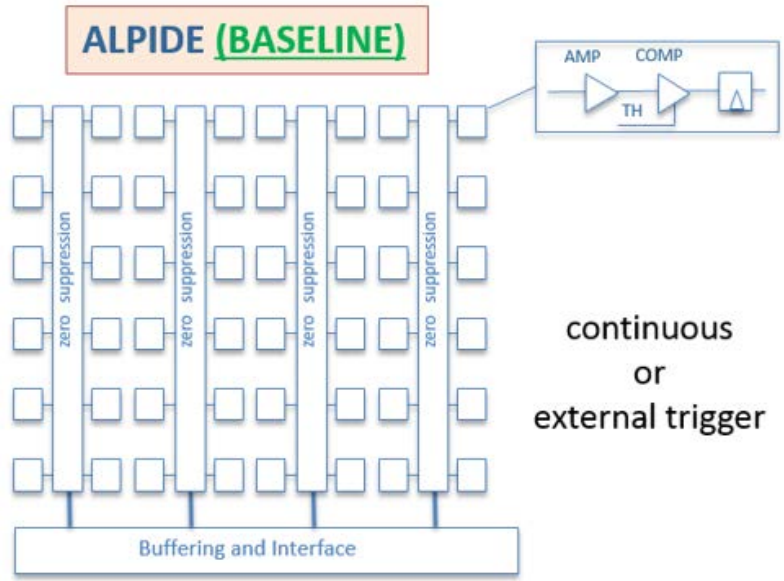
Main parameters

- Dimensions: 30 mm x 15 mm
- Pixel Matrix: 1024 cols x 512 rows
- Pixel pitch: 29 μm x 27 μm





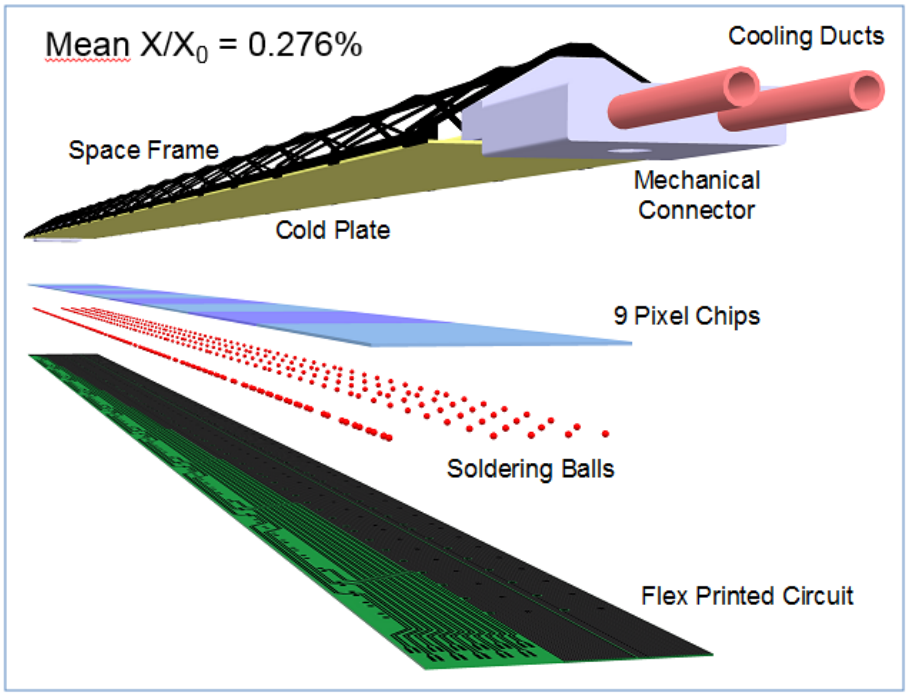
- Excellent efficiency and fake hit rate.
- Further testing is underway.

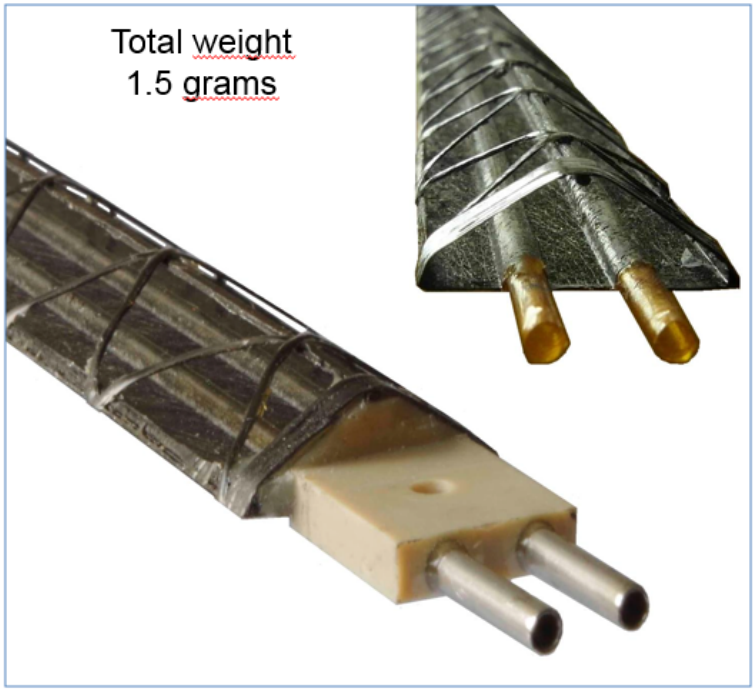


Discriminators are now in pixel. All pixels digitize at the same time when triggered and are read out via priority encoder.

ITS Inner Layers

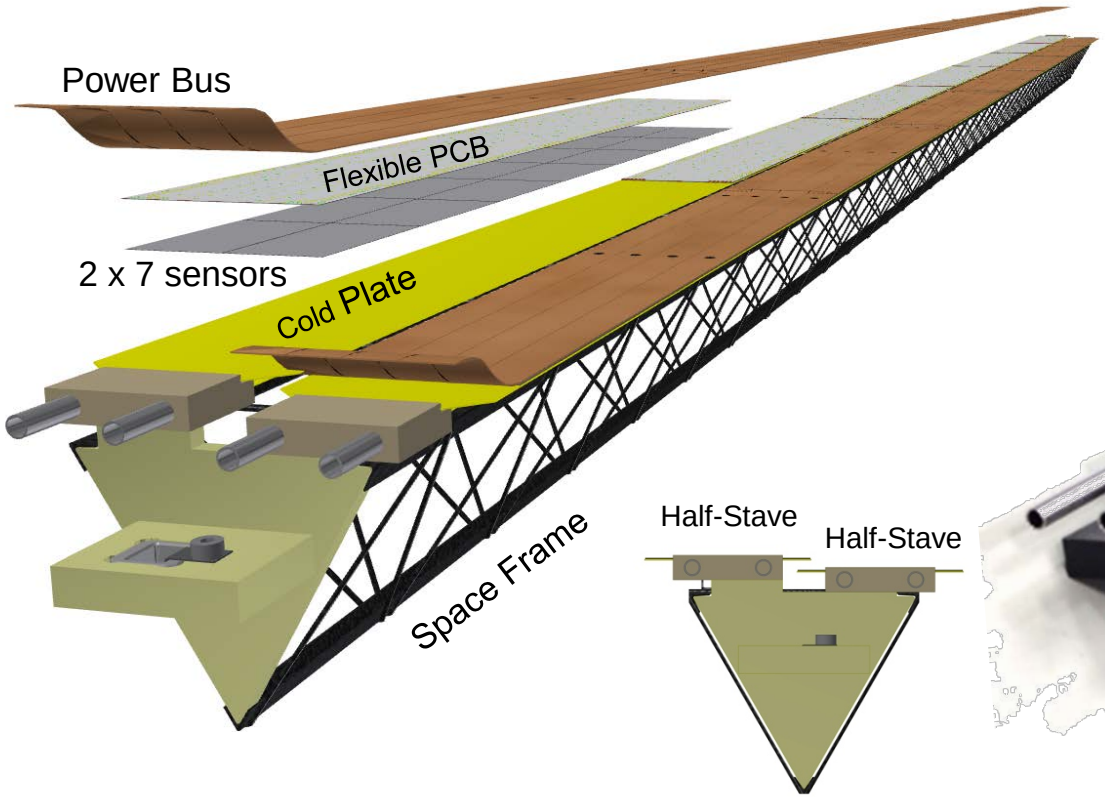
New ITS Layout - Inner Barrel Stave





<Radius> (mm): 23,31,39	Length in z (mm): 290
Nr. of staves: 12, 16, 20	Nr. of chips/stave: 9
Nr. of chips/layer: 108, 144, 180	Material thickness: ~ 0.3% X_0
Power density: < 100 mW/cm^2	Throughput (@100kHz): < 80 Mb/s × cm^{-2}

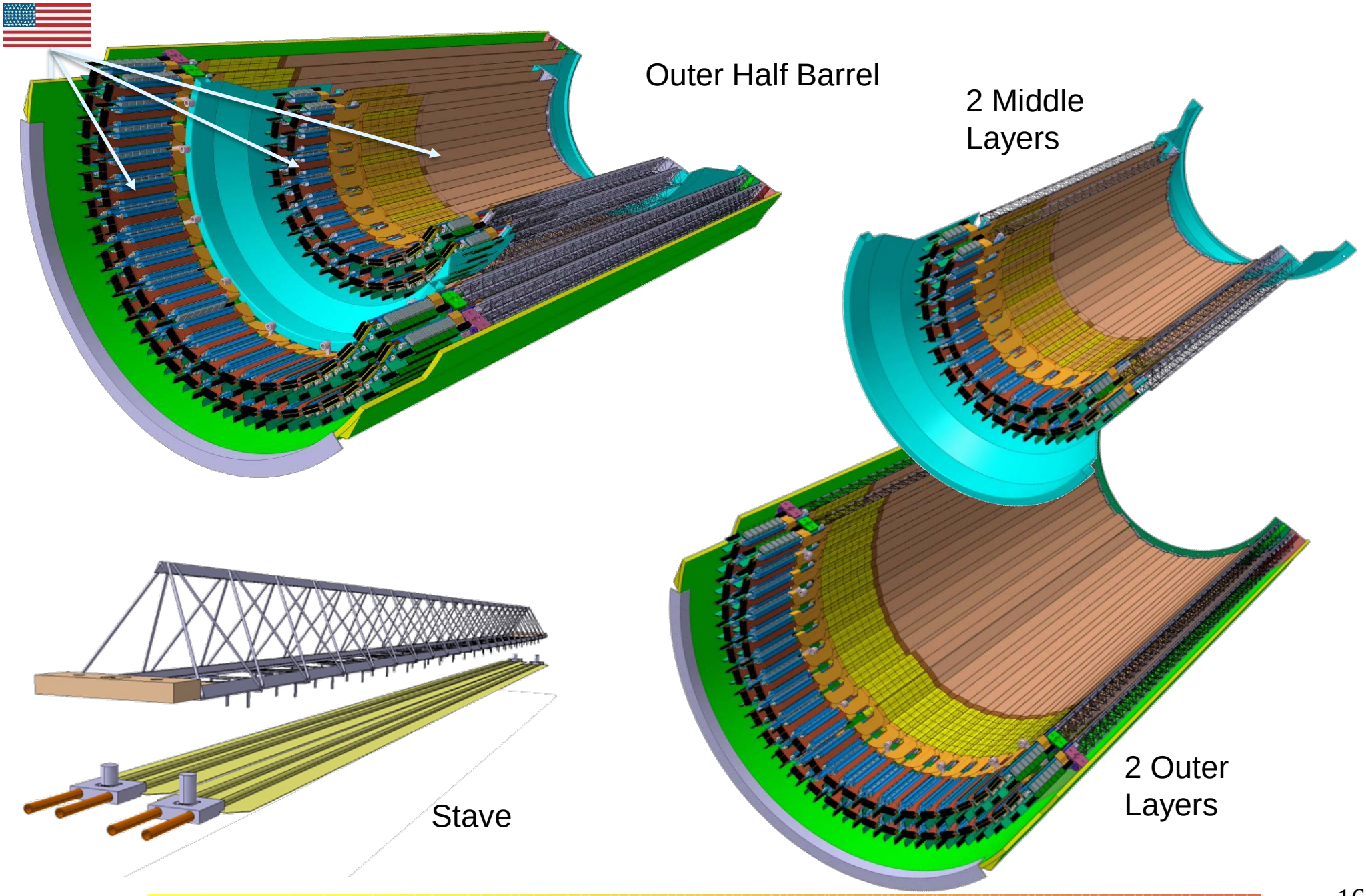
ITS Outer Barrel



Outer Barrel (OB)

<radius> (mm): 194, 247, 353, 405	Length (mm): 900 (ML), 1500 (OL)
Nr. staves: 24, 30, 42, 48	Nr. modules/stave: 4 (ML), 7 (OL)
Nr. Chips/layer: 6048 (ML), 17740(OL)	Material thickness: ~ 1% X_0
Power density < 100 mW / cm^2	Throughput (@100kHz): < 3Mb/s × cm^{-2}

ITS Outer Detector Barrel



ALICE-US Scope

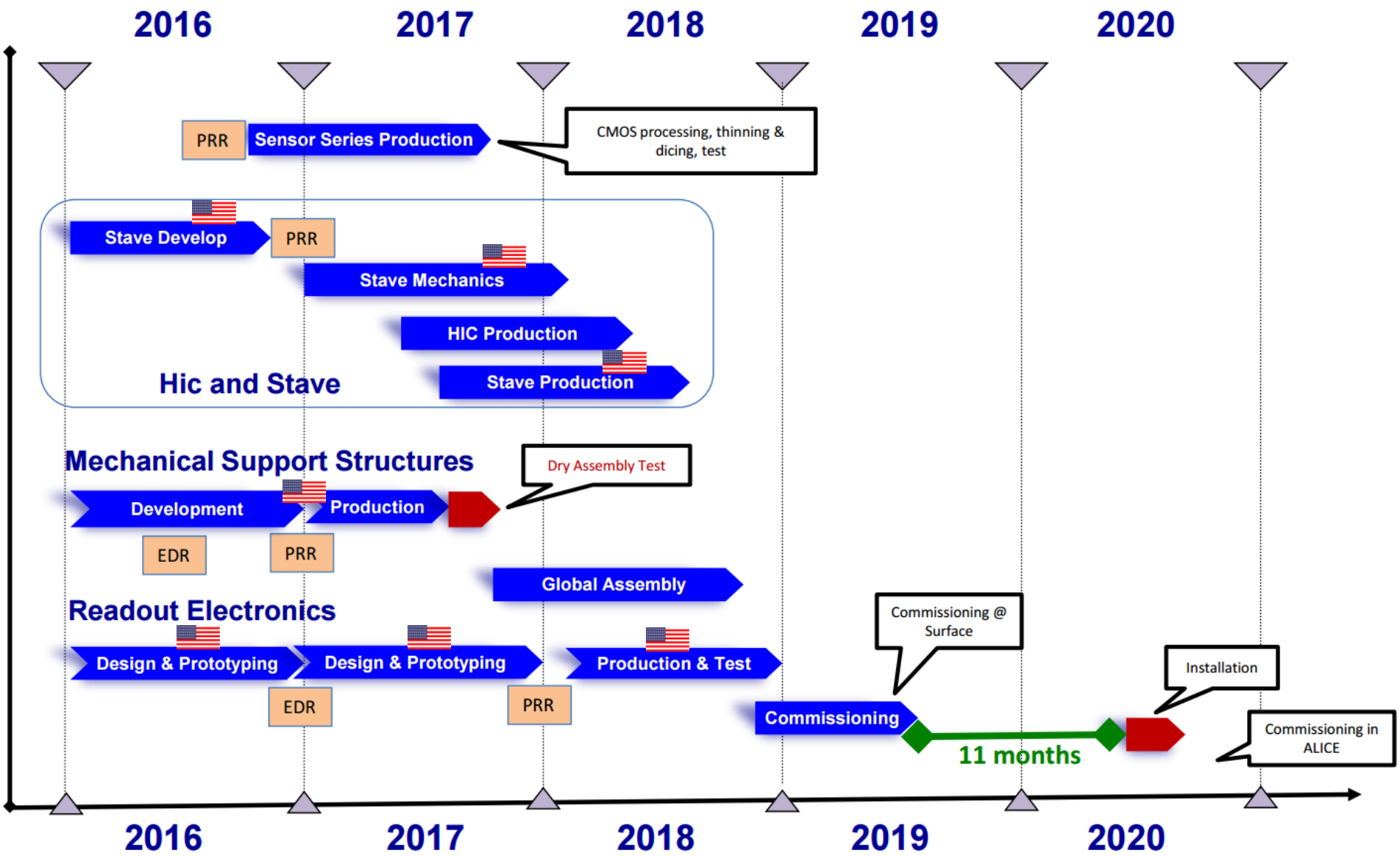
LBNL RNC group is the project leader for the ALICE-USA ITS upgrade construction project.

- Assembly and testing of Middle layer staves (layers 3,4) from components (modules, cold plates, space frames) fabricated by other institutions.
- RDO system design (collaboration) and fabrication of RDO for the middle layers (Univ. of Texas, Austin).
- Design of the powering system for all outer layers (3-6) including power bus, power boards and control system.
- Sensor and component testing at the BASE facility for SEU and SEL (See Mike Johnson's talk). **Synergy with the NSD 88" cyclotron.**
- The large outer layers carbon fiber support cylinder and services cone structures. **Synergy with LBNL engineering division.**

We also have strong support and synergy with UC Berkeley and students are a significant contributor to the development and construction of the ITS upgrade.

We look forward to delivering the detector hardware and following through with the extraction of the physics as was done with the HFT.

ITS Current Schedule



Future Applications

- New experiments and upgrades to existing experiments that require high precision tracking and vertex resolution are a standard feature at collider accelerators.
- RNC is a full service laboratory group with experience with MAPS based sensors, carbon fiber support structures, readout systems and management and integration of large complex systems.
- Some new experiments have strong interest, particularly sPHENIX at RHIC.
- RNC is currently involved in EIC development efforts and will continue to pursue our strong interest in EIC instrumentation and physics.
- RNC will continue to lead the field in the development of state of the art instrumentation projects for physics.

- backup

Readout Topologies

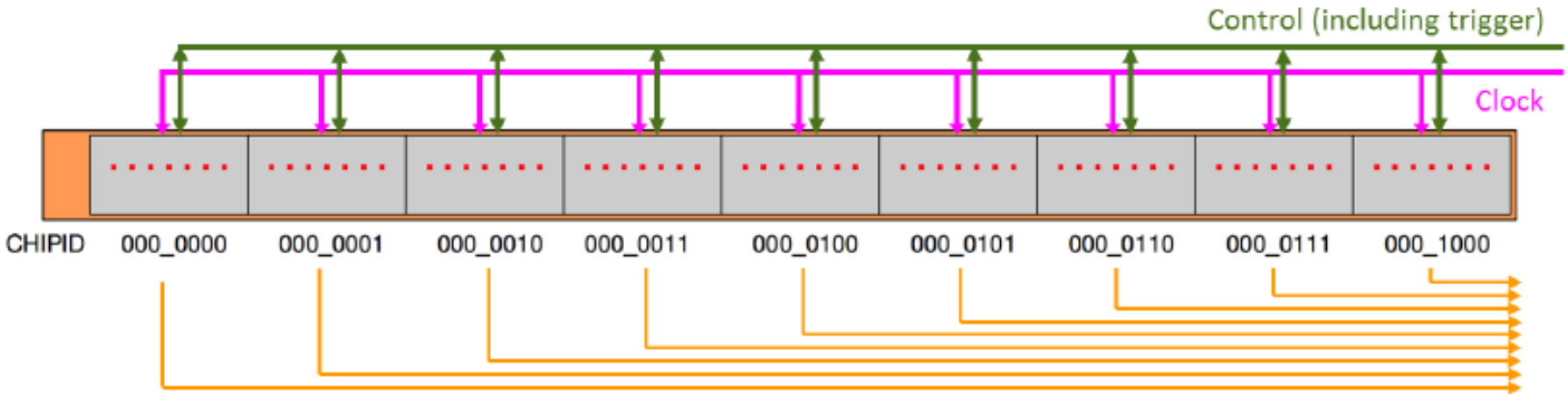


Figure 1 – inner Layers stave sensors and connections schematic.

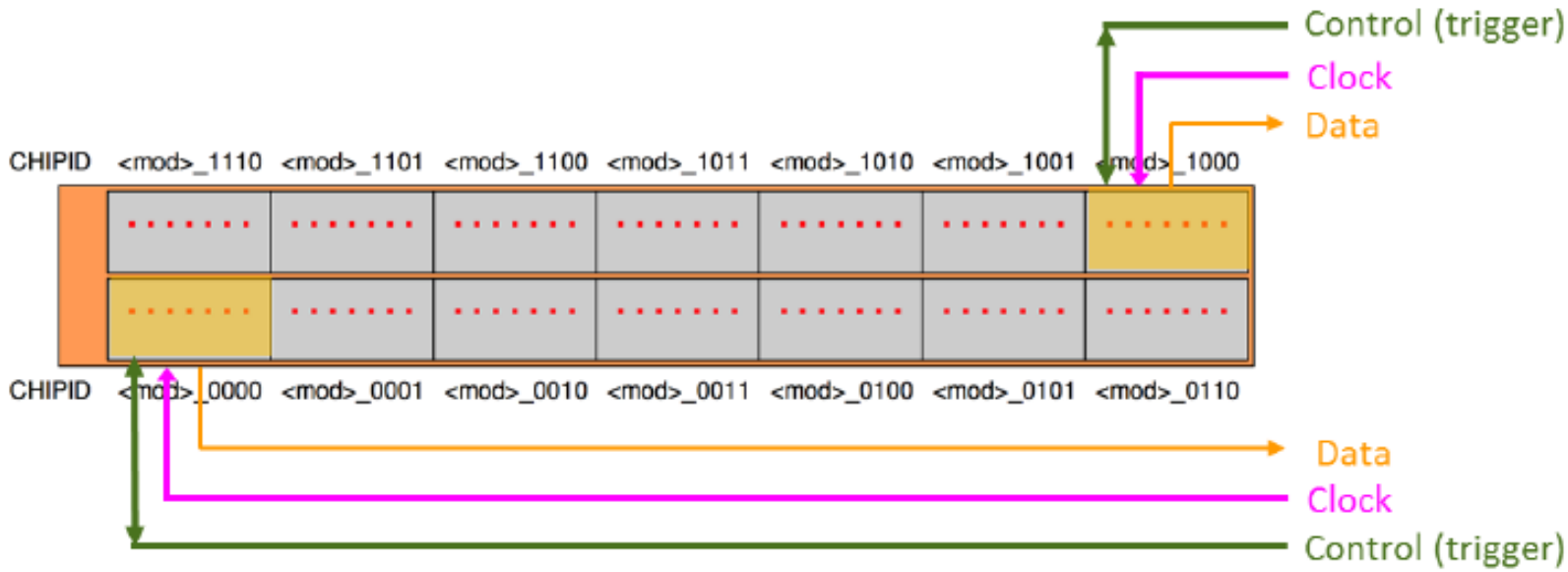
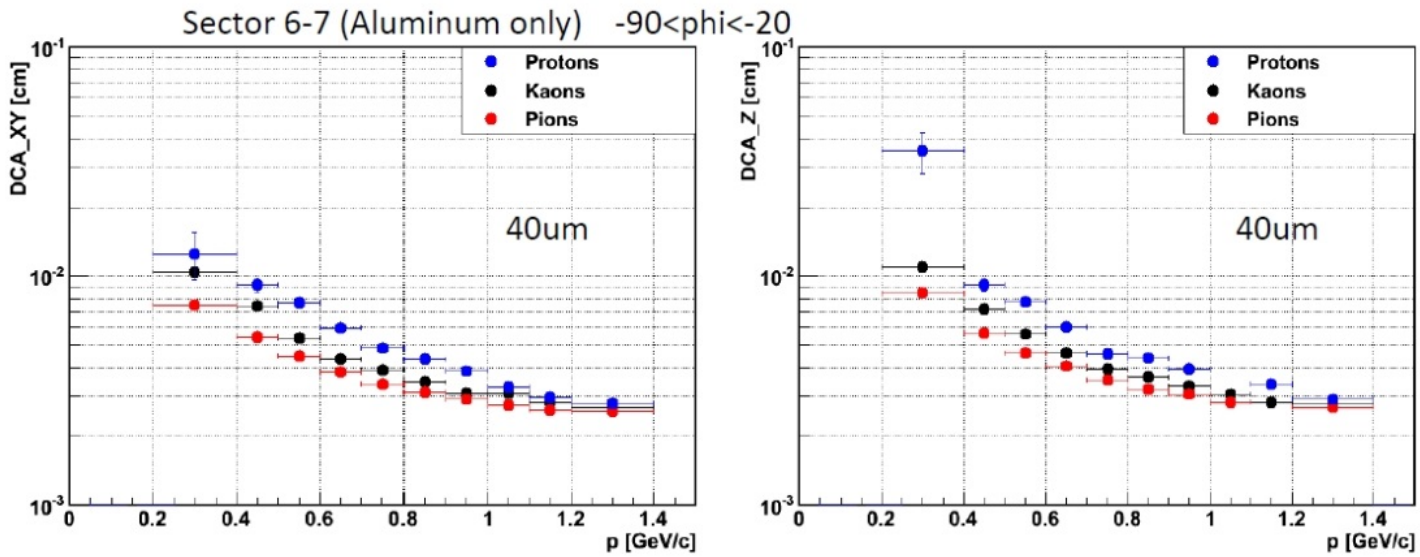


Figure 2 – Module layout with links.

Preliminary DCA Pointing resolution (Au+Au @ 200GeV)

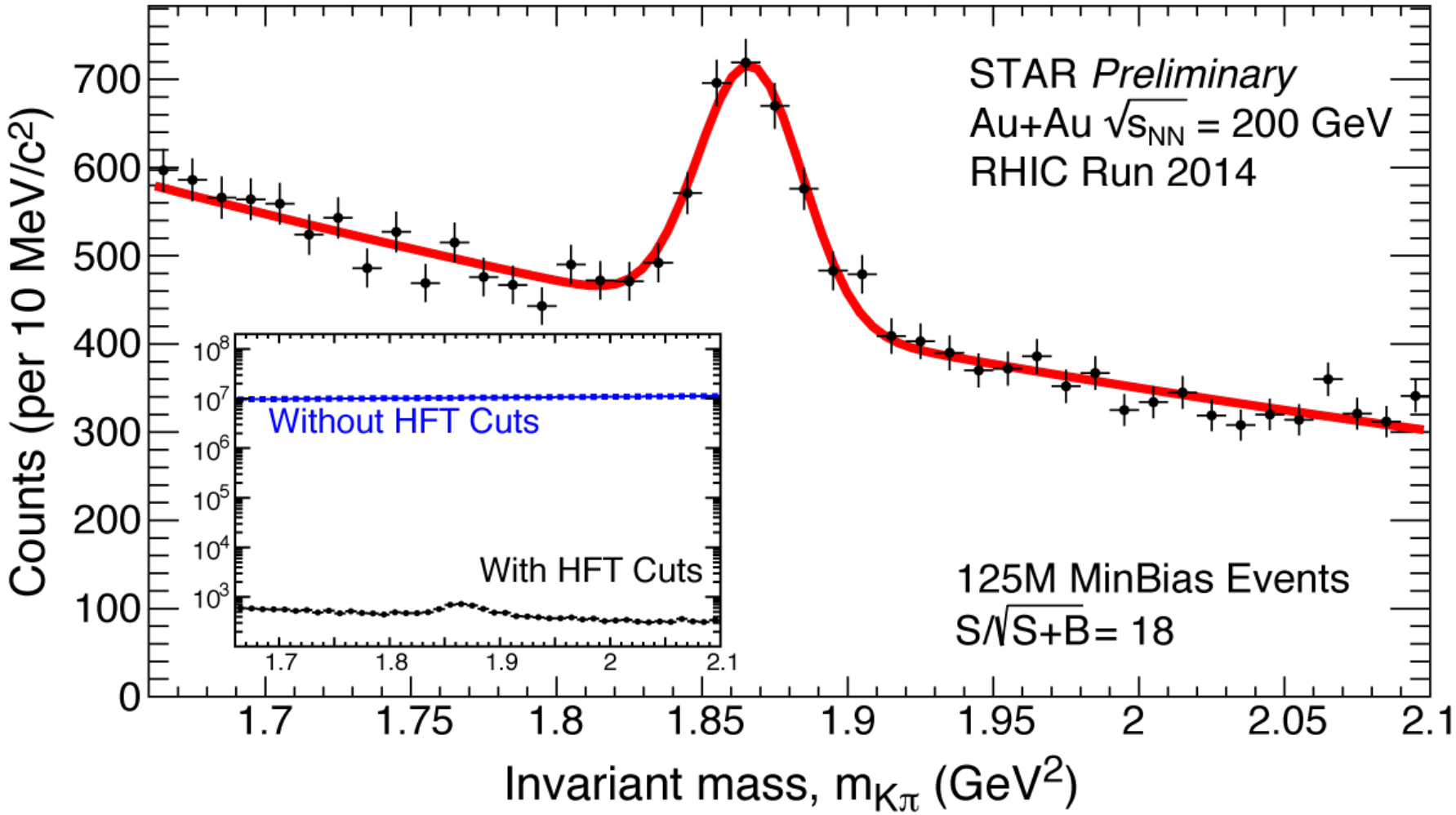
40 µm DCA with Al conductor cables on inner ladders for 750 MeV/c Kaons



TPC + IST + PXL

- Meets tracking requirements for HFT
- Operationally good –
- Early problems with LU induced damage.
- Problem solved operationally after first 2 weeks of running.
- 2nd run gave only 4 sensors damaged.

Overall experience

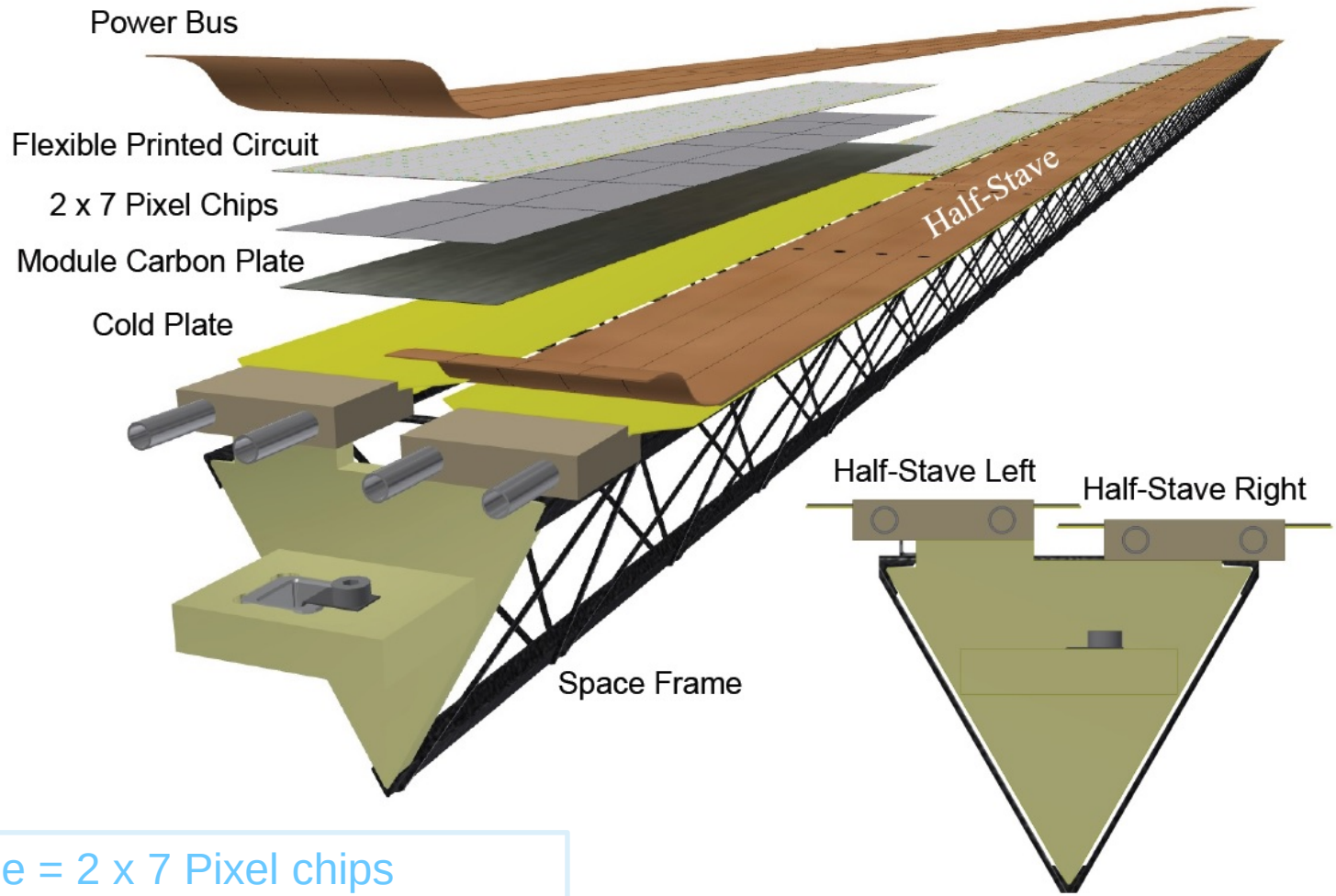


Very Good

Layer	Radius	TID	NIEL	HI Flux
	[mm]	[kRad]	[1 MeV n_{eq} cm^{-2}]	[kHz cm^{-2}]
0	23	646	9.2×10^{12}	
1	32	380	6.0×10^{12}	
2	39	216	3.8×10^{12}	
3	196	15	5.4×10^{11}	
4	245	10	5.0×10^{11}	
5	344	8	4.8×10^{11}	
6	393	6	4.6×10^{11}	15?
Crate				<1?

Table 4 – Expected radiation levels (integrated Pb-Pb luminosity of 10 nb^{-1}).

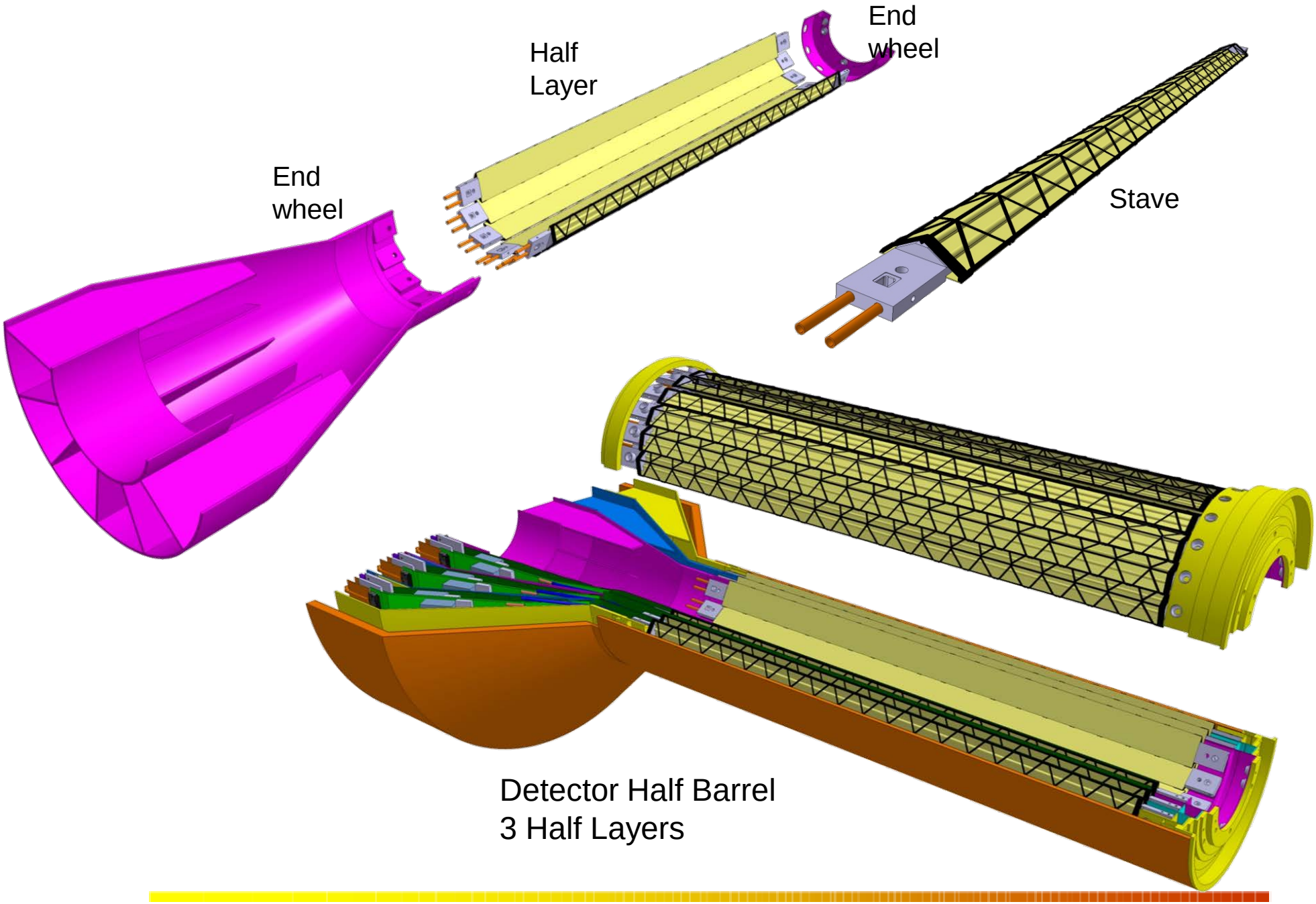
Middle and Outer Layers



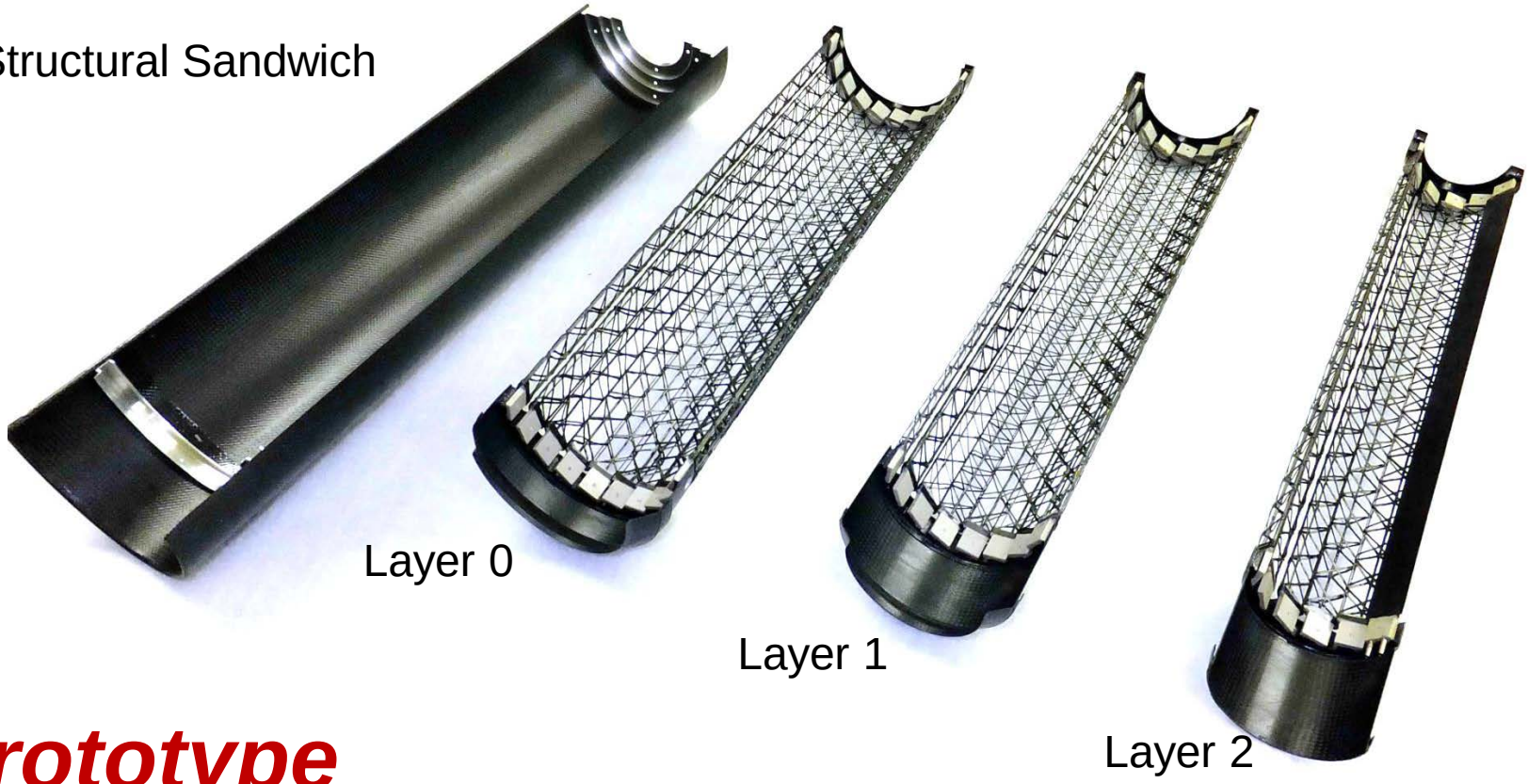
Module = 2 x 7 Pixel chips
Stave = 2 Half-Staves
Outer Layers are 7 modules long
Middle Layers are 4 modules long

Pixel sensors are ~15 mm x ~30 mm
Modules are ~3 cm x ~21cm

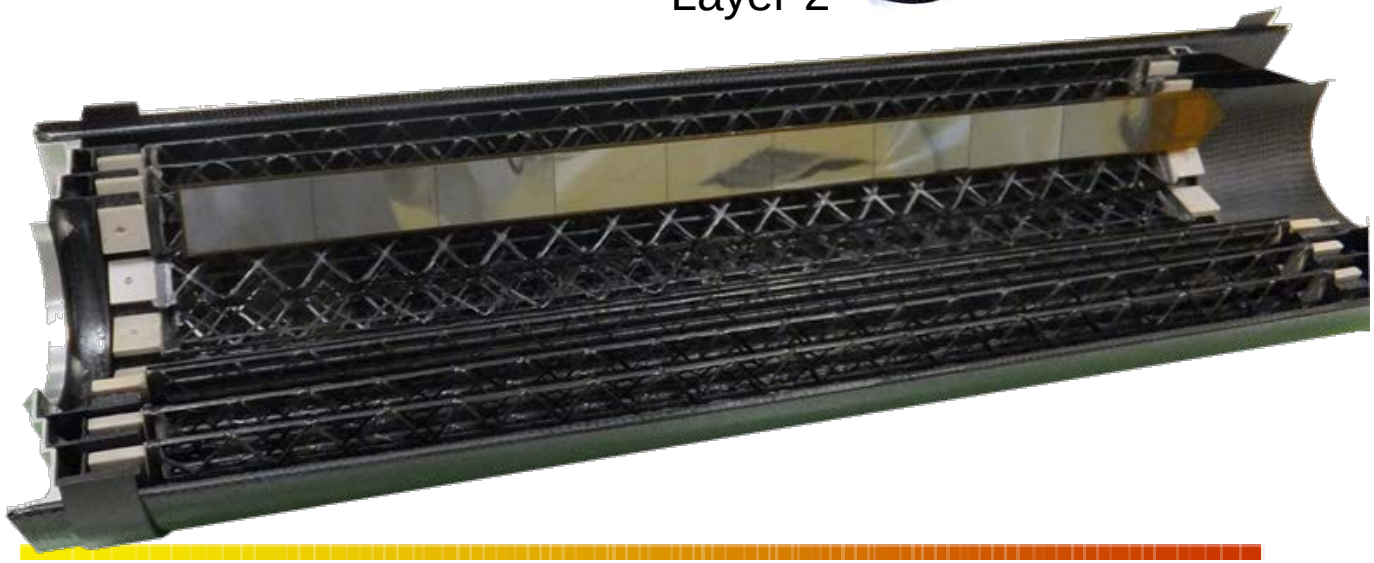
Inner Barrel



Inner Barrel – full-scale prototype



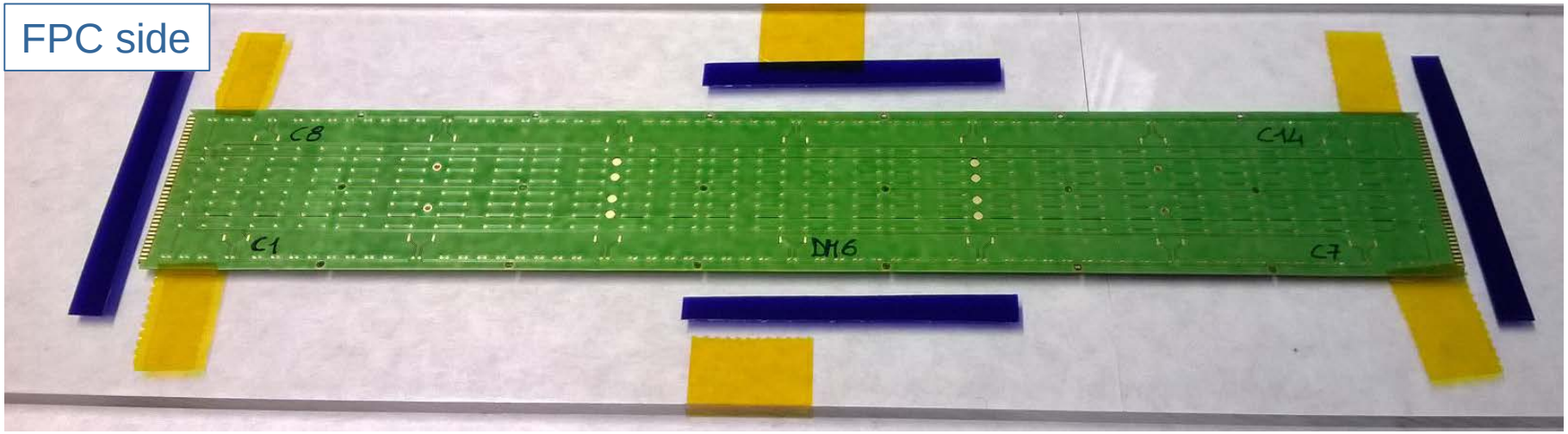
Prototype



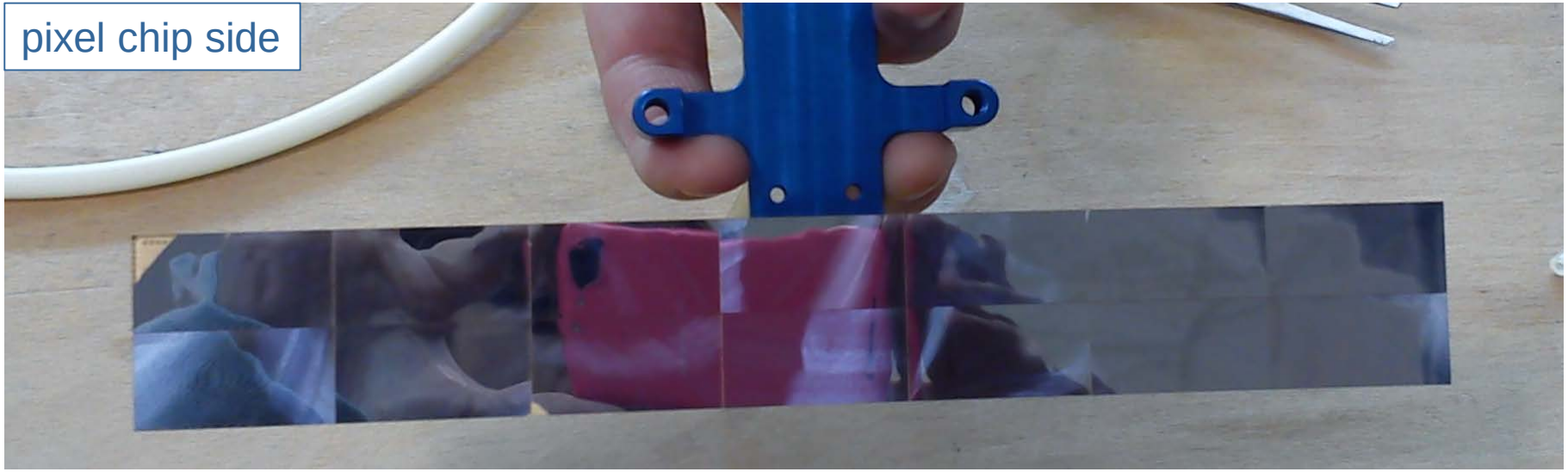
ITS Outer Barrel

HIC: Interconnection of pixel chip on flexible printed circuit (FPC)

FPC side

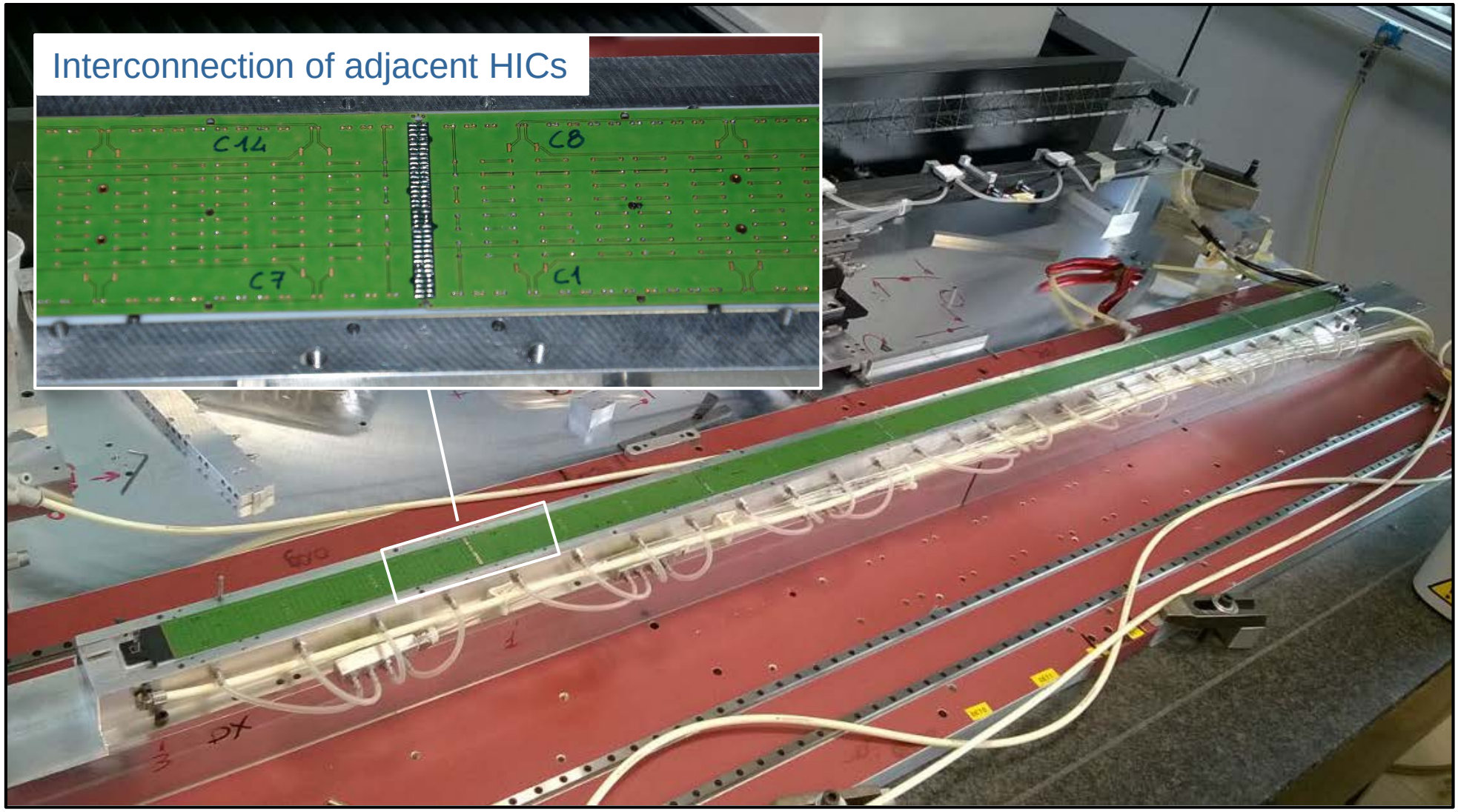


pixel chip side

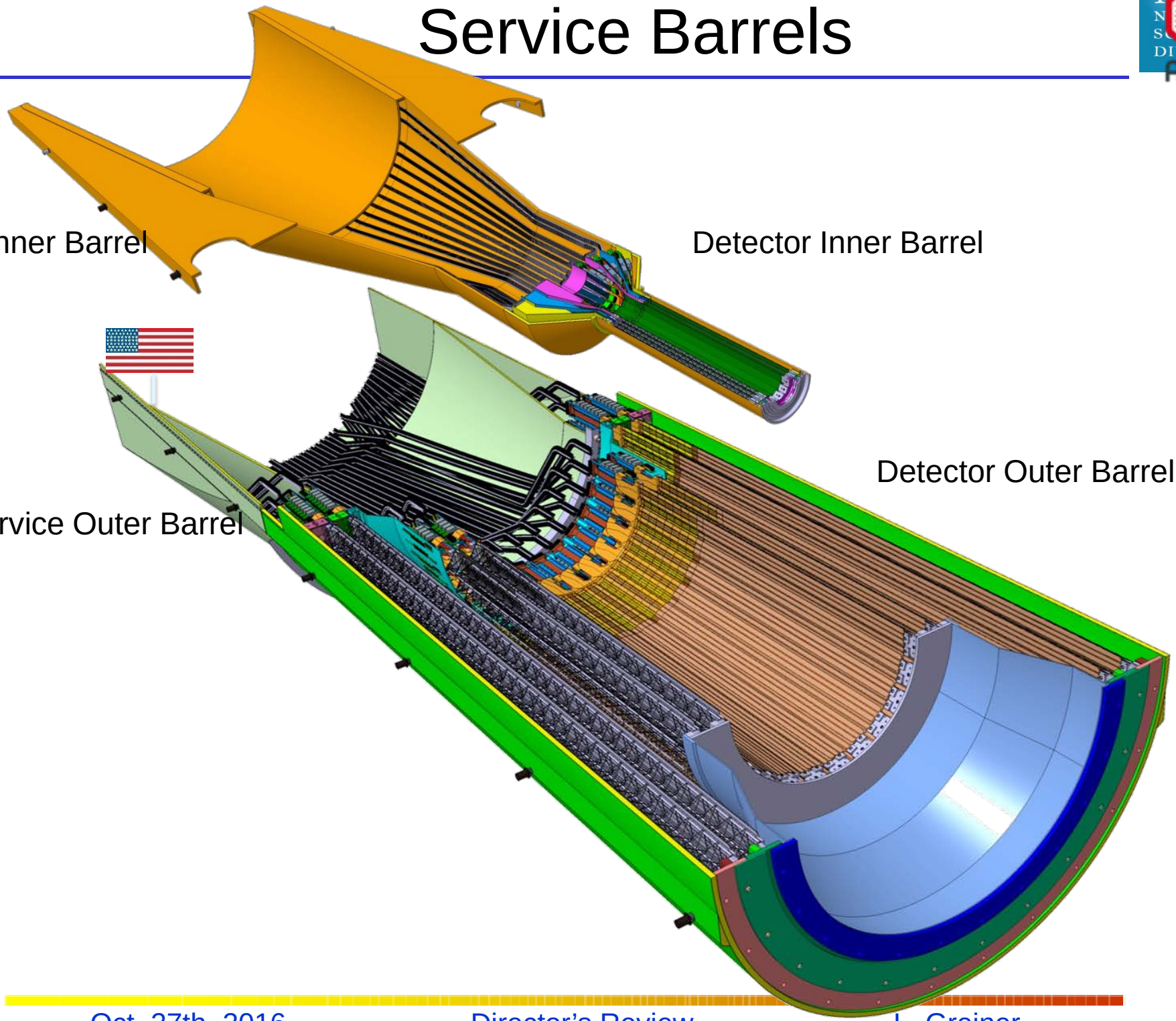


ITS Outer Barrel

Half-stave equipped with dummy HICs (dummy silicon chips)



Service Barrels



ALPIDE Pixel Logic

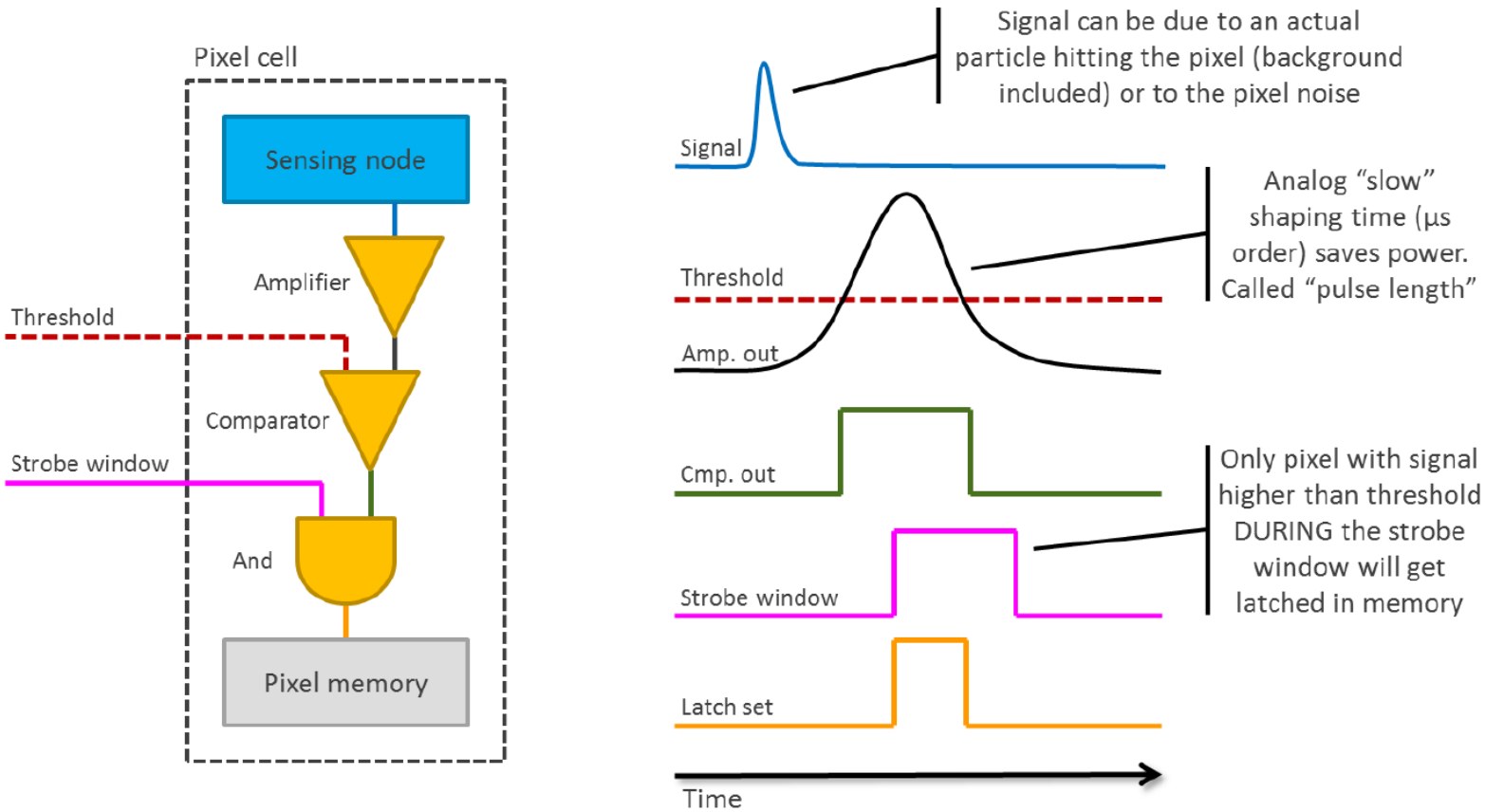


Figure 14 – Pixel logic schematic and timing diagram.

Readout Structure

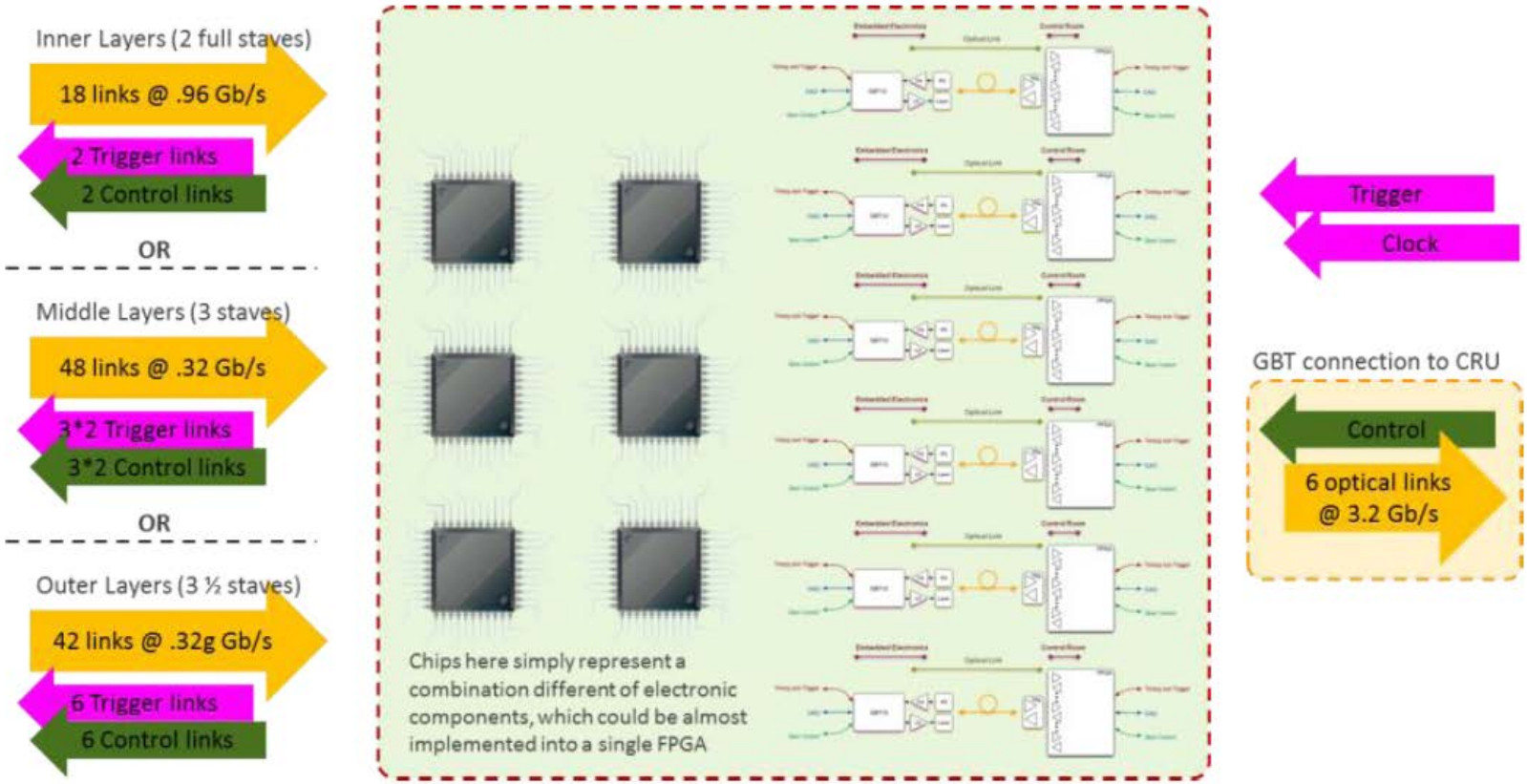


Figure 9 – RU based on GBT links connecting to the CRU (data load is payload only).

Data Rate Capabilities

Pb-Pb => first layer

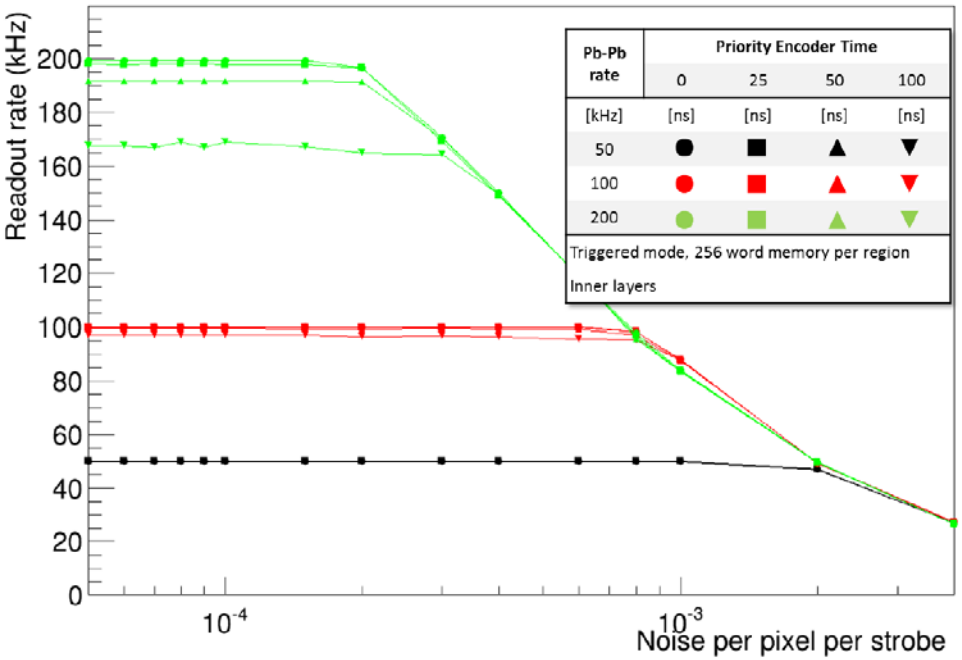


Figure 25 – Pb-Pb collisions in the 1st layer from 50 kHz to 200 kHz average rate in trigger mode. The readout rate should match the average trigger rate, but it fails whenever the noise rate too high and/or the time required to read out the matrix (Priority Encoder time) is too long.

Pb-Pb => fourth layer

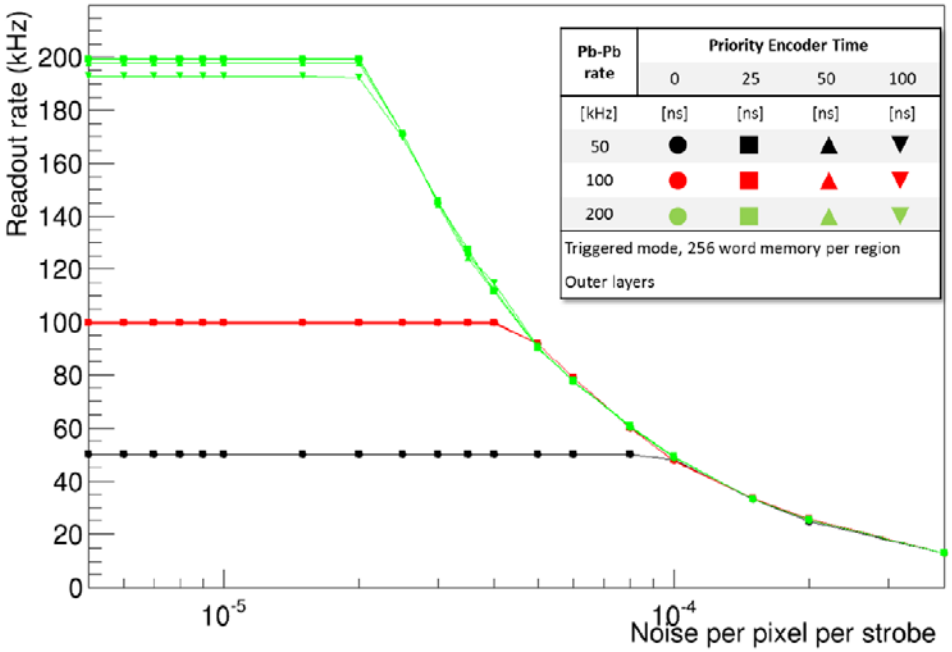
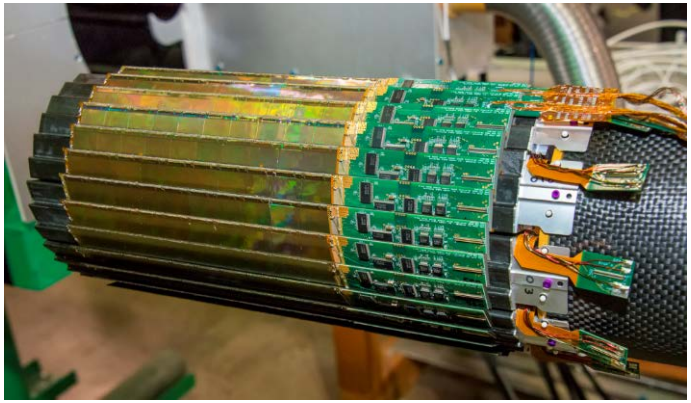
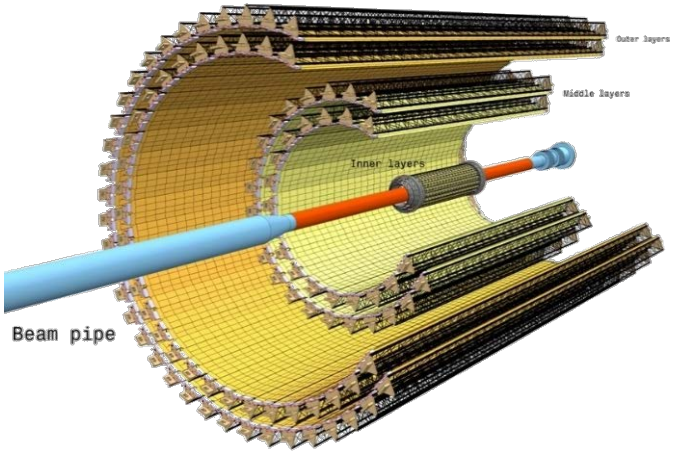


Figure 26 – Pb-Pb collisions in the 4th layer from 50 kHz to 200 kHz average rate in triggered mode. The readout rate should match the average trigger rate, but it fails whenever the noise rate is too high and/or the time required to read out the matrix (Priority Encoder time) is too long.

Silicon Vertex Detector Development at RNC based on Monolithic Active Pixel Sensors



- STAR PXL Detector
- First vertex detector at a collider experiment based on ***Monolithic Active Pixel Sensor*** technology
- Received CD2-3 in 2011.
- Project completed in 2014 and met all CD-4 parameters.
- Completed on time and under budget.



- ALICE ITS Upgrade Detector
- Next generation MAPS based vertex detector
- Received CD2-3 equivalent in 2015.
- LBNL responsible for middle layers, Carbon Fiber support structures, RDO.
- Installation scheduled for end of LS2 (2019-2020).

Future: sPHENIX ?

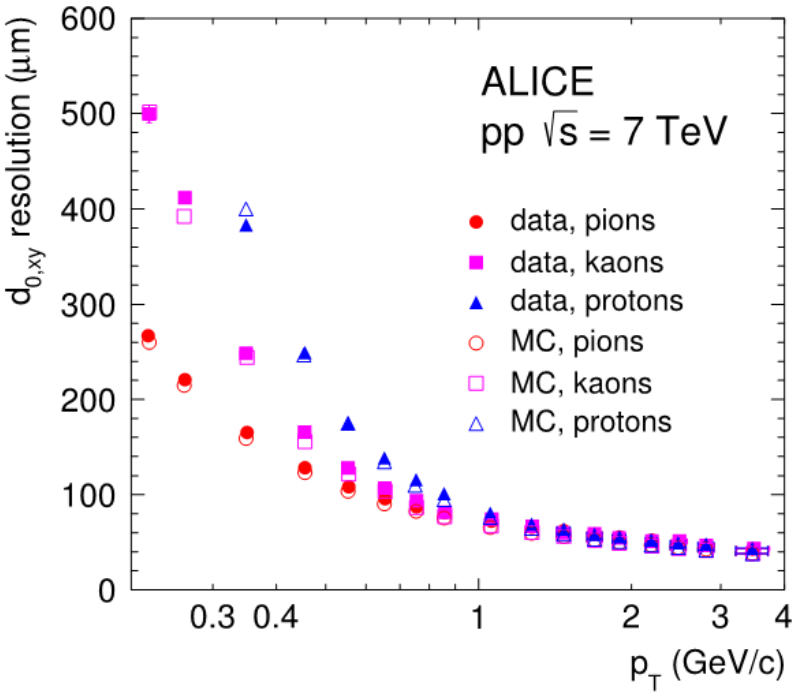
- ALICE MAPS sensor technology
- Next generation MAPS based vertex detector for RHIC
- Proposal in progress.

Existing ITS Performance

ALICE ITS Upgrade – Impact parameter resolution

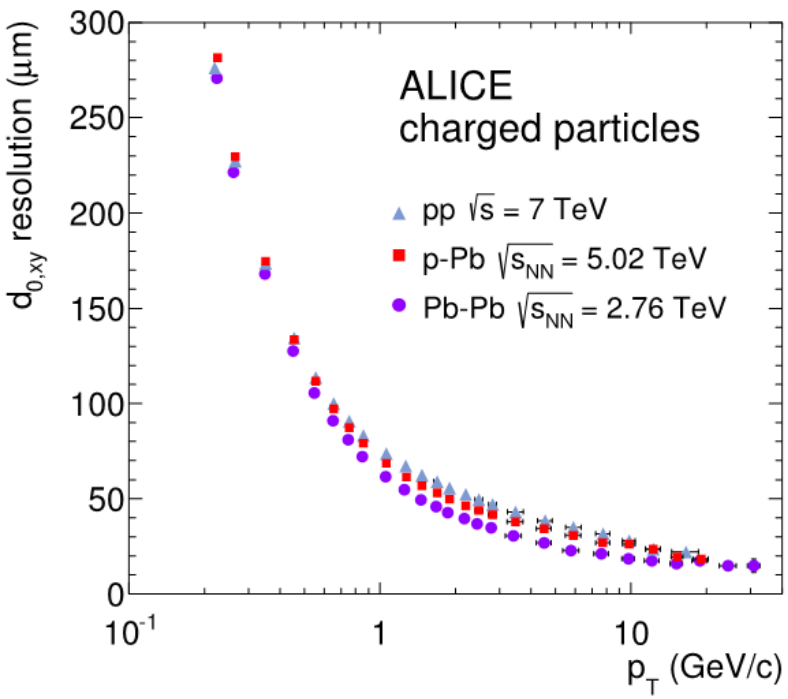
Hybrid pixels, silicon drift, silicon strips – X/X_0 ~1% inner layers

Very good MC description



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

Very weak dependence on the colliding system



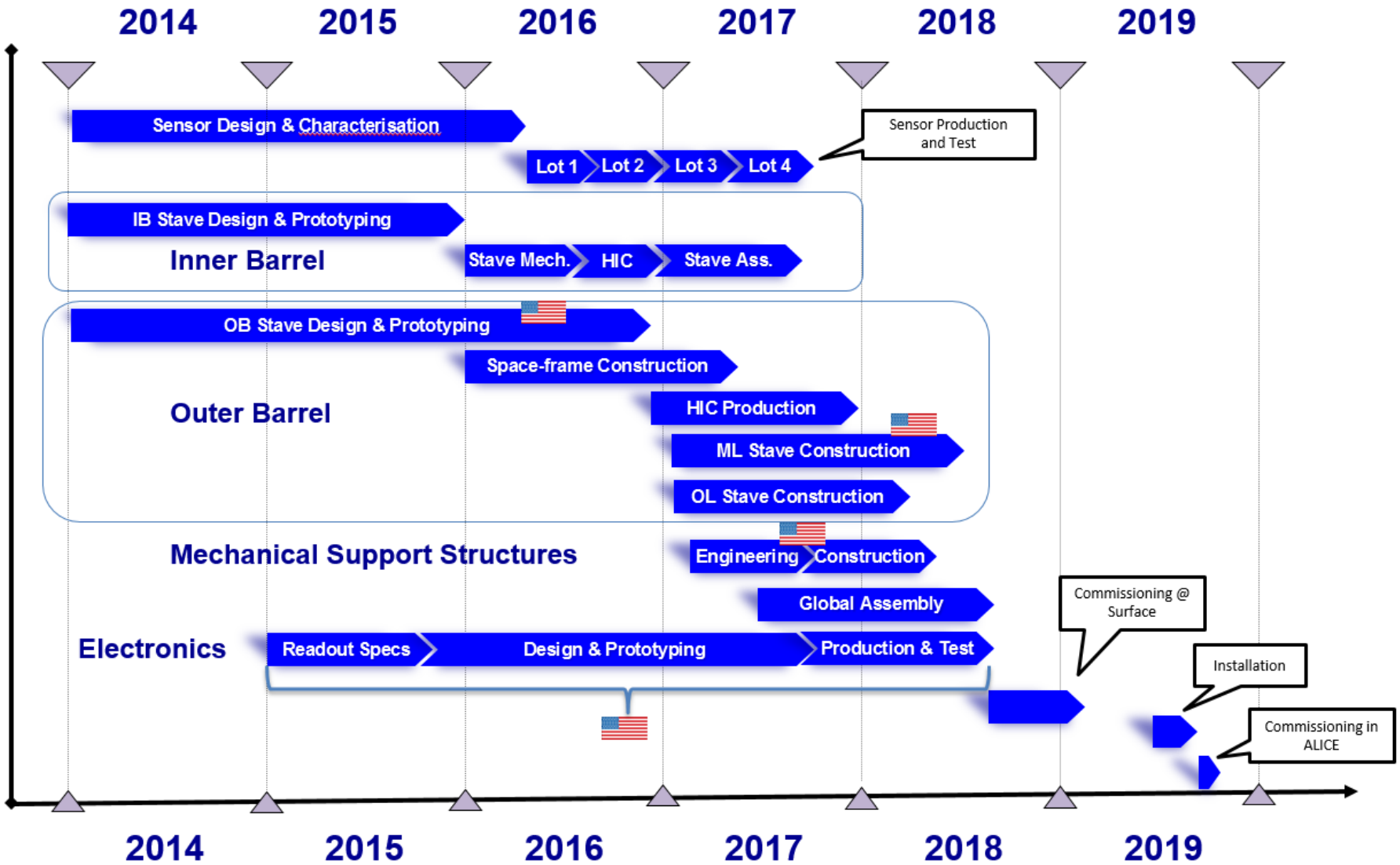
ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

120 μm at p_T = 500 MeV/c

5

ITS Current Schedule

Planning (simplified global view)



L. Musa