

Diagnostics WG meeting on Cryoelectronics

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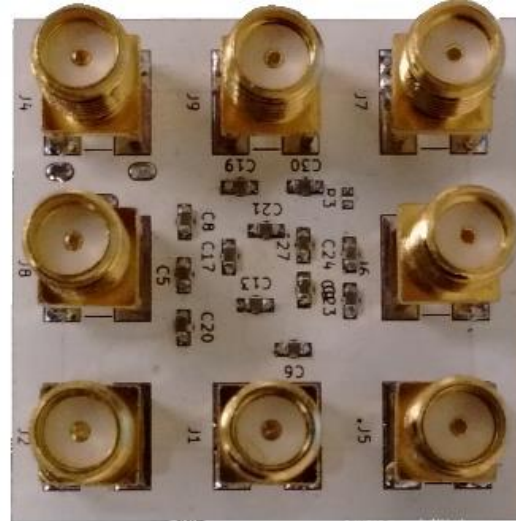
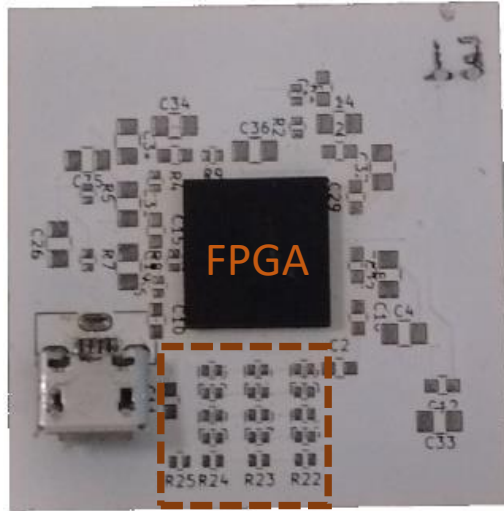
Lawrence Berkeley National Laboratory

2021

FPGA BOARD AND HYBRID FLASH FOLDING ADC

Cryo FPGA Implementation version 1

JTAG

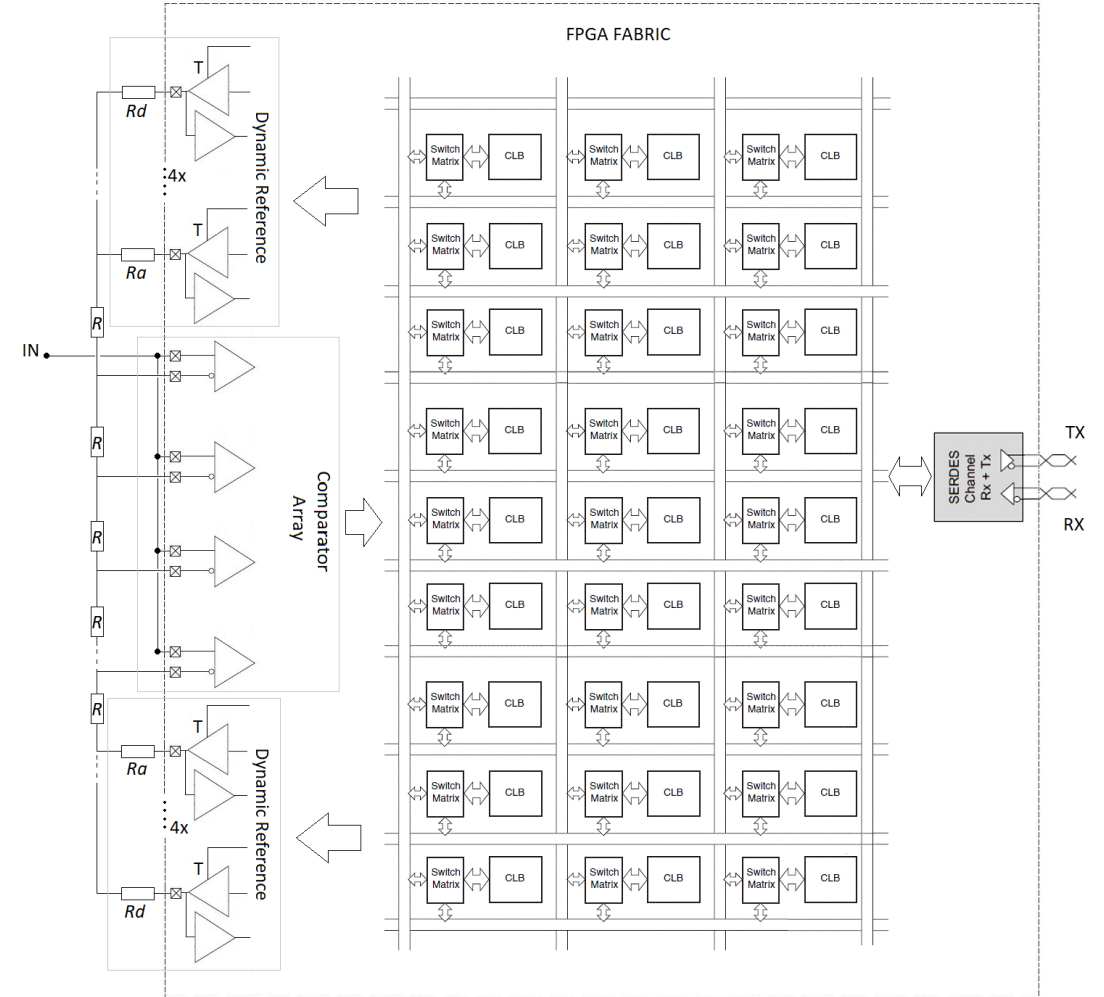


Resistor Array:

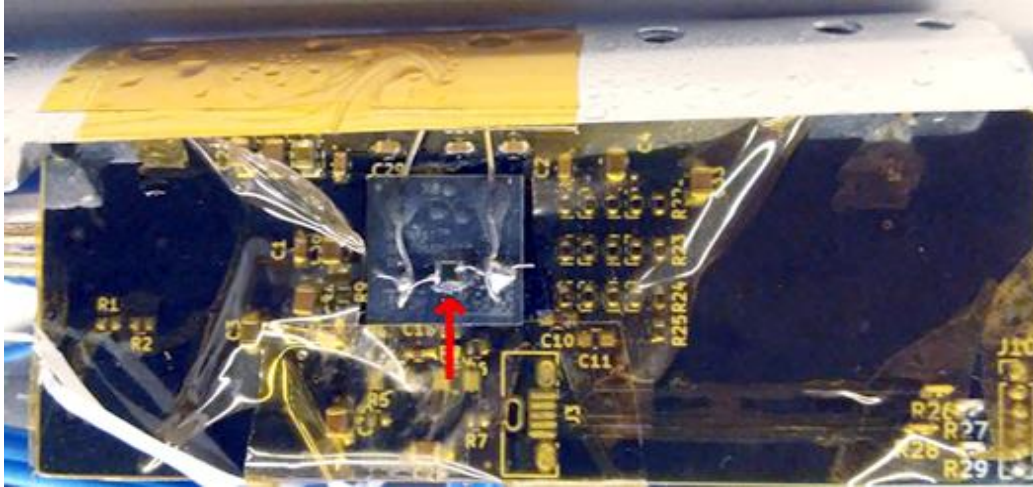
- Connected to FPGA differential buffers
- Uses FPGA bank reference

SMA interface:

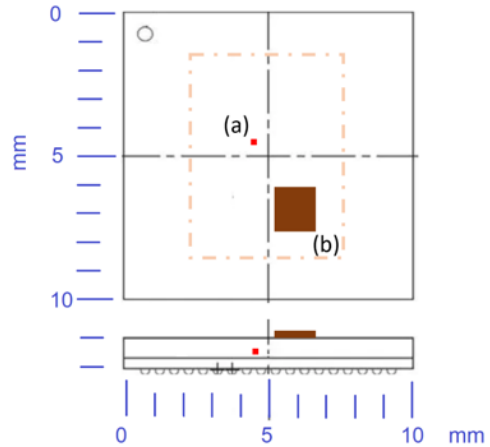
- Power (Core and I/O)
- Analog In
- Digital In
- Digital Out



TEST STAND AND TEMPERATURE MONITORING

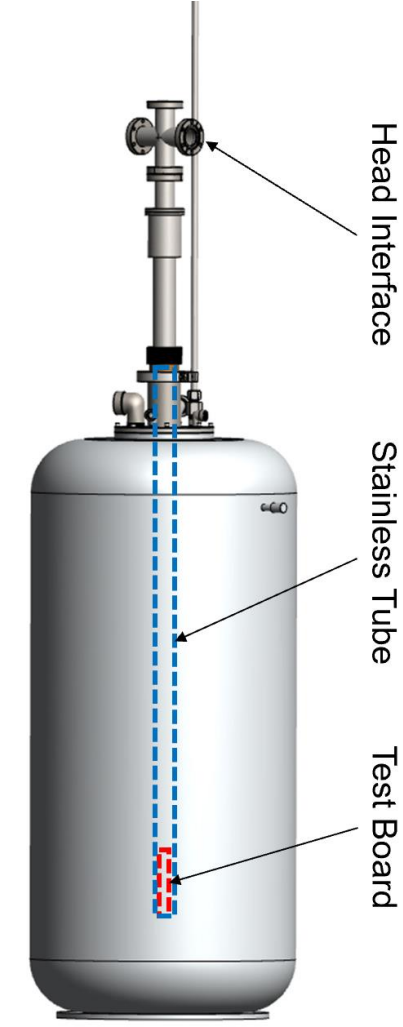


The RuO thermometer indicated by the red arrow glued on top of the FPGA (shown with an arrow)



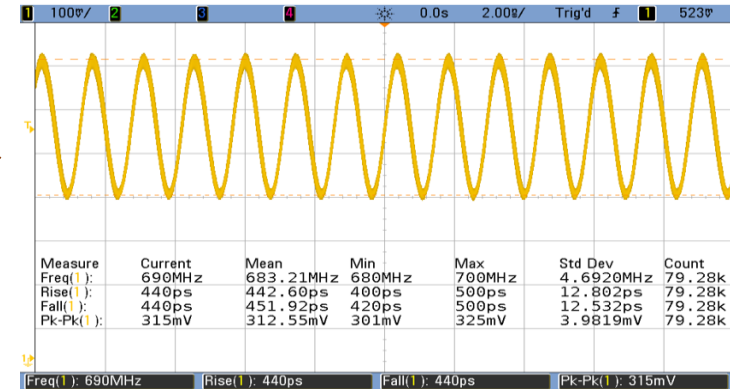
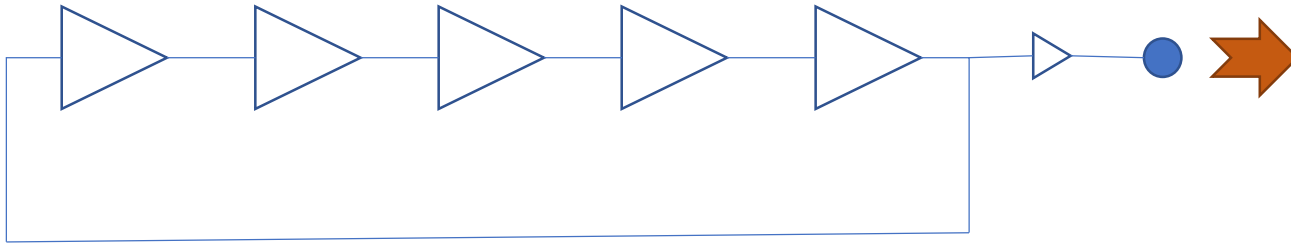
(a) Internal Thermometer

(b) RuO Thermometer

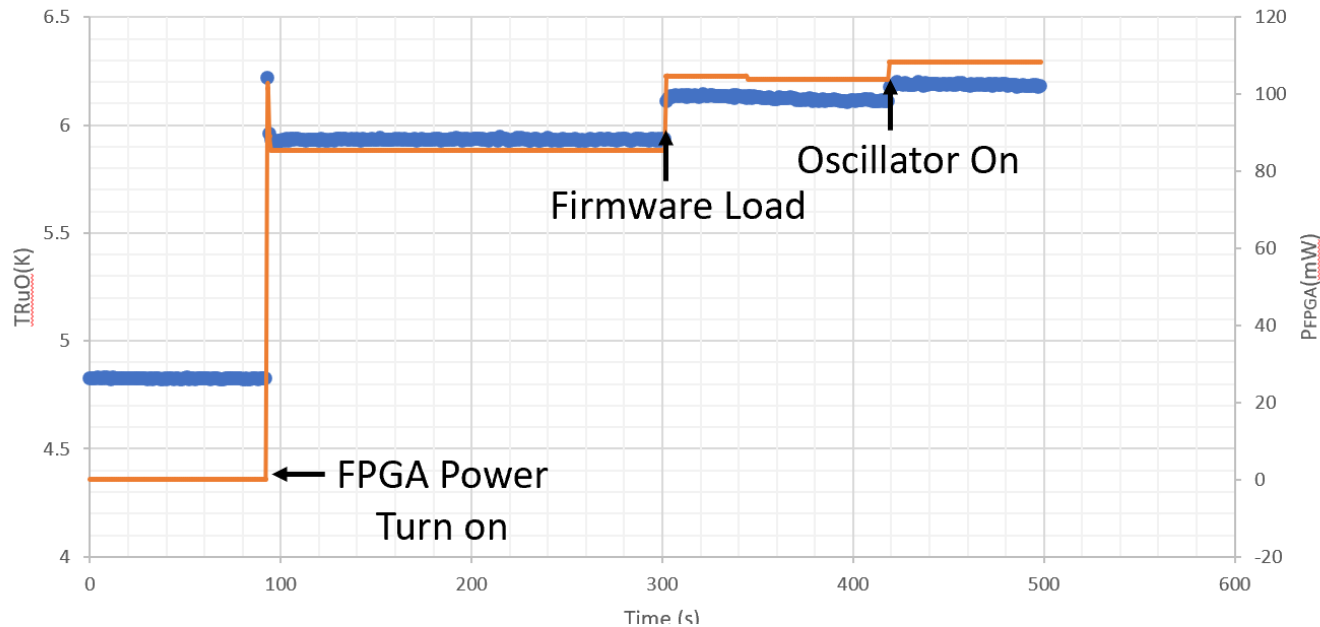


INTERNAL TEST CIRCUIT: Ring Oscillator

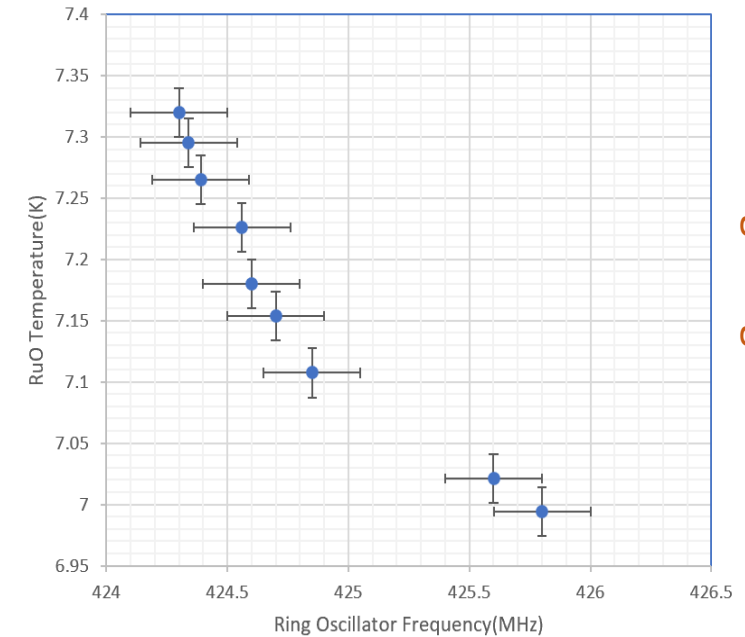
Five stage ring oscillator



Ring Oscillator @ 800MHz
RuO Thermometer vs FPGA Power

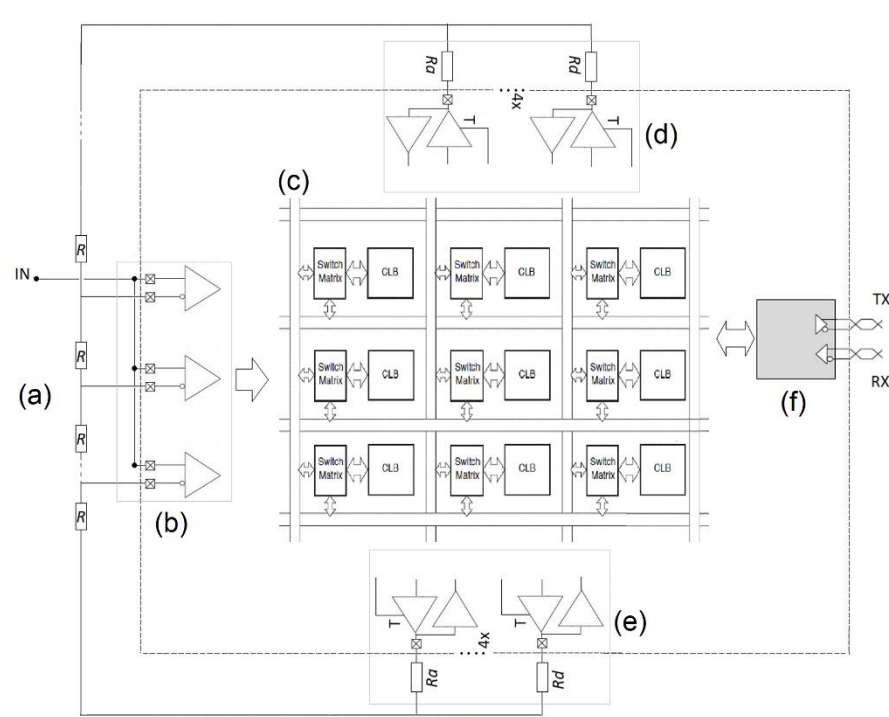


Ring Oscillator Temperature vs Frequency

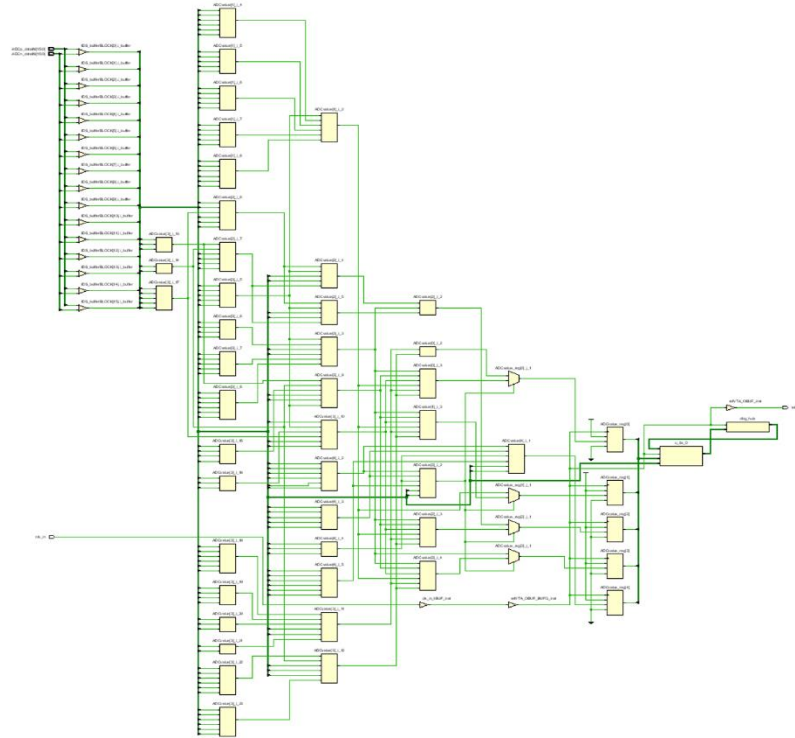


Seven stage ring oscillator

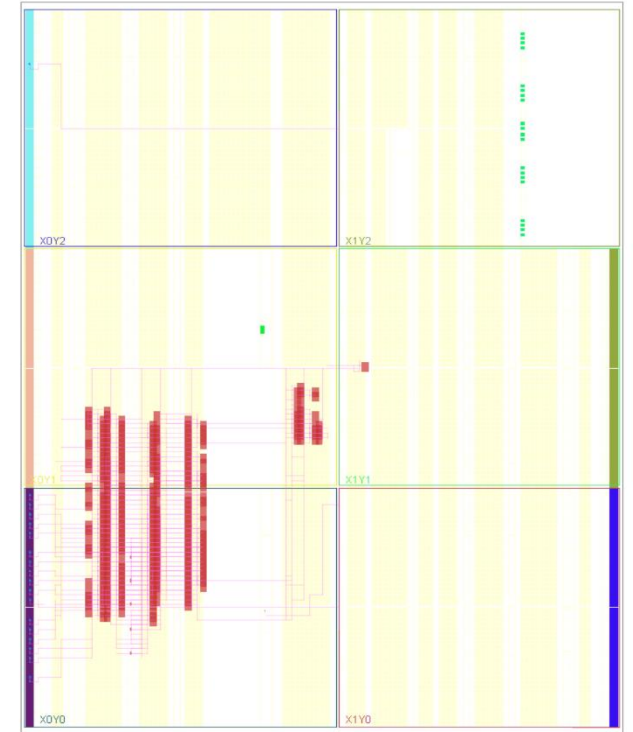
4b FLASH FOLDING ADC IMPLEMENTATION



Reconfigurable Flash Folding Architecture. With this architecture it is possible to change the ADC resolution on the fly.

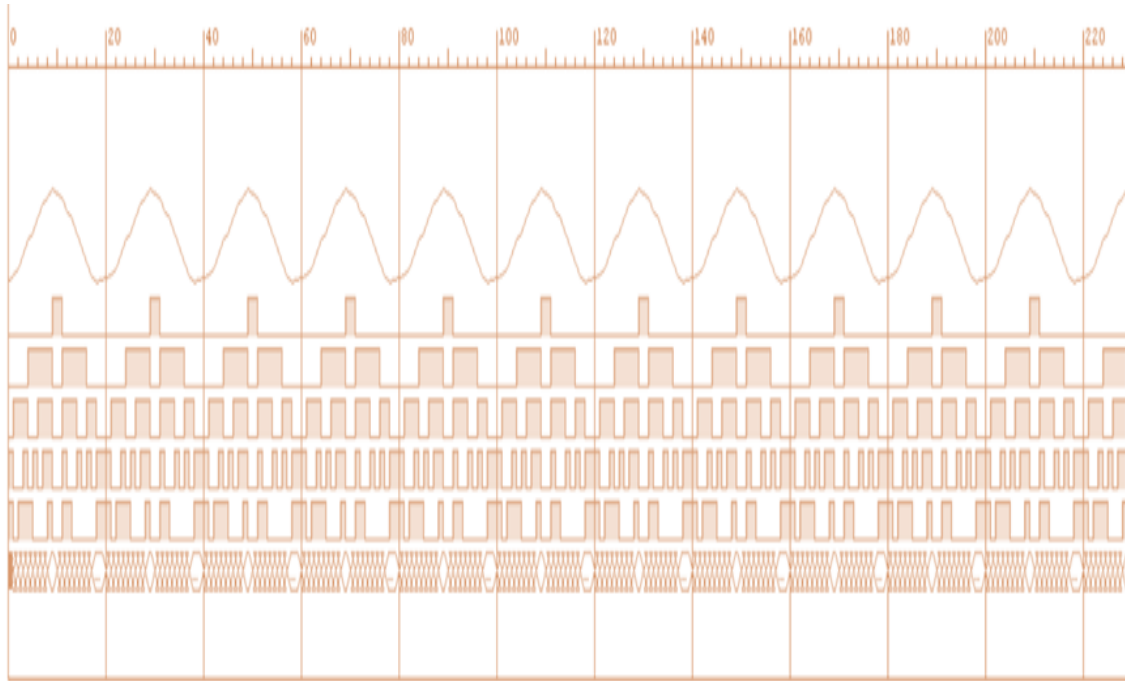


Logic implementation is based on LVDS buffers for discrimination, LUTs for decoding, and a Ring Oscillator for Clock.

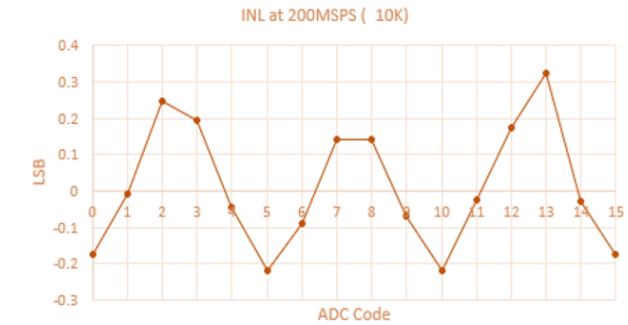
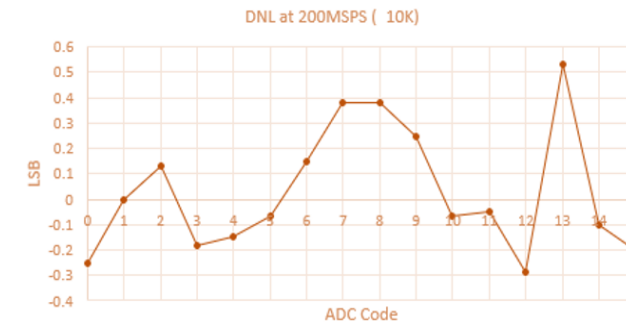
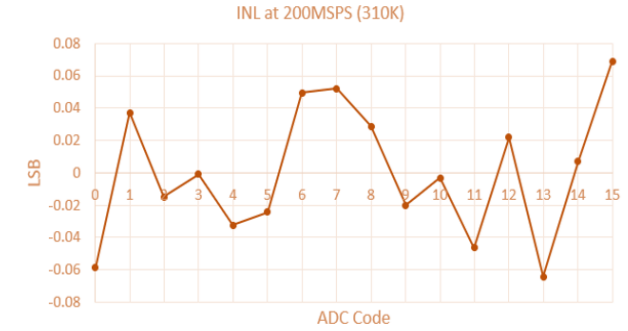
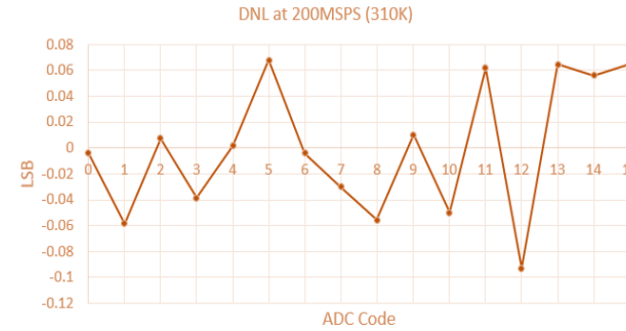


Implementation utilized under 15% of the FPGA logic resources.

4b FLASH FOLDING ADC RESULTS

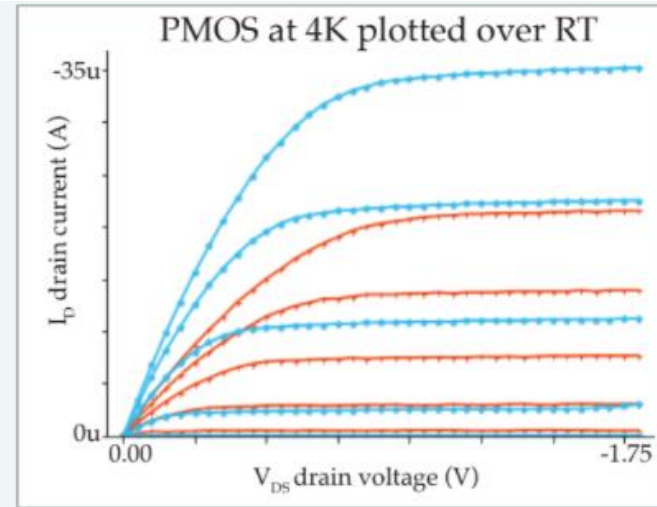
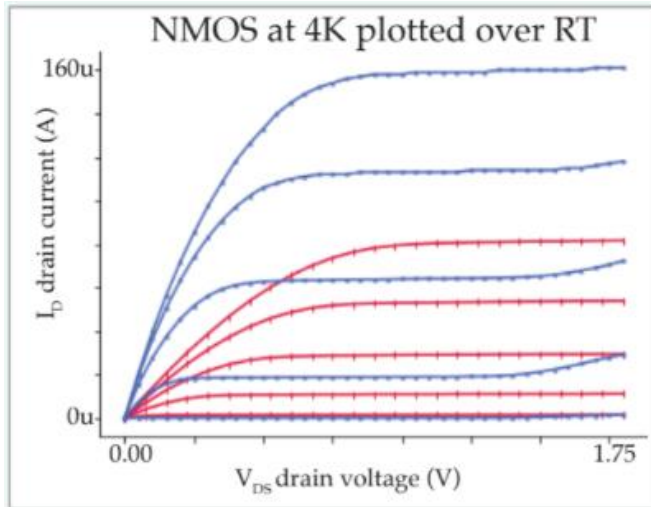
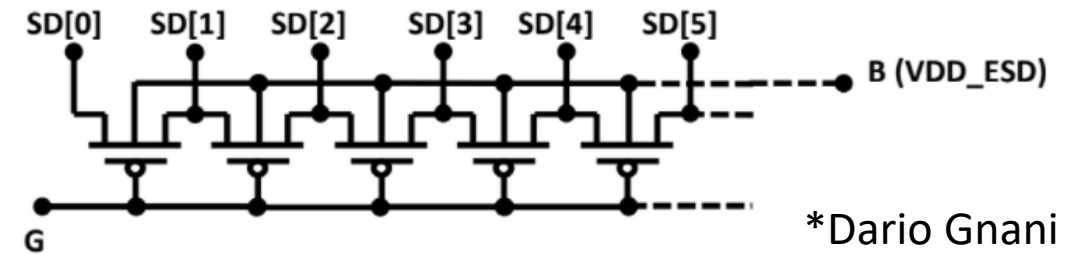
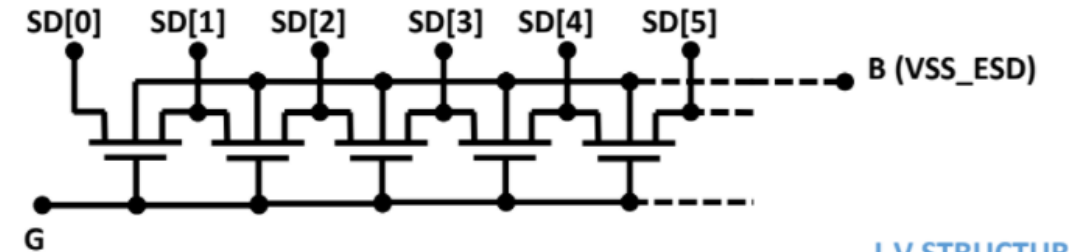
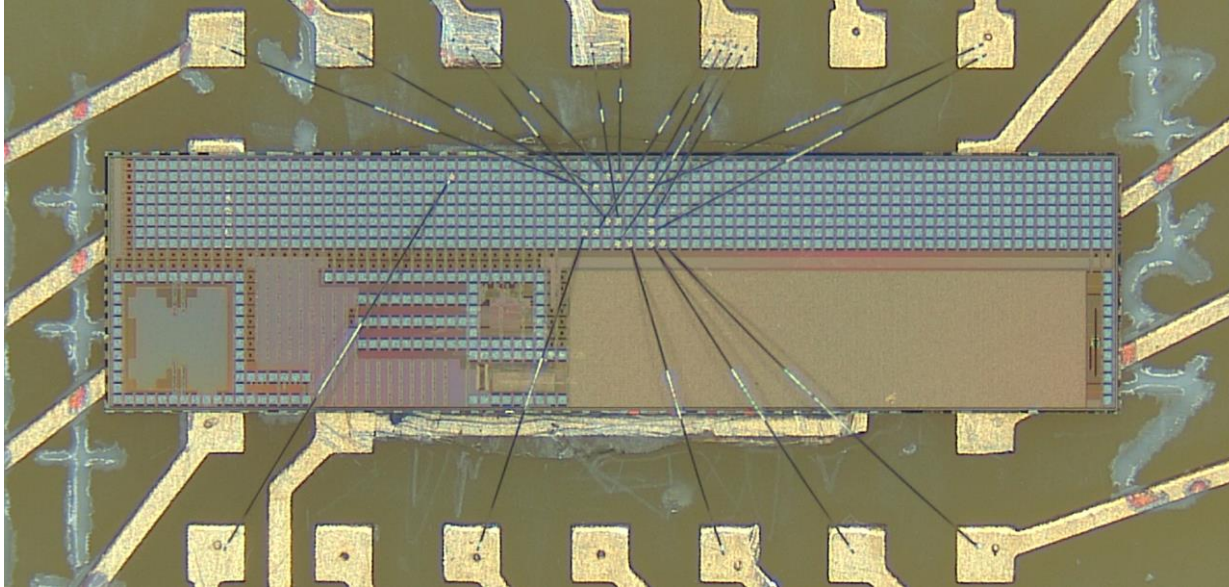


Digitization of a sine wave viewed through Chipscope. On top the reconstructed analog signal and in the bottom its digital makeup.



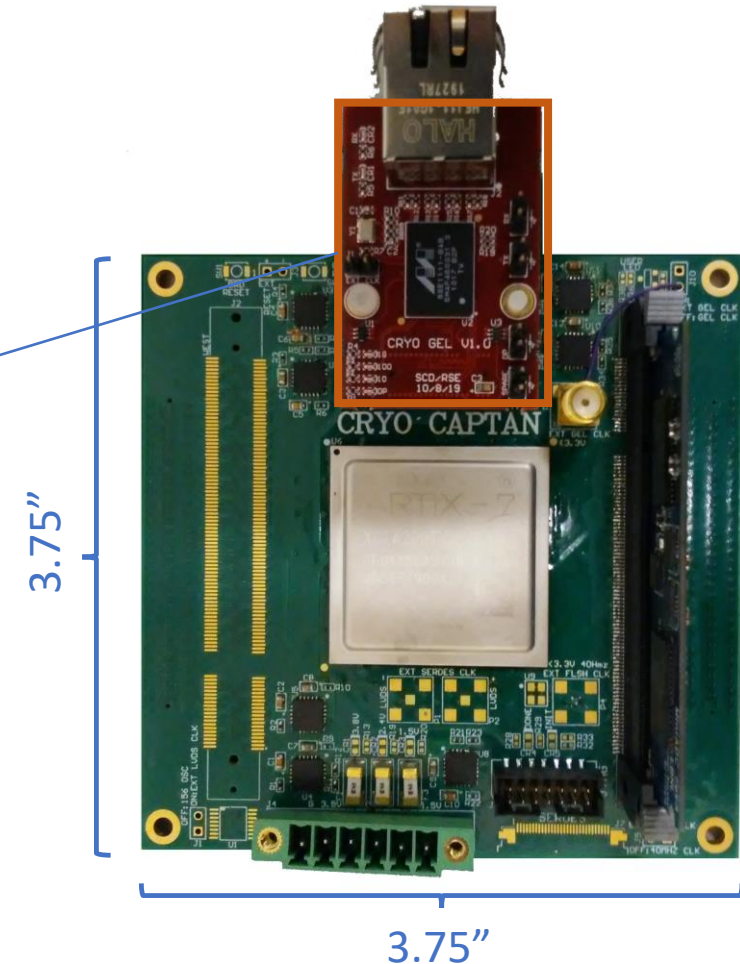
ADC noise performance at room temperature and at 10K. Notice that although thermal noise decreases with temperature the non-linearity actually increased.

SEA-OF-TRANSISTORS



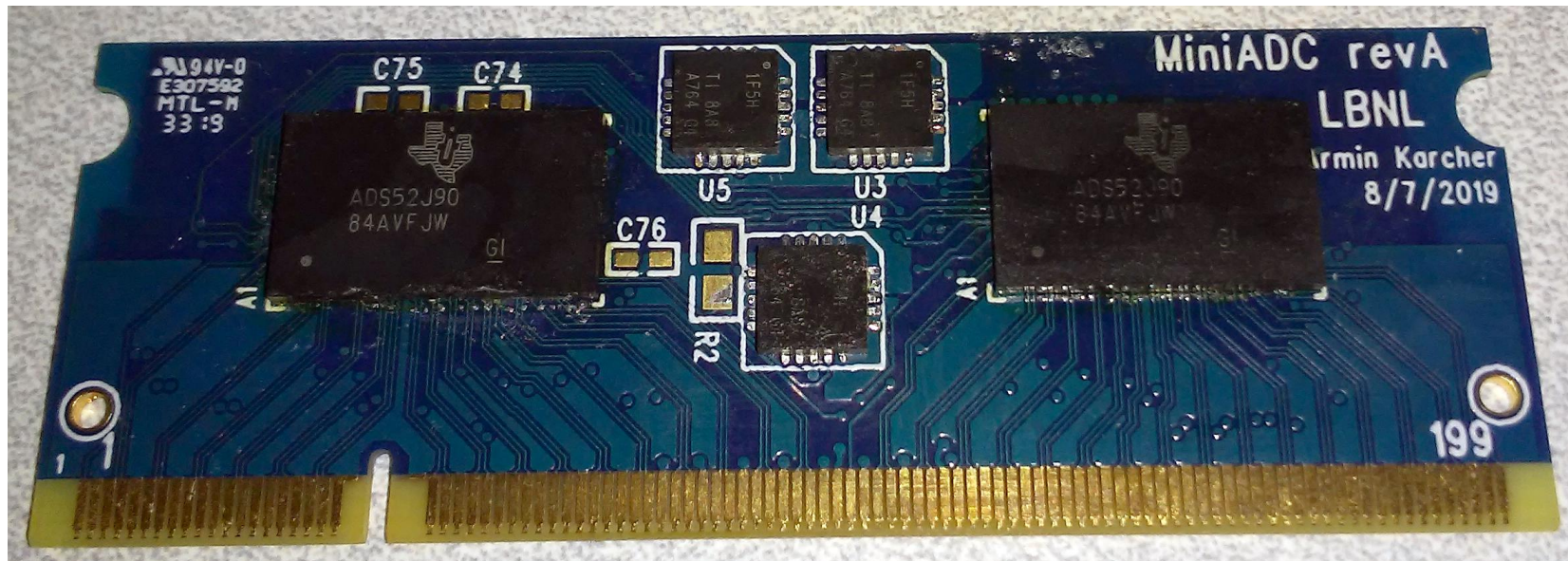
CryoDAQ – LBNL-Fermilab

- Large Artix FPGA (28nm)
- 64 Analog channels
- External Clock
- Laser Driver for communications
- LDO's
- External Clock
- Max operational clock 1GHz
- Expected around 1 W of power dissipation



CryoDAQ ADC – LBNL-Fermilab

- 32 ADCs
- Sampling rate up to 100MSPS (50MHz signals)
- 14bits
- Not tested cold yet at LBNL



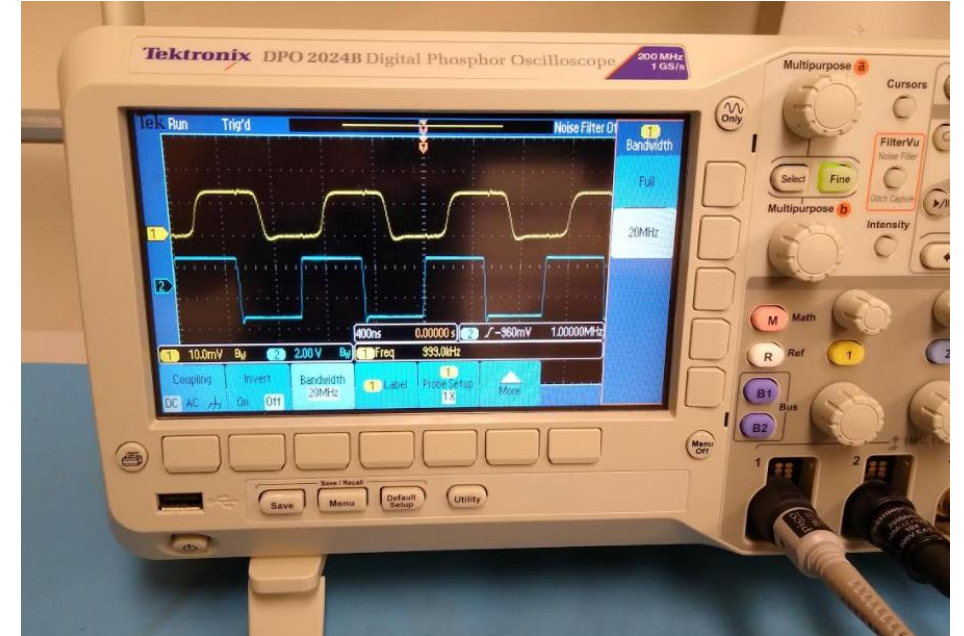
CONNECTING COMPONENTS



POF Receiver



POF Under Test



LN - Blue TX, Yellow RX (1MHz)

POF Receiver – When cold requires the receiver voltage bias to be increased. Generally the transmitter needs to work on top of a higher light intensity. Clock speeds up to 100MHz are achievable with POF.