ITS3 R&D status & MLR1 chip first results

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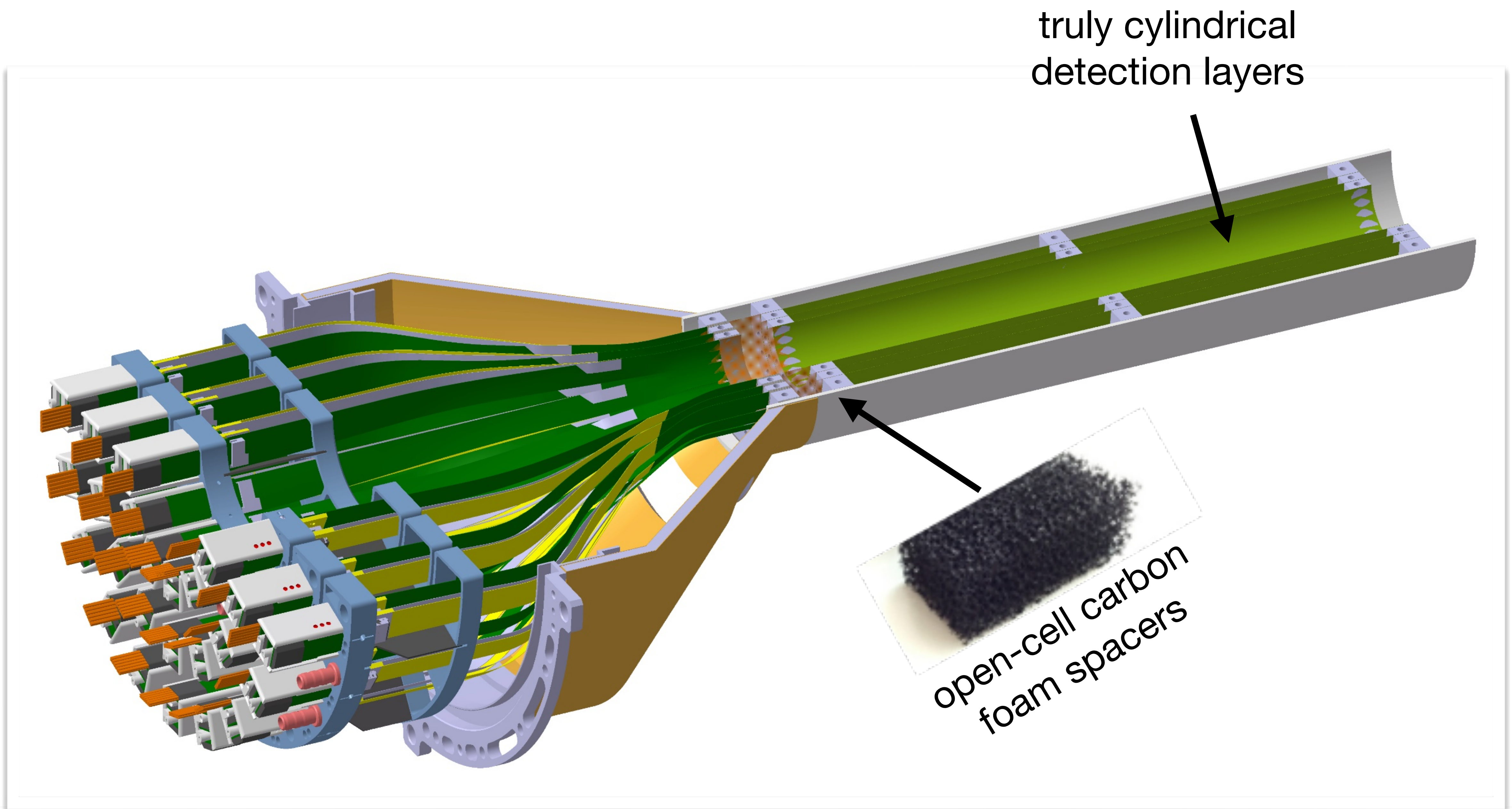
EIC group meeting
09/11/2021

Slides from
Magnus Mager (CERN) | ALICE ITS3 | CERN detector seminar

ITS3 details



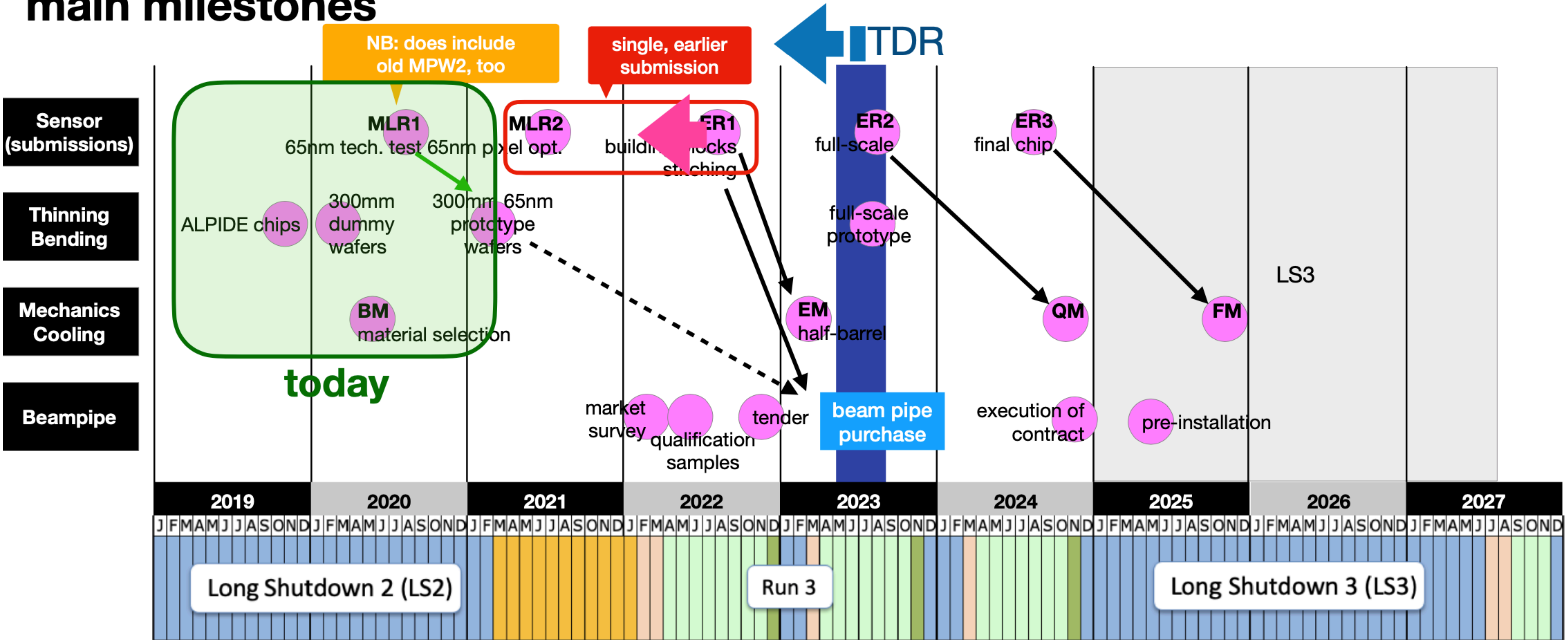
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

- Key ingredients:
  - 300 mm wafer-scale sensors, fabricated using stitching
  - thinned down to 20-40 µm (0.02-0.04% X_0), making them flexible
  - bent to the target radii
  - mechanically held in place by carbon foam ribs
- Key benefits:
  - extremely low material budget: 0.02-0.04% X_0 (beampipe: 500 µm Be: 0.14% X_0)
  - homogeneous material distribution: negligible systematic error from material distribution

The whole detector will consist of six (!) sensors (current ITS IB: 432) – and barely anything else

Timeline

main milestones



NB: does include old MPW2, too

single, earlier submission

TDR

Sensor (submissions)

Thinning Bending

Mechanics Cooling

Beampipe

MLR1
65nm tech. test

65nm pixel opt.
MLR2

building blocks stitching
ER1

ER2
full-scale

ER3
final chip

ALPIDE chips

300mm dummy wafers

300mm 65nm prototype wafers

full-scale prototype

BM
material selection

EM
half-barrel

QM

FM

LS3

today

market survey

qualification samples

tender

beam pipe purchase

execution of contract

pre-installation

2019 2020 2021 2022 2023 2024 2025 2026 2027

J F M A M J J A S O N D

Long Shutdown 2 (LS2)

Run 3

Long Shutdown 3 (LS3)

MLR: multiple layer per reticle, **ER:** engineering run,
BM: breadboard module, **EM:** engineering module, **QM:** qualification module, **FM:** final module

On track!

Beam test of bend MAPS

A series of beam tests was performed in 2020 and 2021:

- Jun 2020 (DESY): first bent chip
- Aug 2020 (DESY): bent chip on cylinder
- Dec 2020 (DESY): bent chip at large radii
- Apr 2021 (DESY): bent chips at all radii, carbon foam
- Jul 2021 (SPS): µITS3, “W”
- Sep 2021 (DESY): MLR1, “W”, carbon foam

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Beam test: bent chip testing

1st paper: arxiv:2105.13000

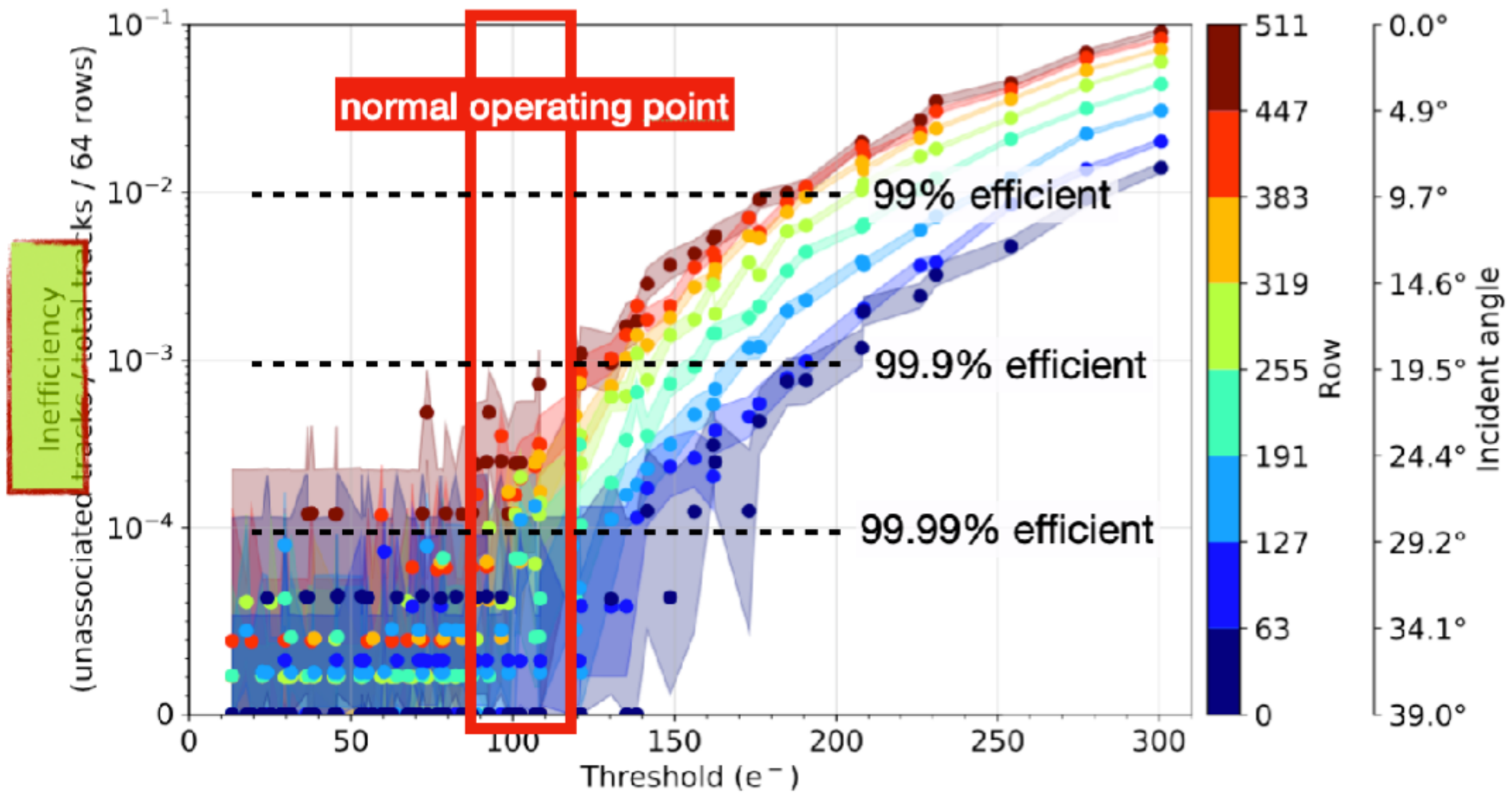
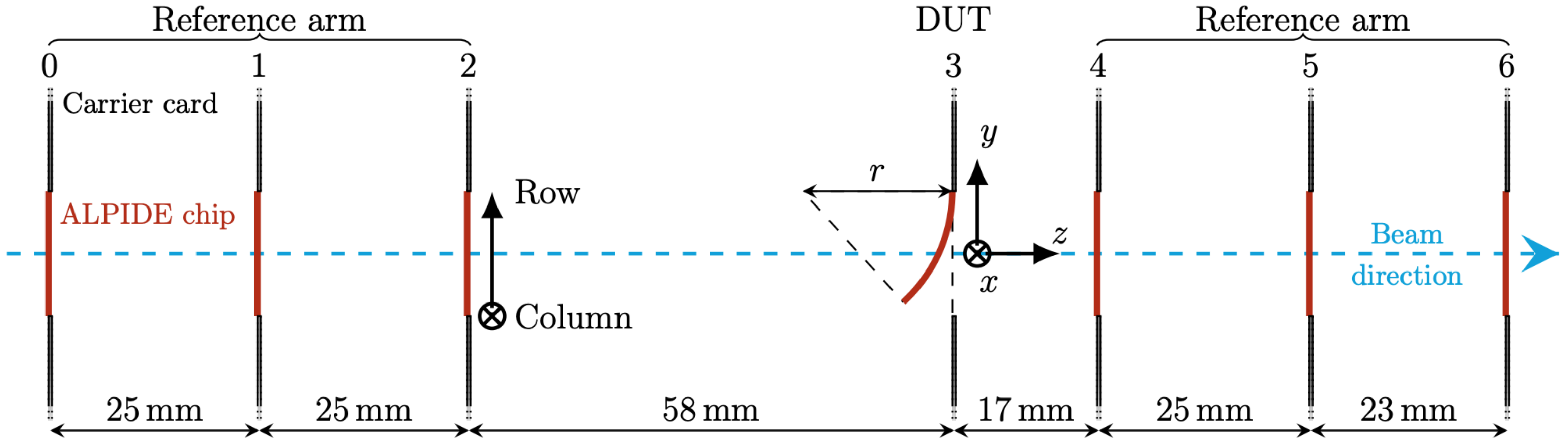
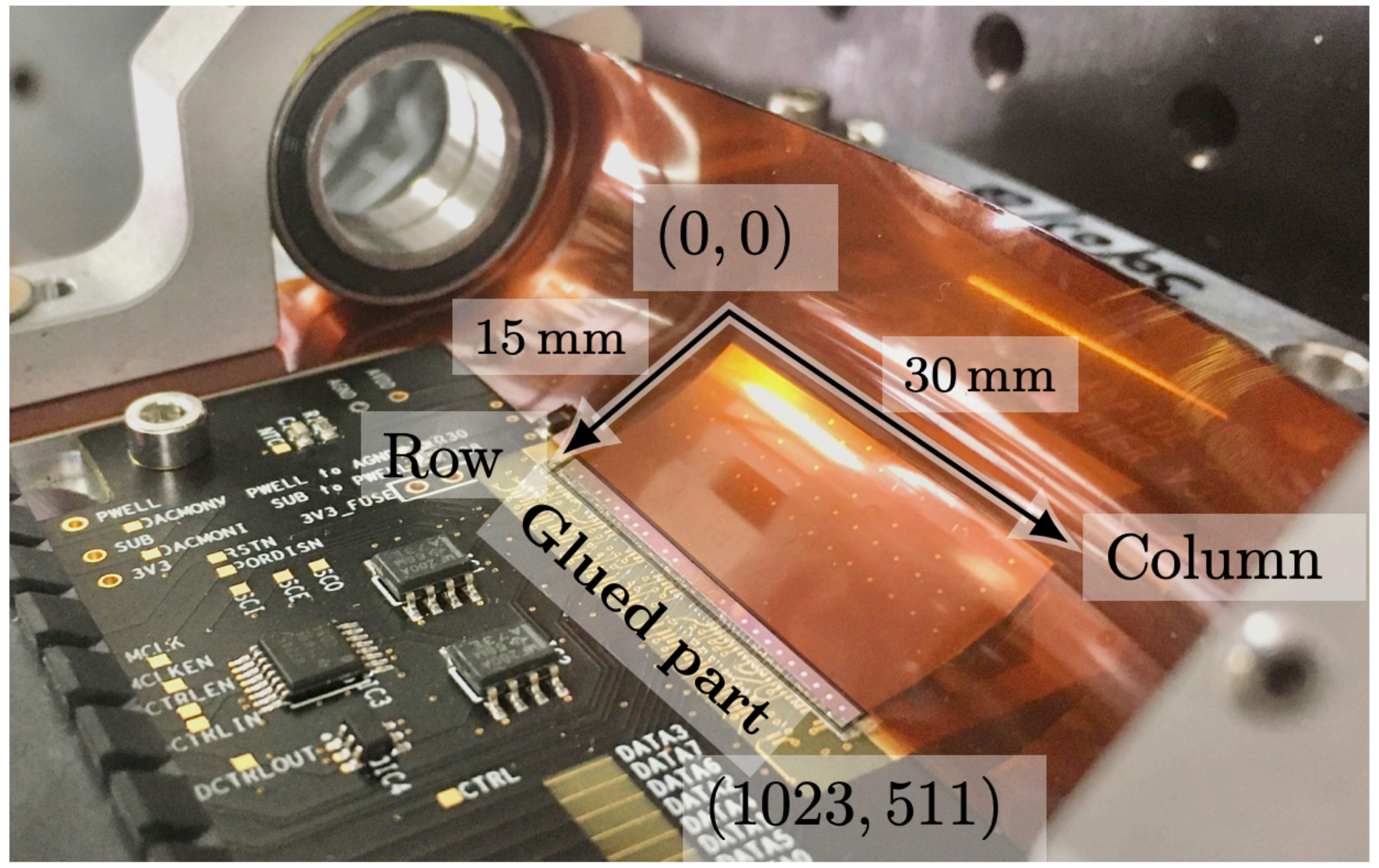
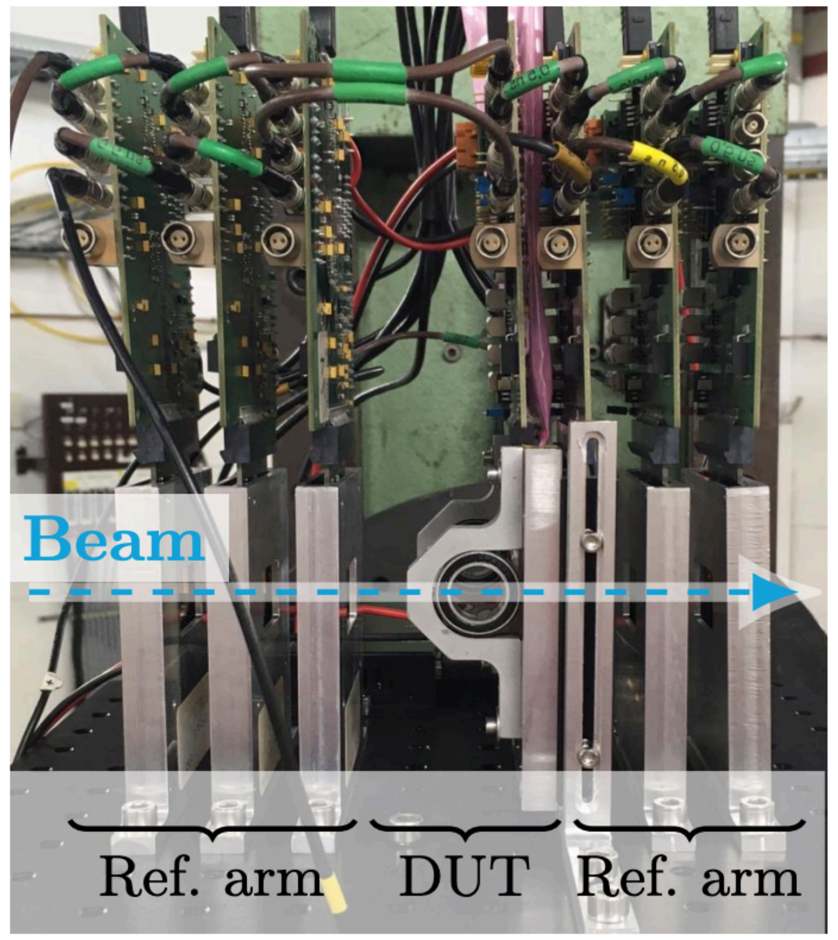


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.





(a) Bent ALPIDE chip on the carrier card

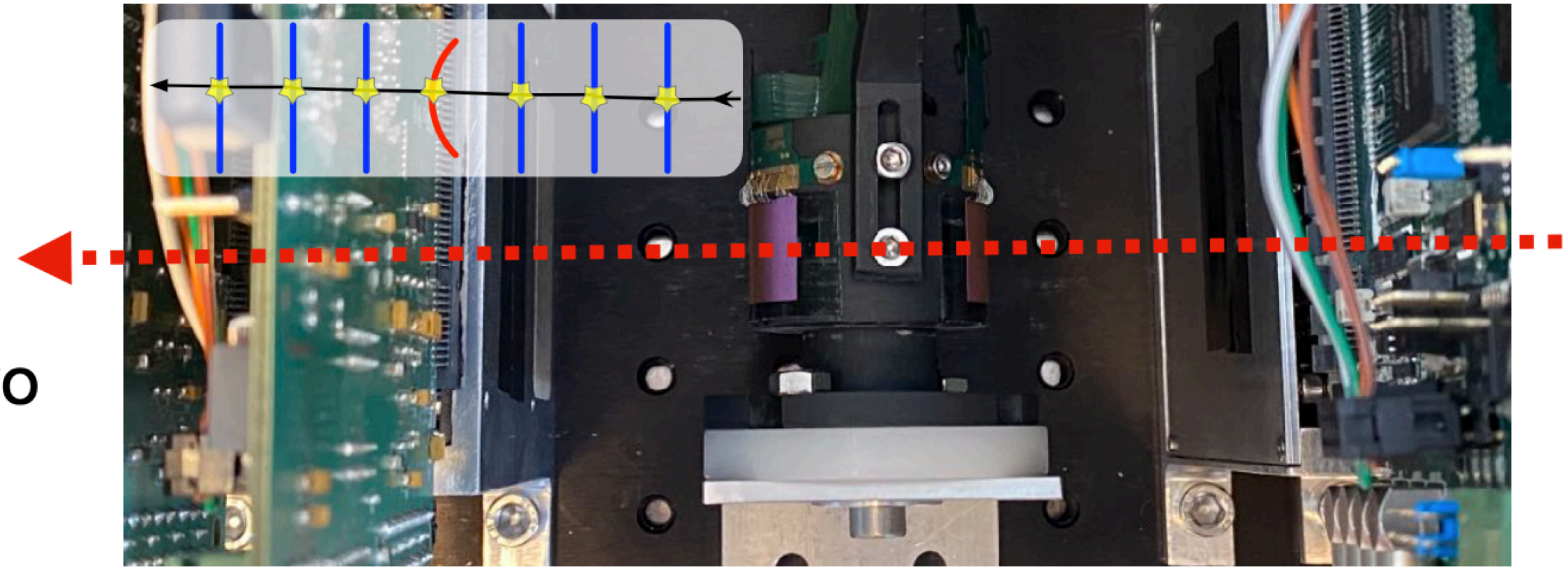


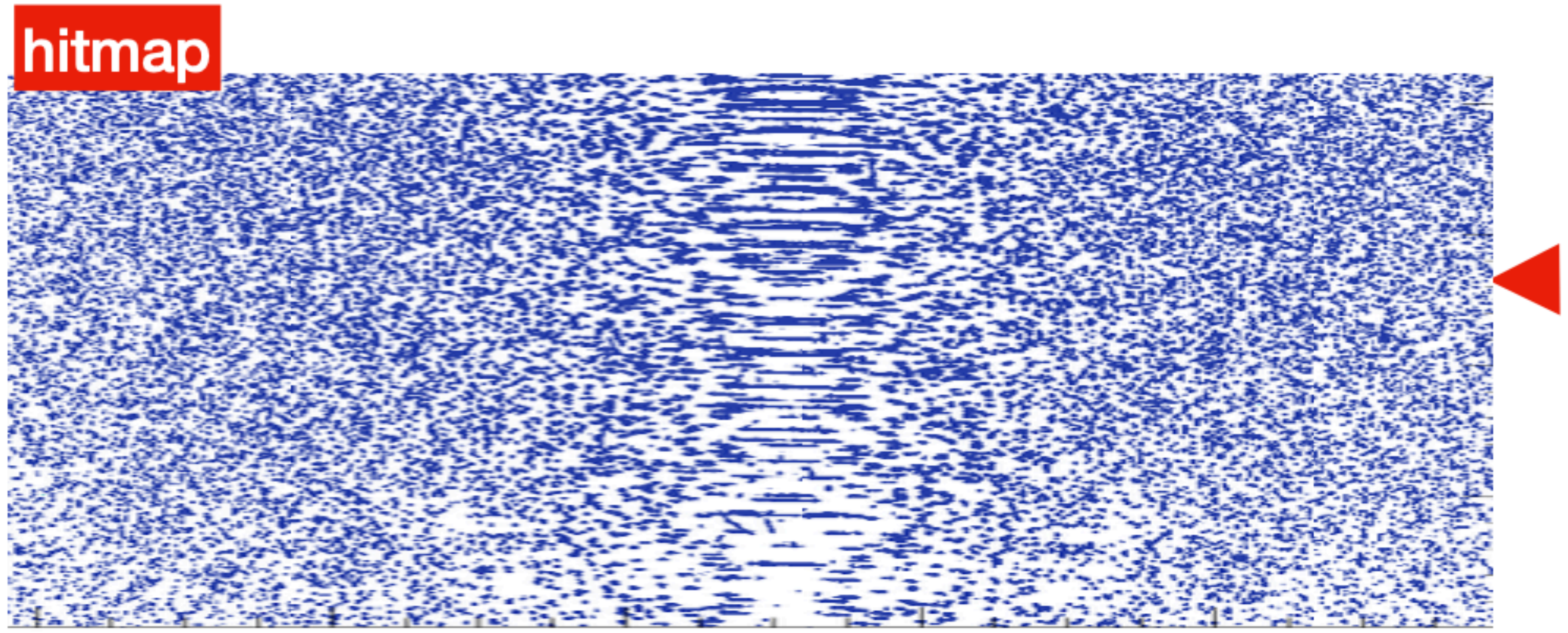
(b) Testbeam telescope

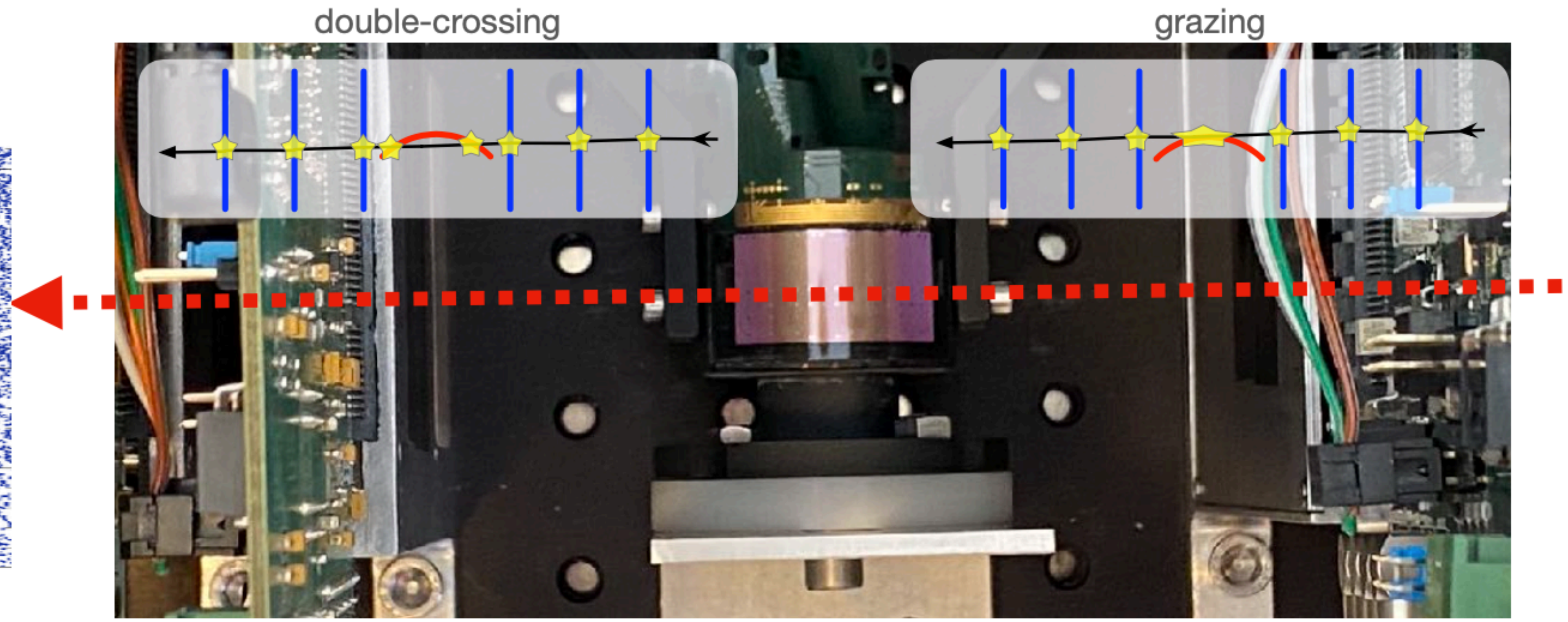
sensors maintain their excellent performance after bending, with detection efficiencies above 99.9 %

Beam test: bent chip on cylinder

- Very interesting geometries are becoming possible
- For instance, one can observe two crossings of the same particle

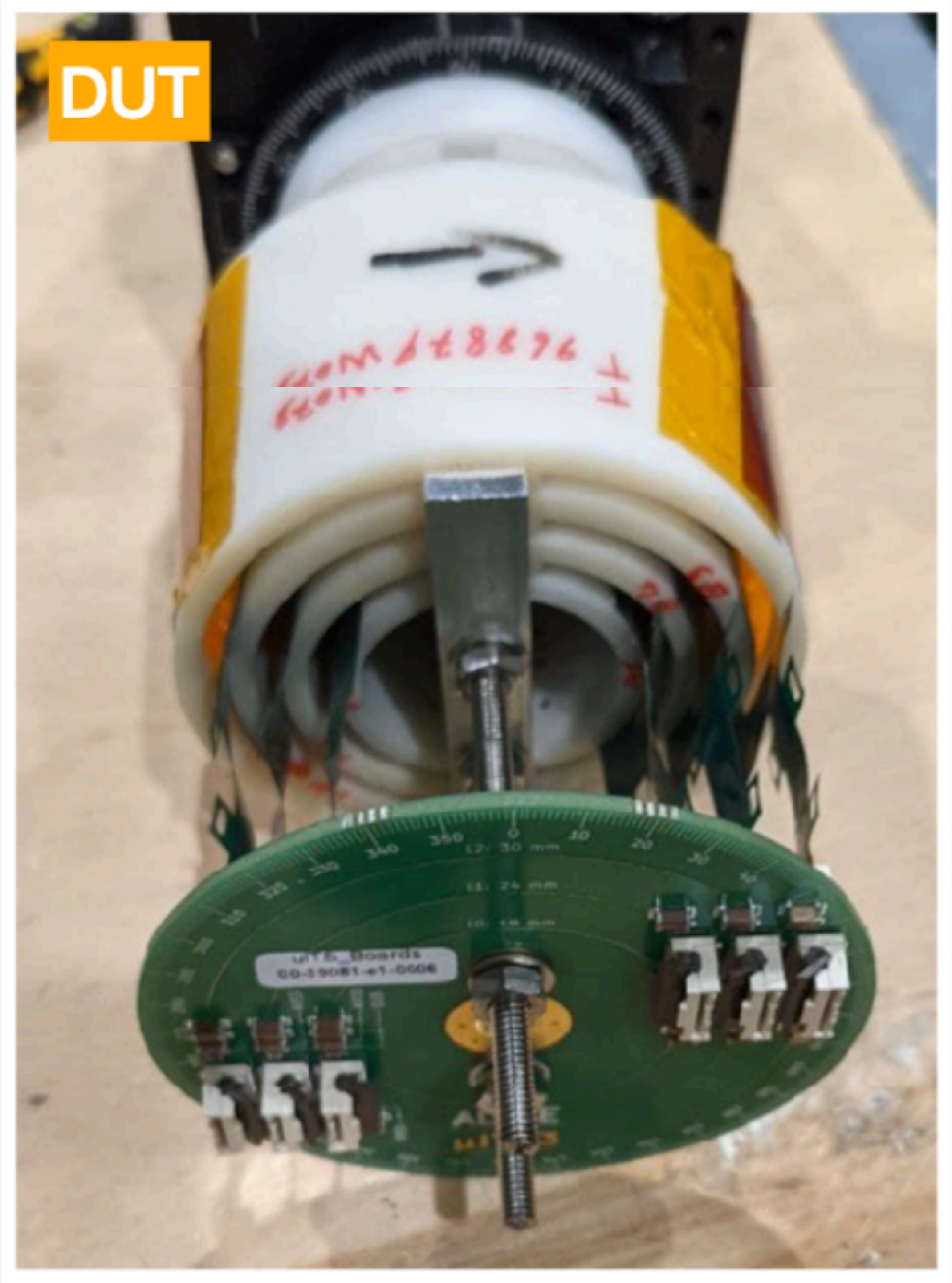


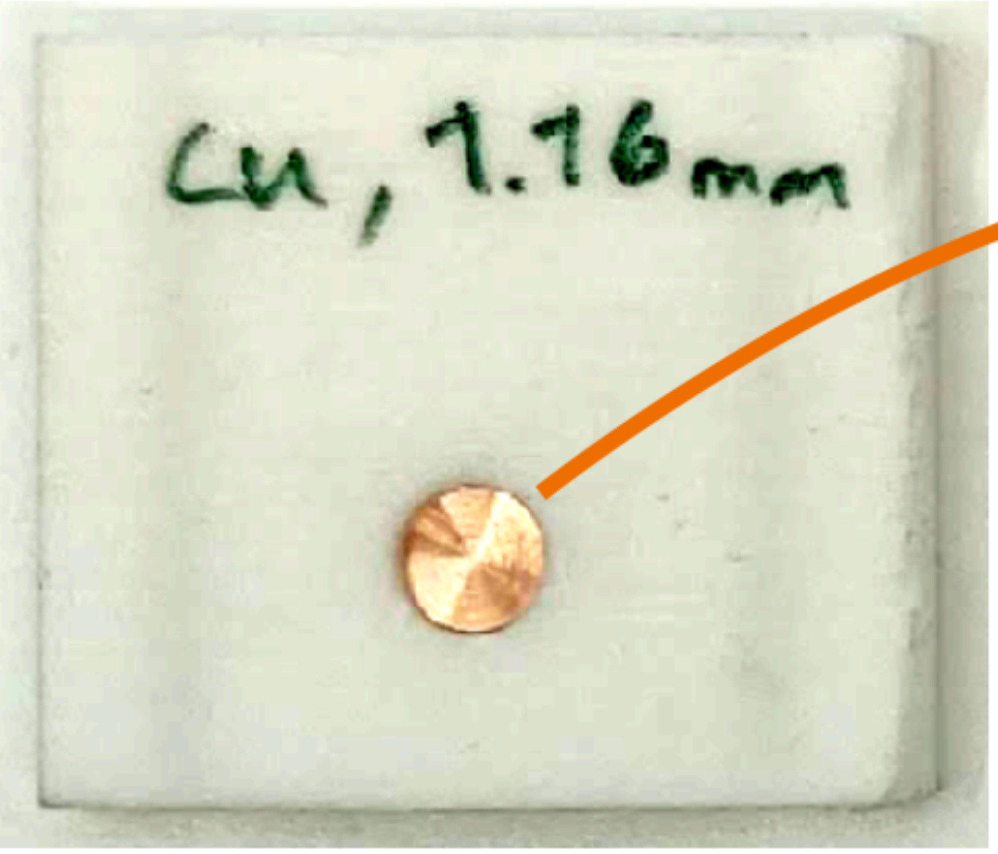


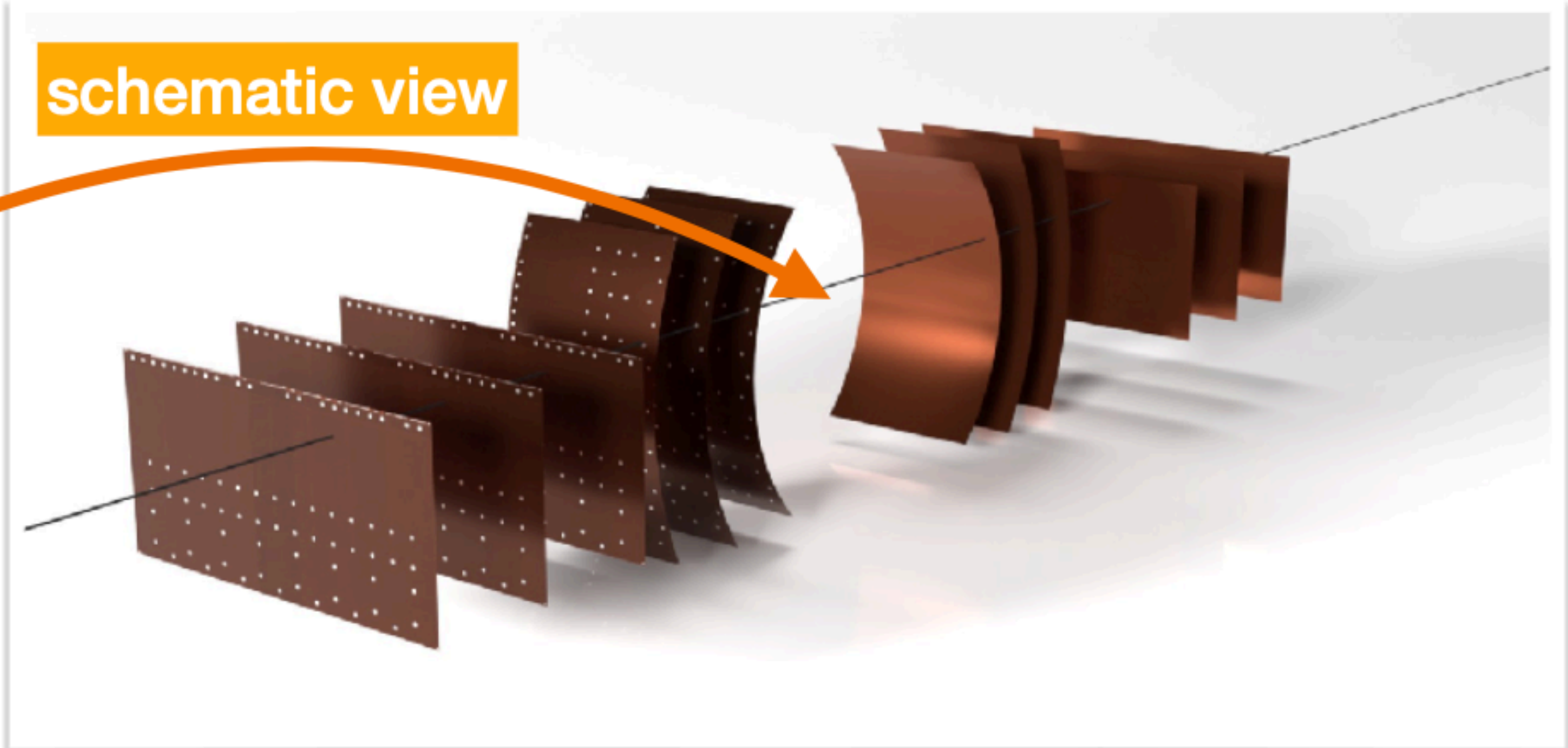


Beam test: μITS3 setup

- μITS3, i.e. 6 ALPIDEs at ITS3 radii
  - two complete setups based on “gold” quality ALPIDE chips
  - one has a Cu target in the center: expect to see 120 GeV proton/pion–Cu collisions
- Several days of continuous data taking
  - detailed analysis ongoing

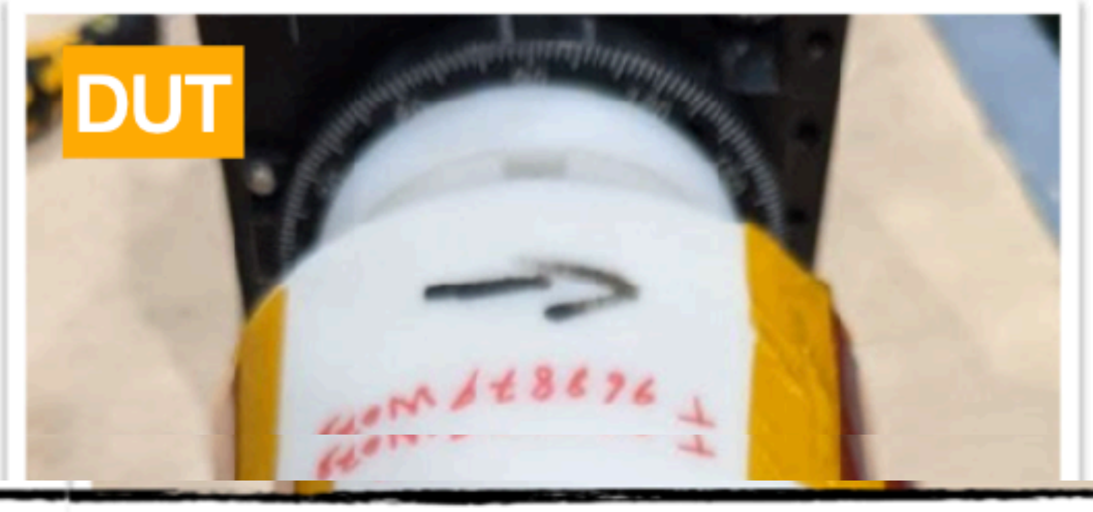




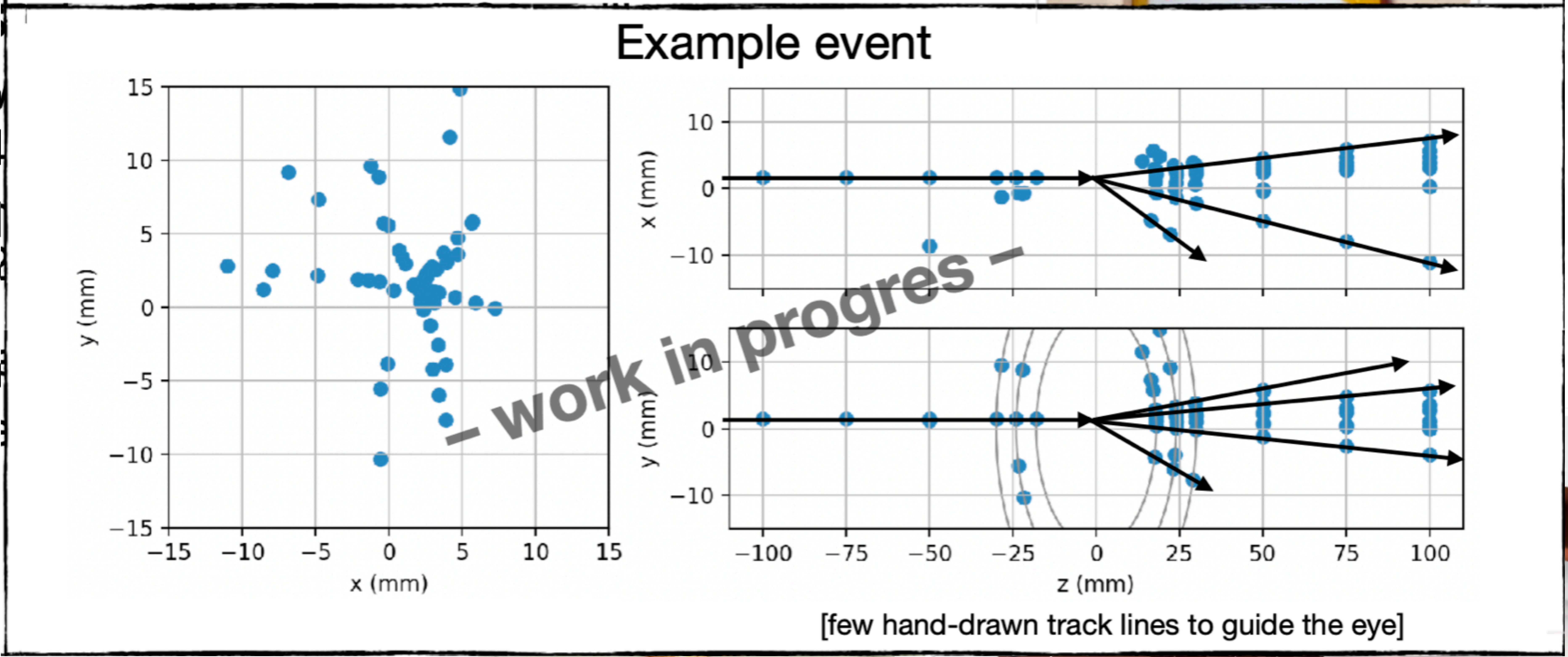


First “real” experiment, allows to study tracking/reconstruction

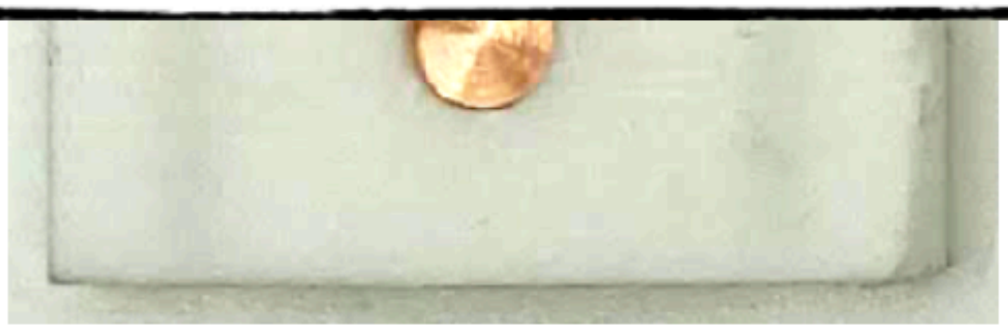
Beam test: μITS3 setup



- μITS3,
  - two
    ALPI
  - one
    120
- Severa
  - deta


Example event

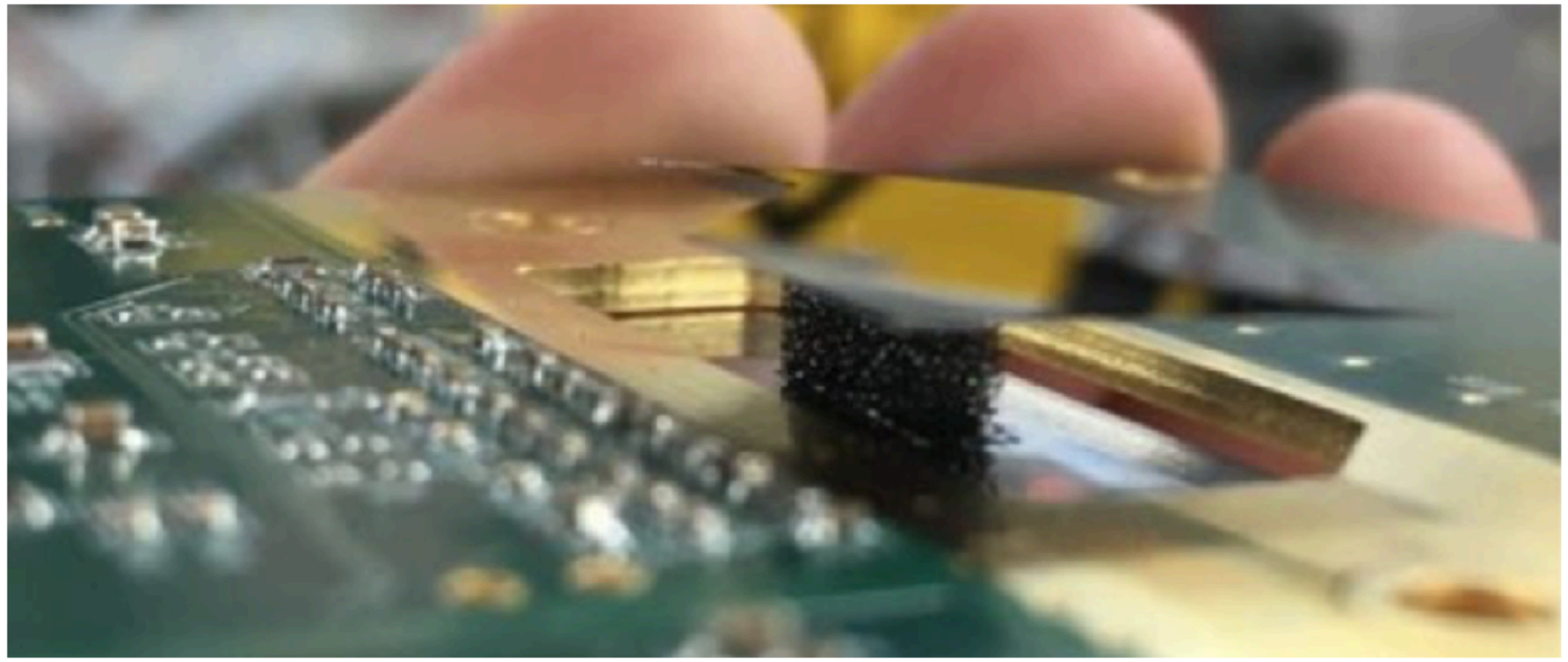
[few hand-drawn track lines to guide the eye]

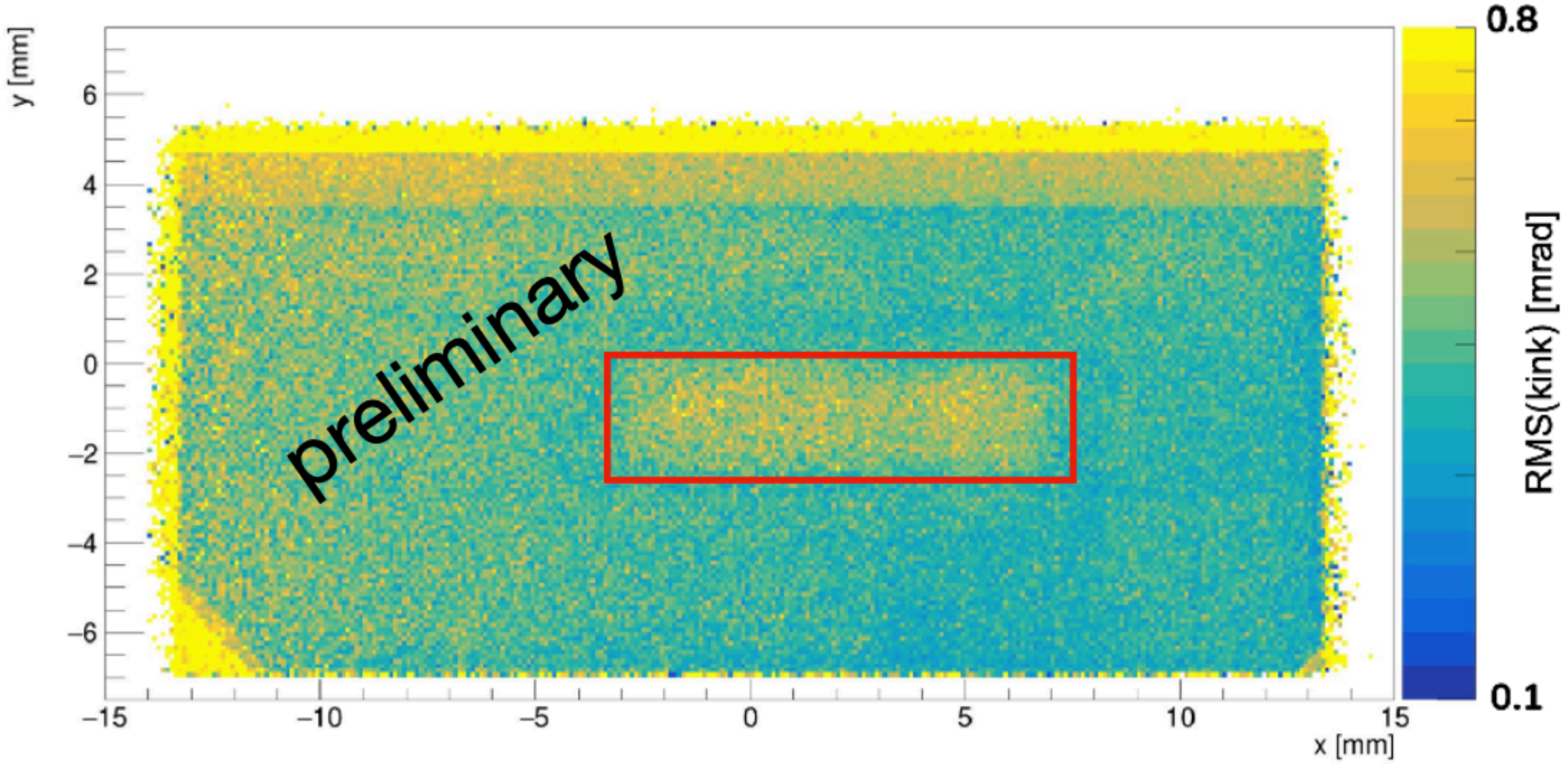


First “real” experiment, allows to study tracking/reconstruction

Beam test: material budget studies (carbon foam)

- A sandwich of chip-foam-chip was brought to beam
- Scattering angle due to carbon foam is measured
- Very small (but visible) effect, as expected

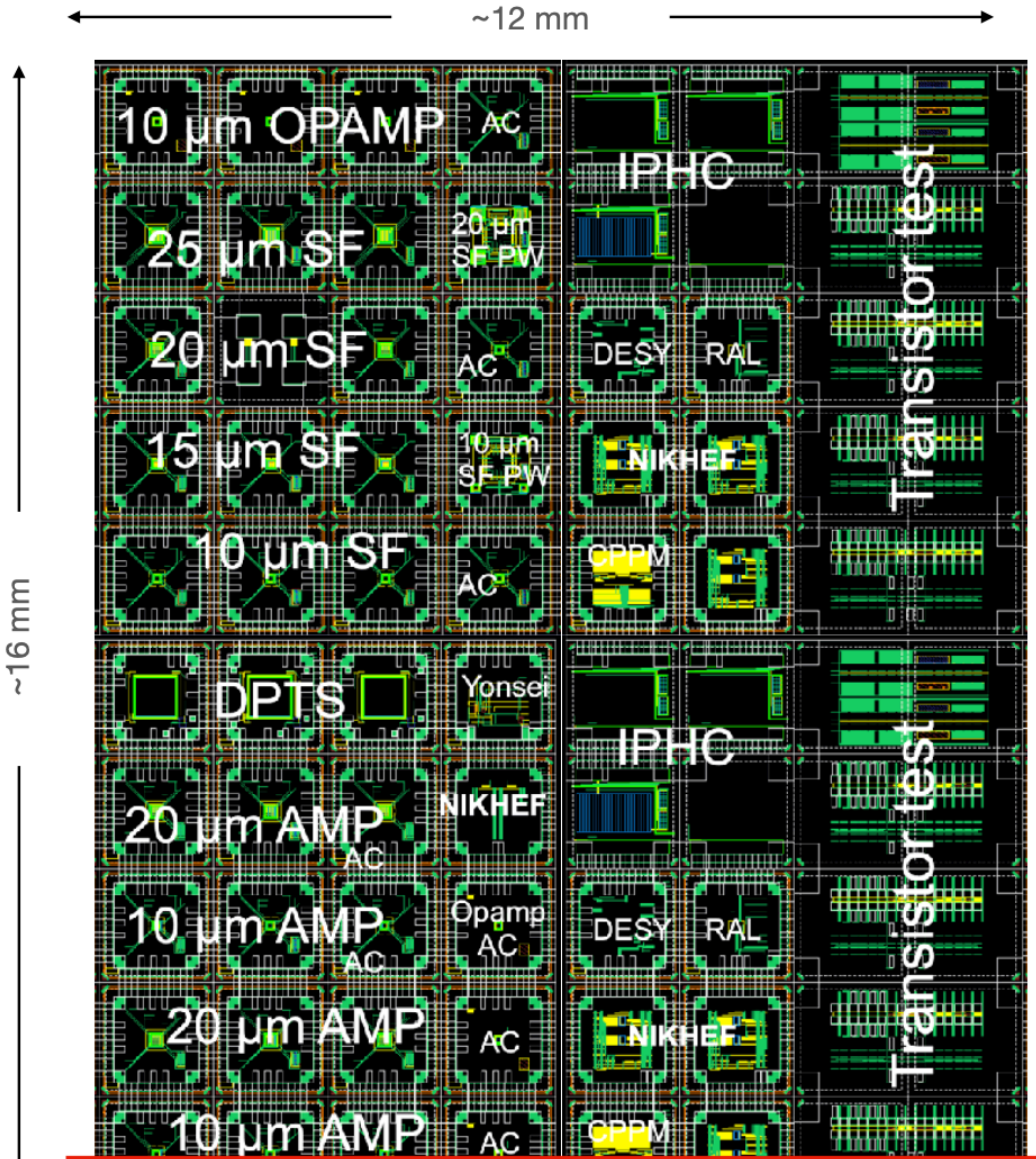




Gives confidence in system-level X_0 numbers, tests now done routinely for glueing optimisation

Sensor R&D

65 nm prototypes, MLR1



- First submission in TowerJazz 65nm
  - scoped within CERN EP R&D WP1.2
  - significant drive from ITS3
  - + important contributions from outside (not ALICE) groups
- Contained several test chips
  - radiation test structures
  - pixel test structures
  - pixel matrices
  - analog building blocks (band gaps, LVDS drivers, etc)

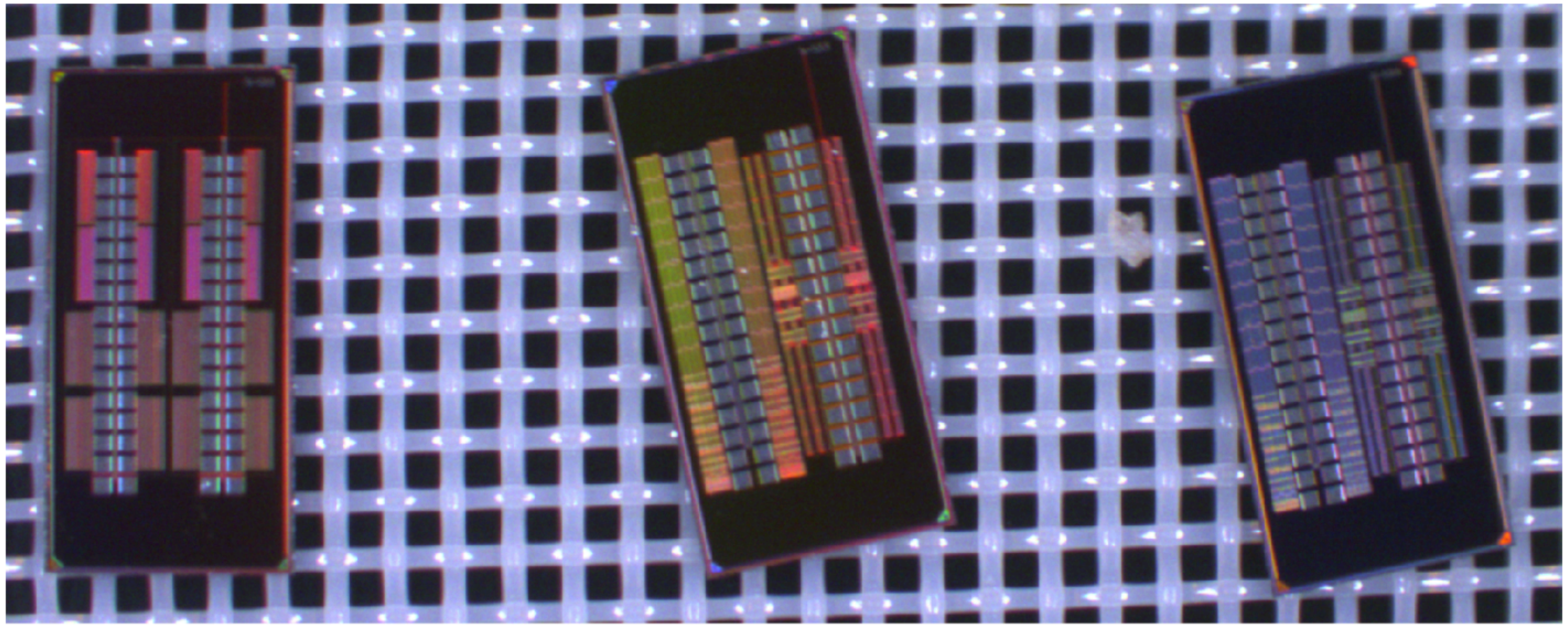
Very versatile first submission, combining what was initially planned for 2 MPWs

Sensor R&D

65 nm prototypes, MLR1

transistor test structures

- Compatible with existing test system based on probe card
- Tests have already started
  - no apparent showstoppers so far
  - detailed analysis ongoing and in discussion with foundry



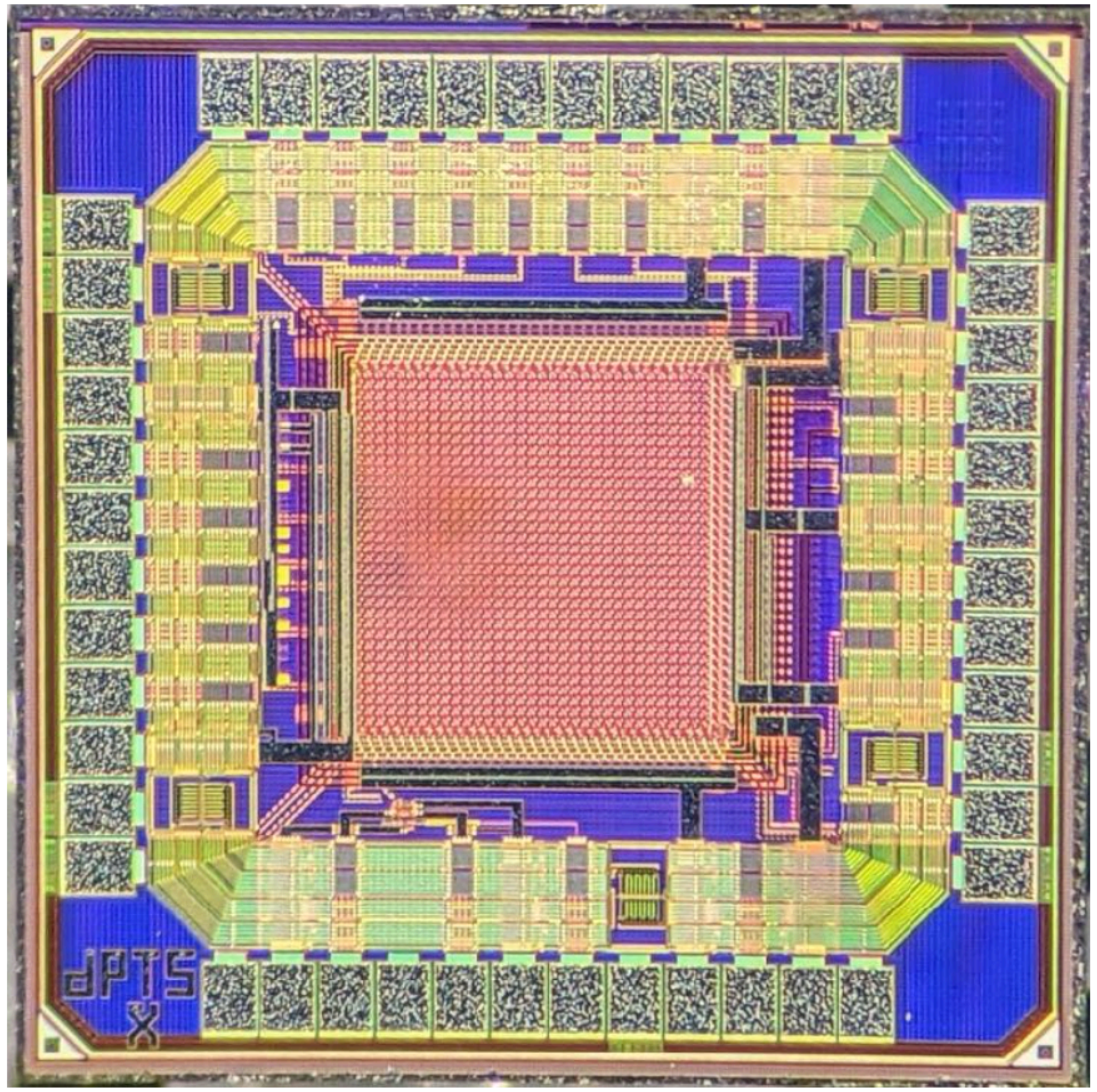
Very encouraging results, clears first milestone of 65 nm verification

Sensor R&D

65 nm prototypes, MLR1

Digital Pixel Test Structure (DPTS)

- 32 x 32 pixels, 15 μm pitch
  - sizeable prototype, allows for “easy” test beam integration
- Asynchronous digital readout with ToT information
- Allows to verify:
  - sensor performance
  - front-end performance
  - basic digital building blocks

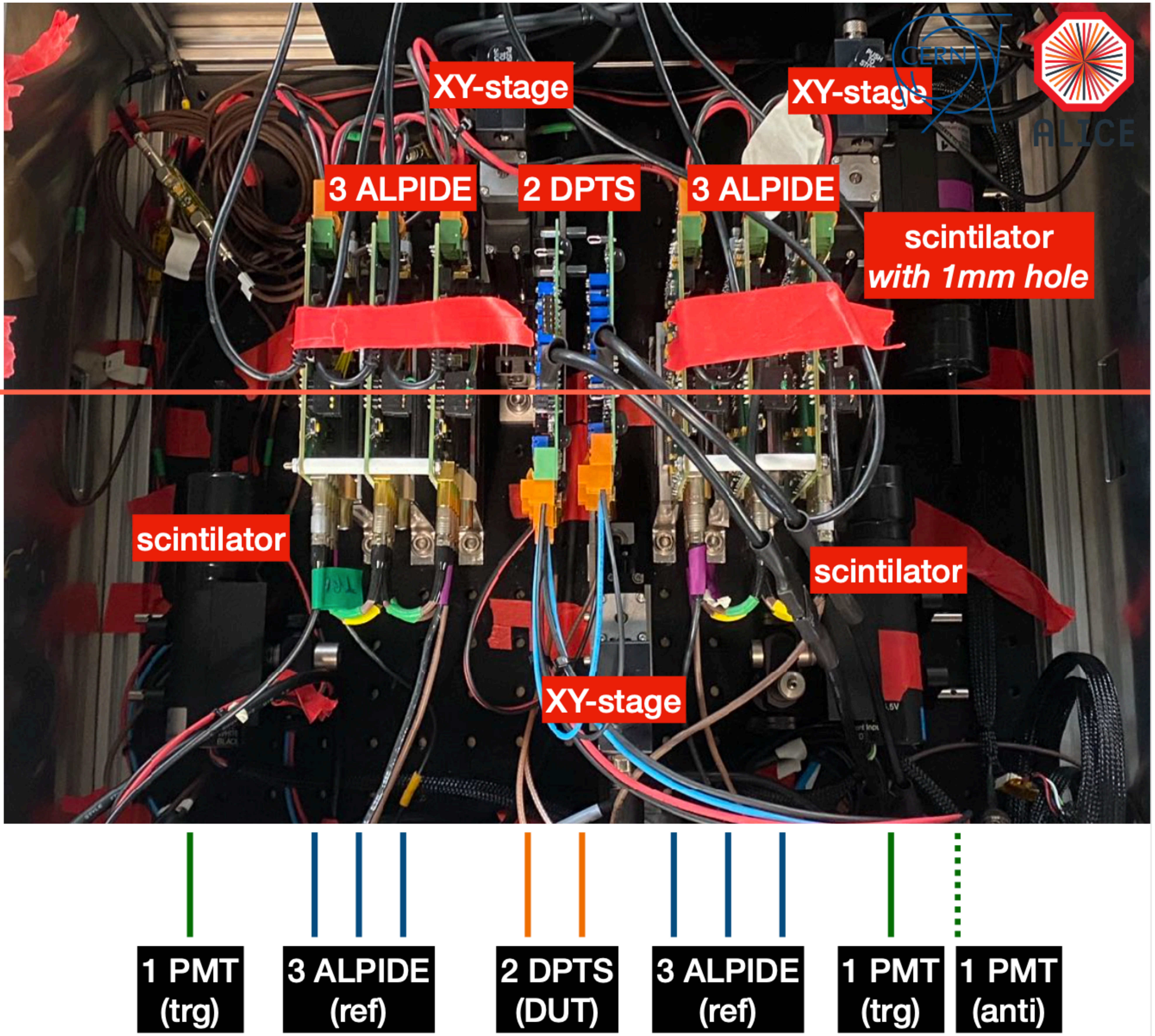


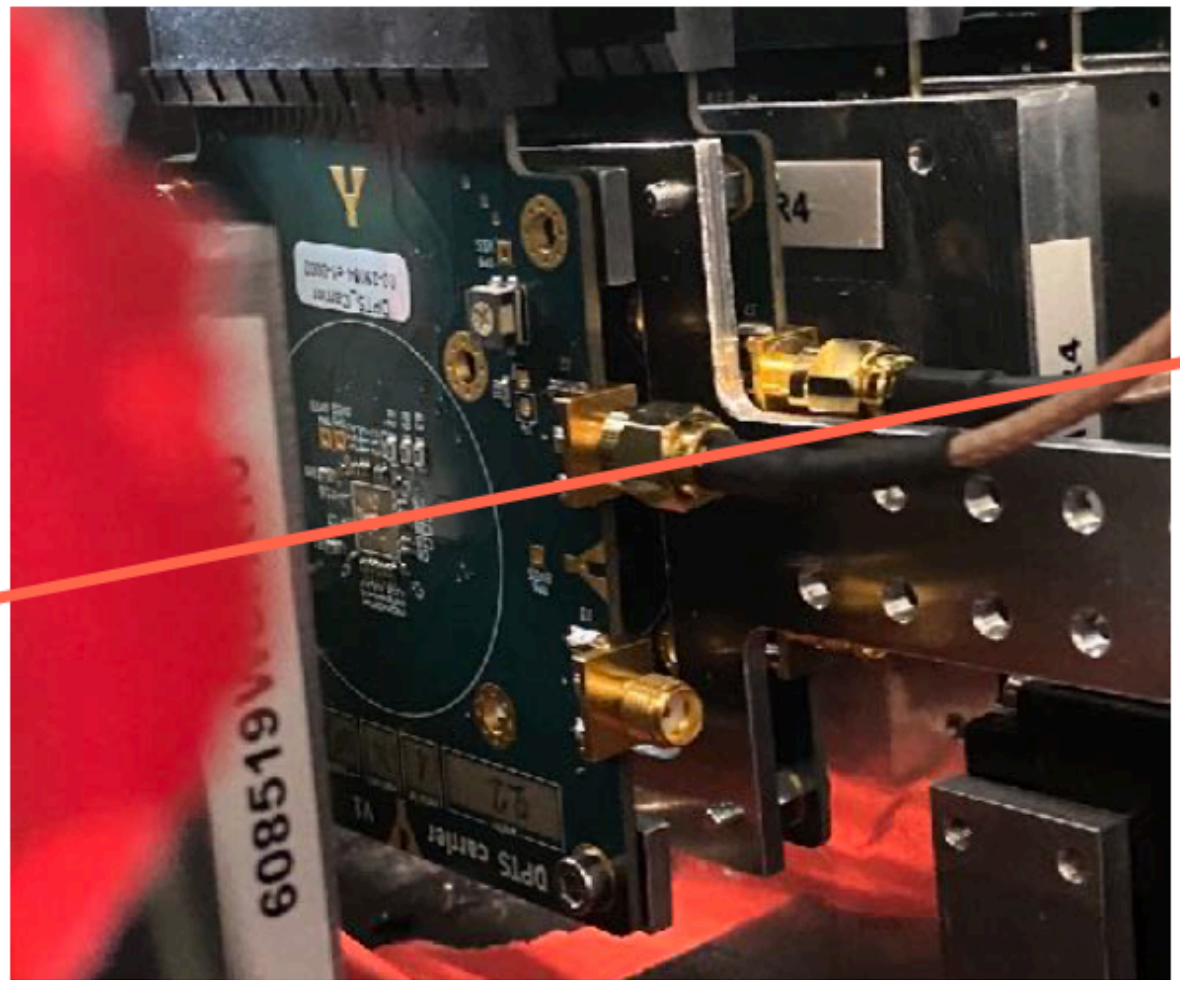
Sensor R&D

First beam test

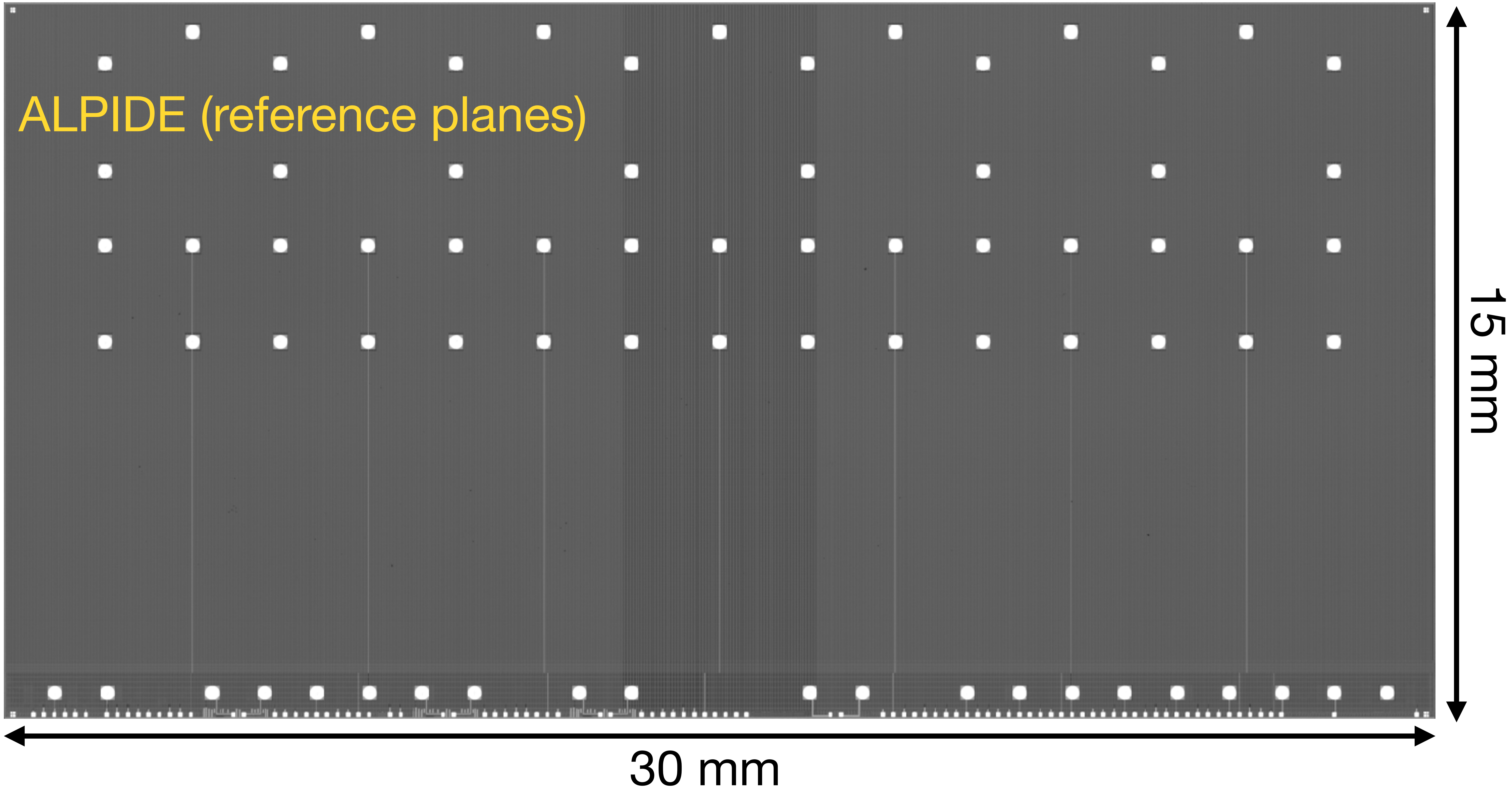
Telescope with DPTS

- Scintillator with 1mm hole can be used to trigger on narrow beam spot
- 6 precision linear stages with remote control allow to precisely align 2 DTPS and scintillators





Schematic setup



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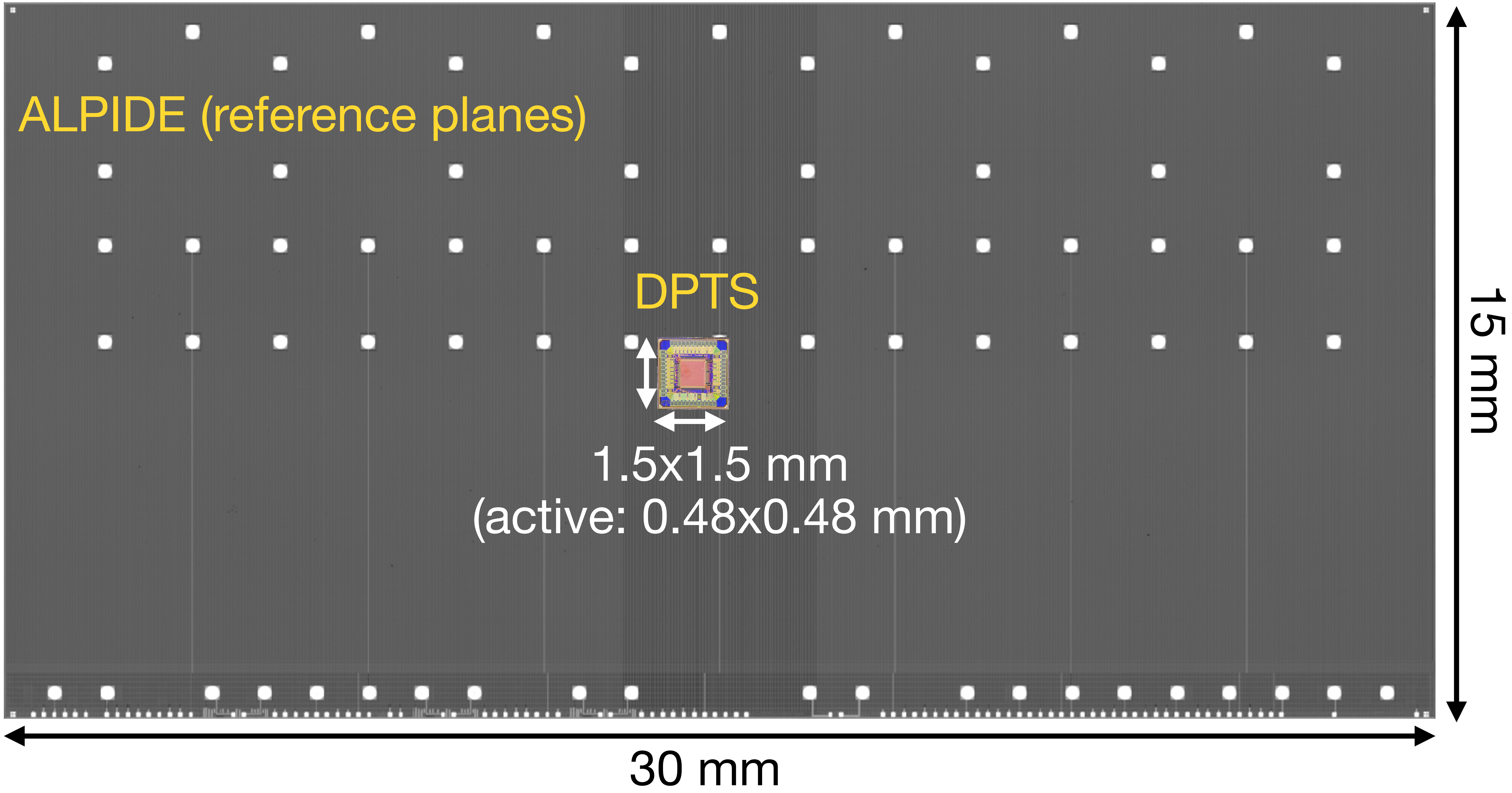
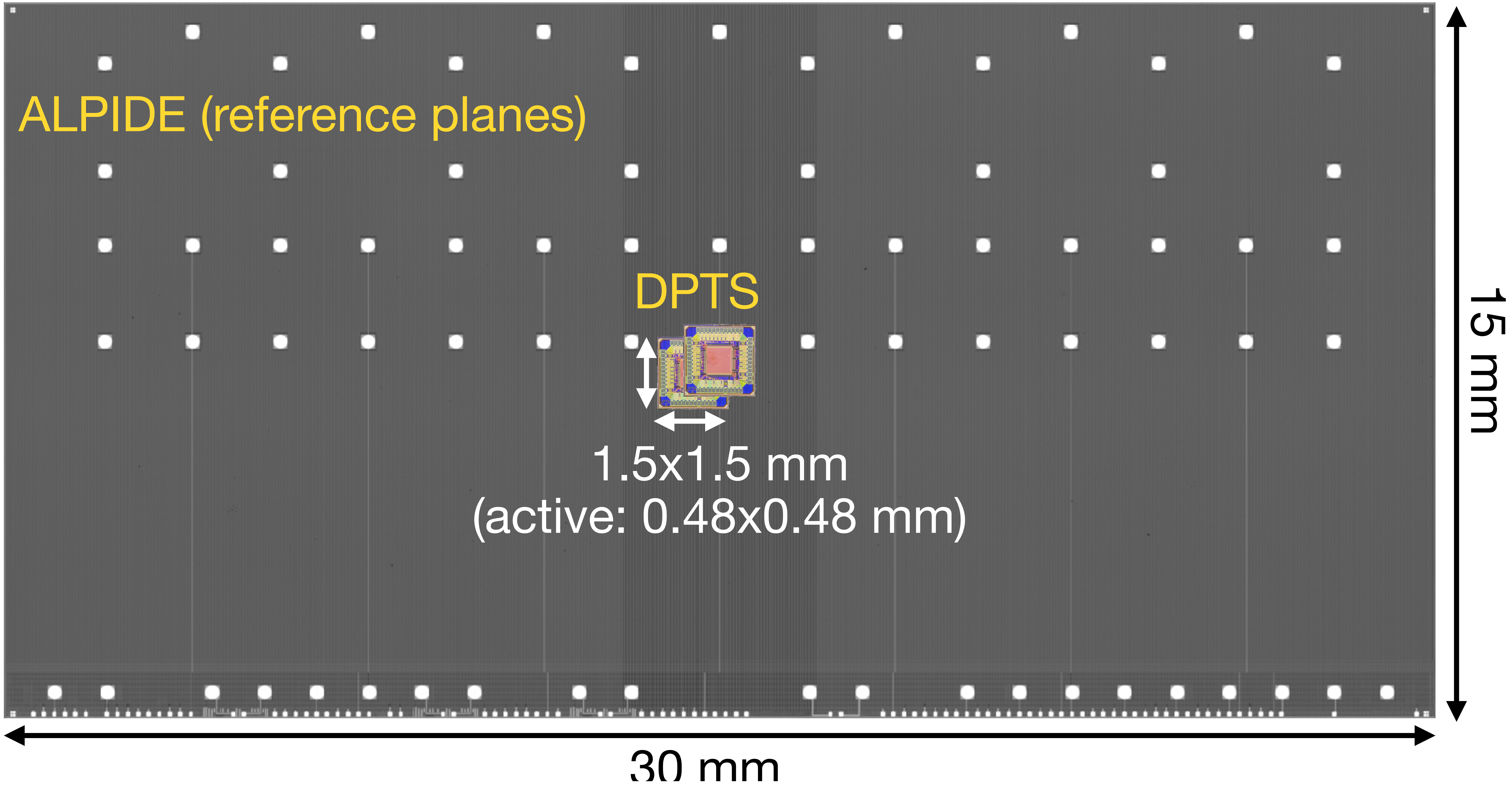


Schematic setup



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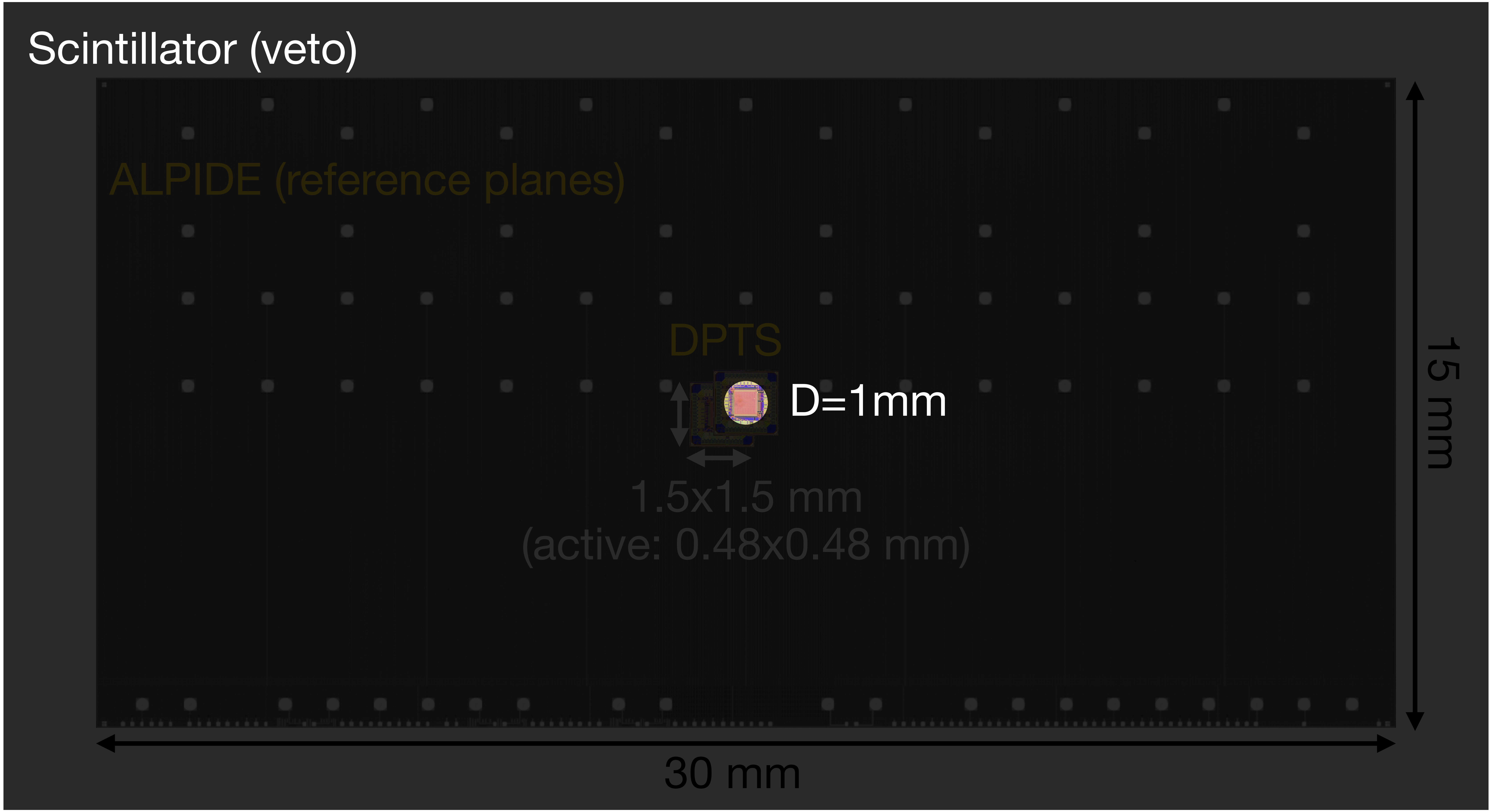


Scintillator (veto)

ALPIDE (reference planes)

DPTS

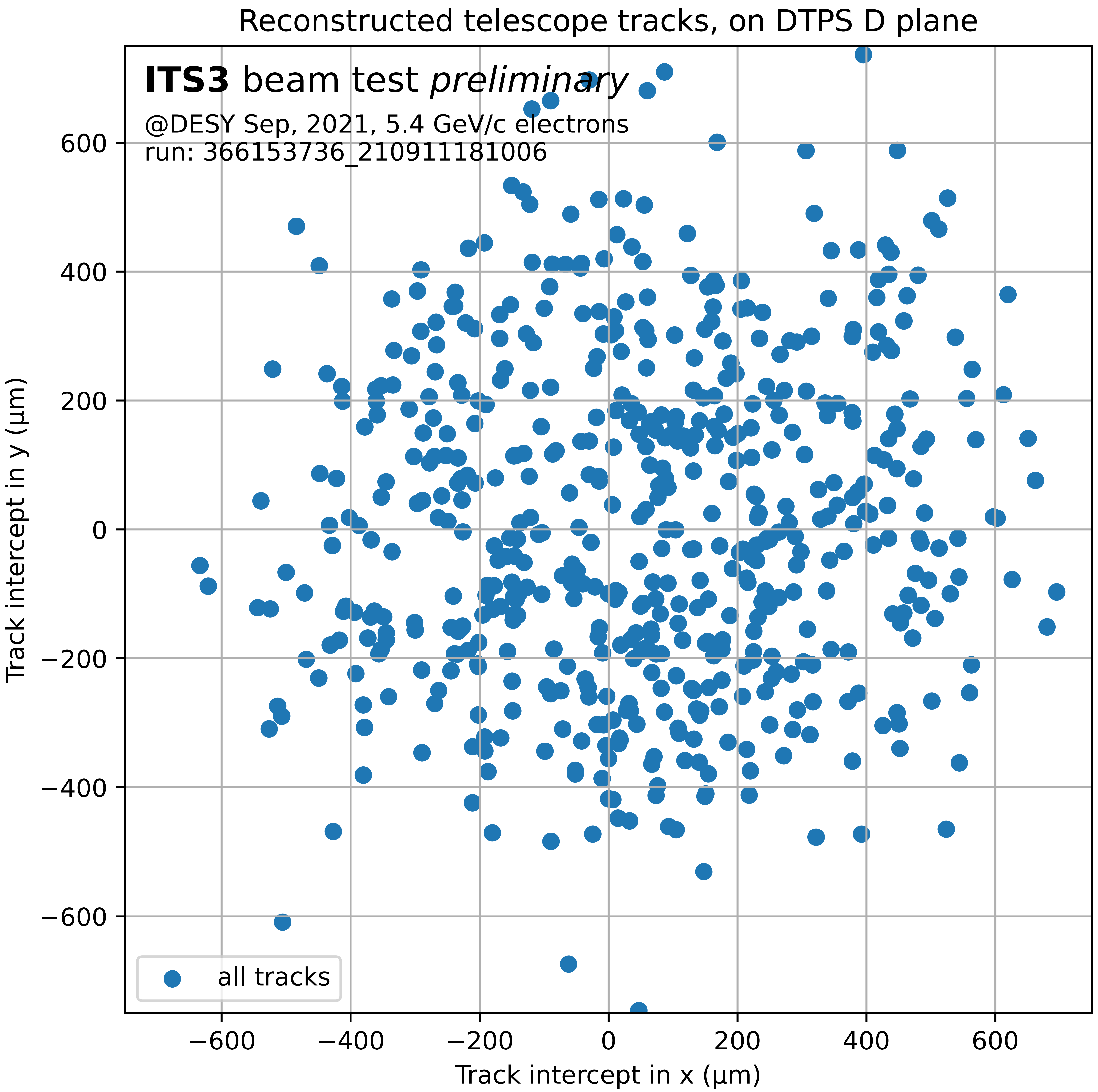
D=1mm

1.5x1.5 mm
(active: 0.48x0.48 mm)

15 mm

30 mm

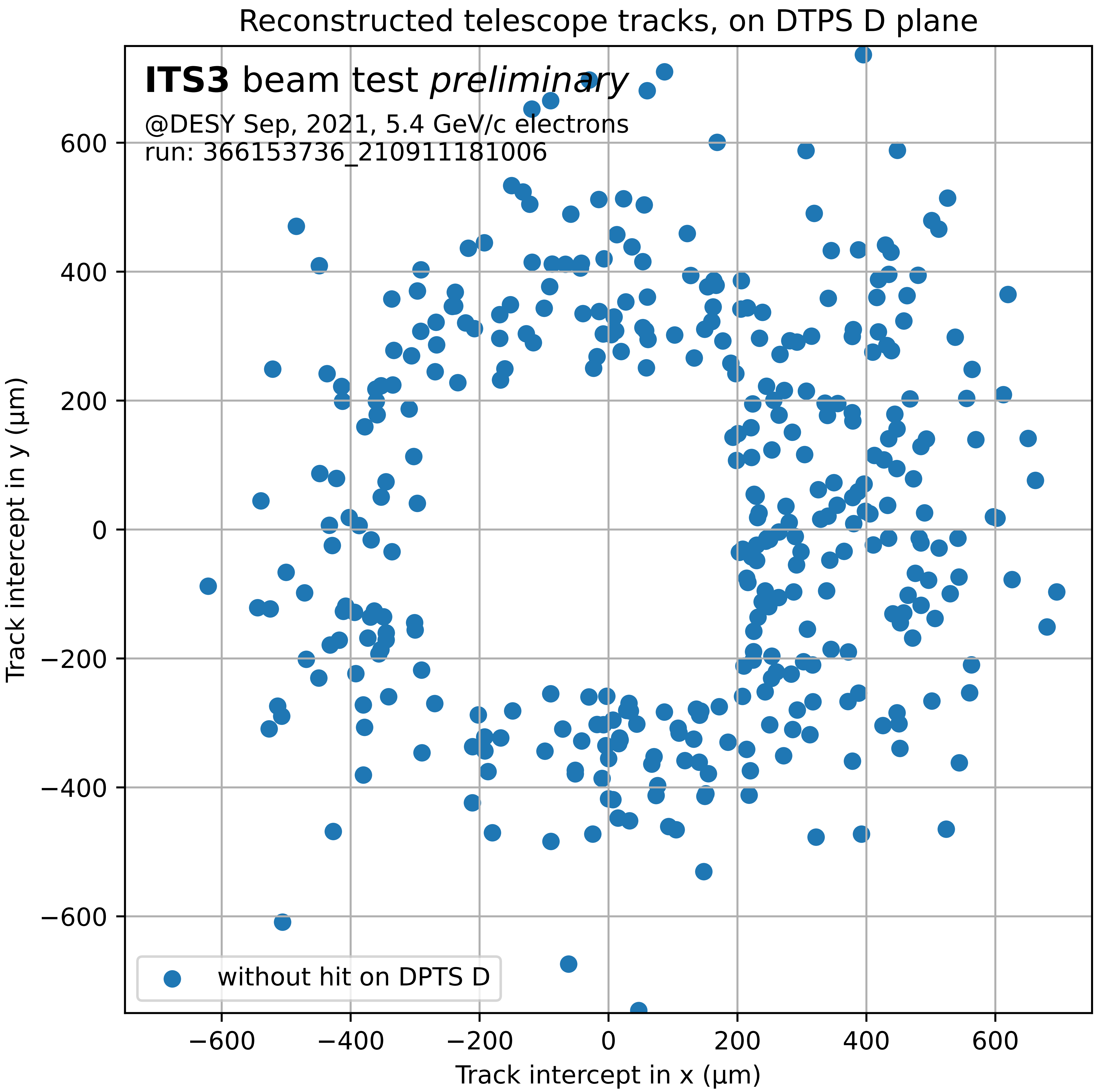
DPTS beam test results



first few % of total statistics analysed

- Beam spot and trigger tuned to illuminate a small area

DPTS beam test results

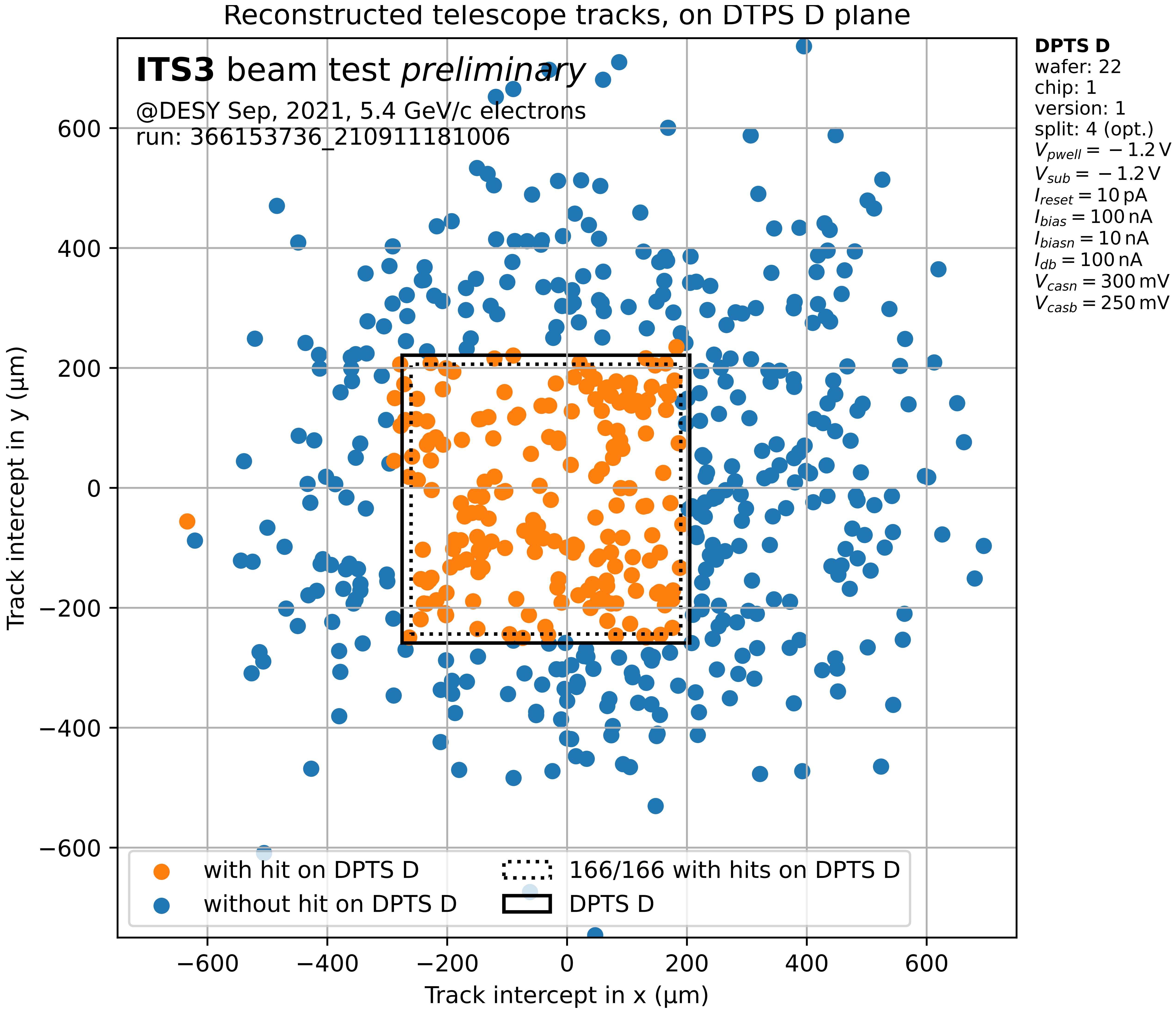


DPTS D
wafer: 22
chip: 1
version: 1
split: 4 (opt.)
$V_{pwell} = -1.2\,\mathrm{V}$
$V_{sub} = -1.2\,\mathrm{V}$
$I_{reset} = 10\,\mathrm{pA}$
$I_{bias} = 100\,\mathrm{nA}$
$I_{biasn} = 10\,\mathrm{nA}$
$I_{db} = 100\,\mathrm{nA}$
$V_{casn} = 300\,\mathrm{mV}$
$V_{casb} = 250\,\mathrm{mV}$

- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen

first few % of total statistics analysed

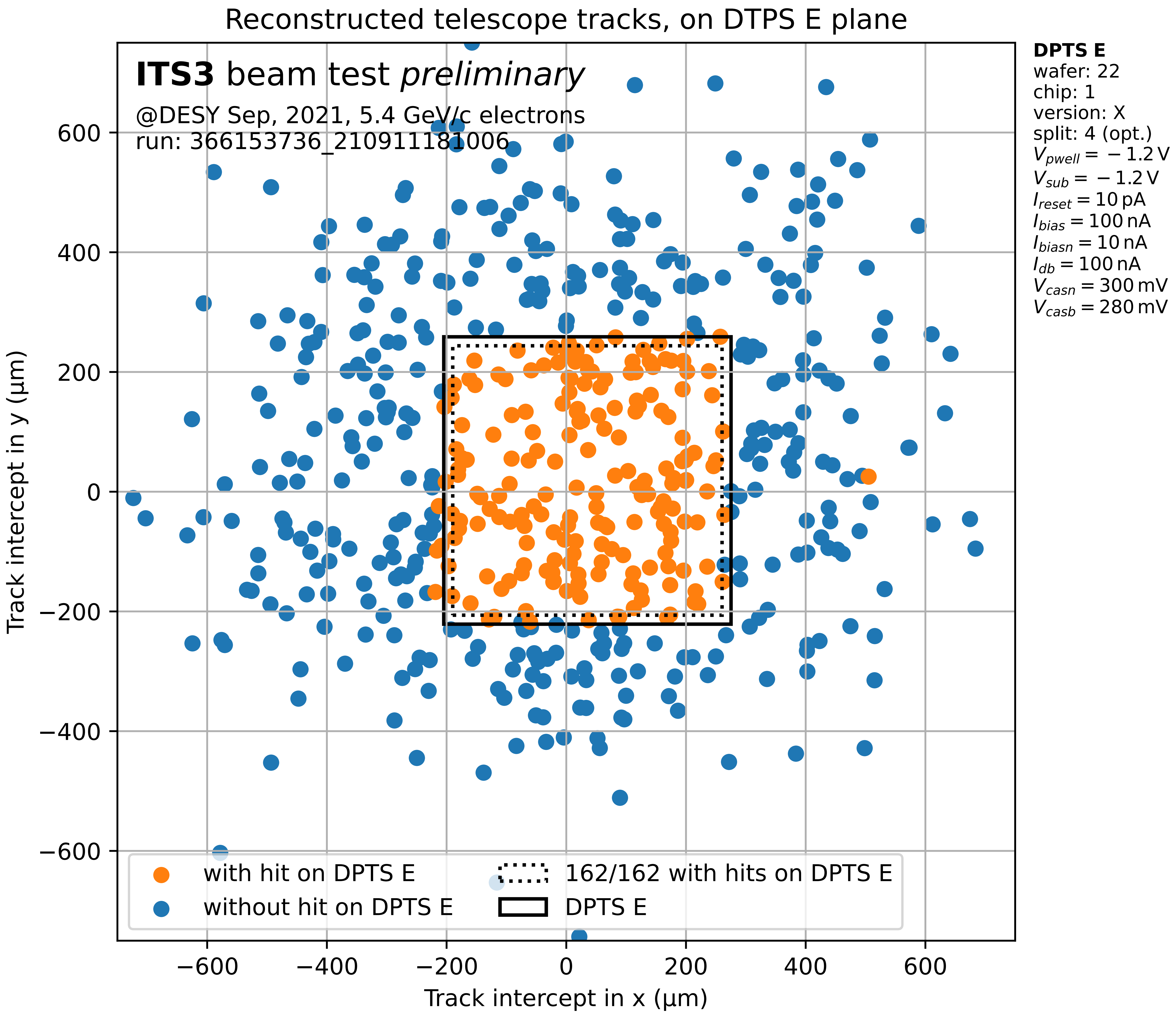
DPTS beam test results



first few % of total statistics analysed

- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen
- The area matches precisely the DPTS
- **166/166** tracks in region of interest

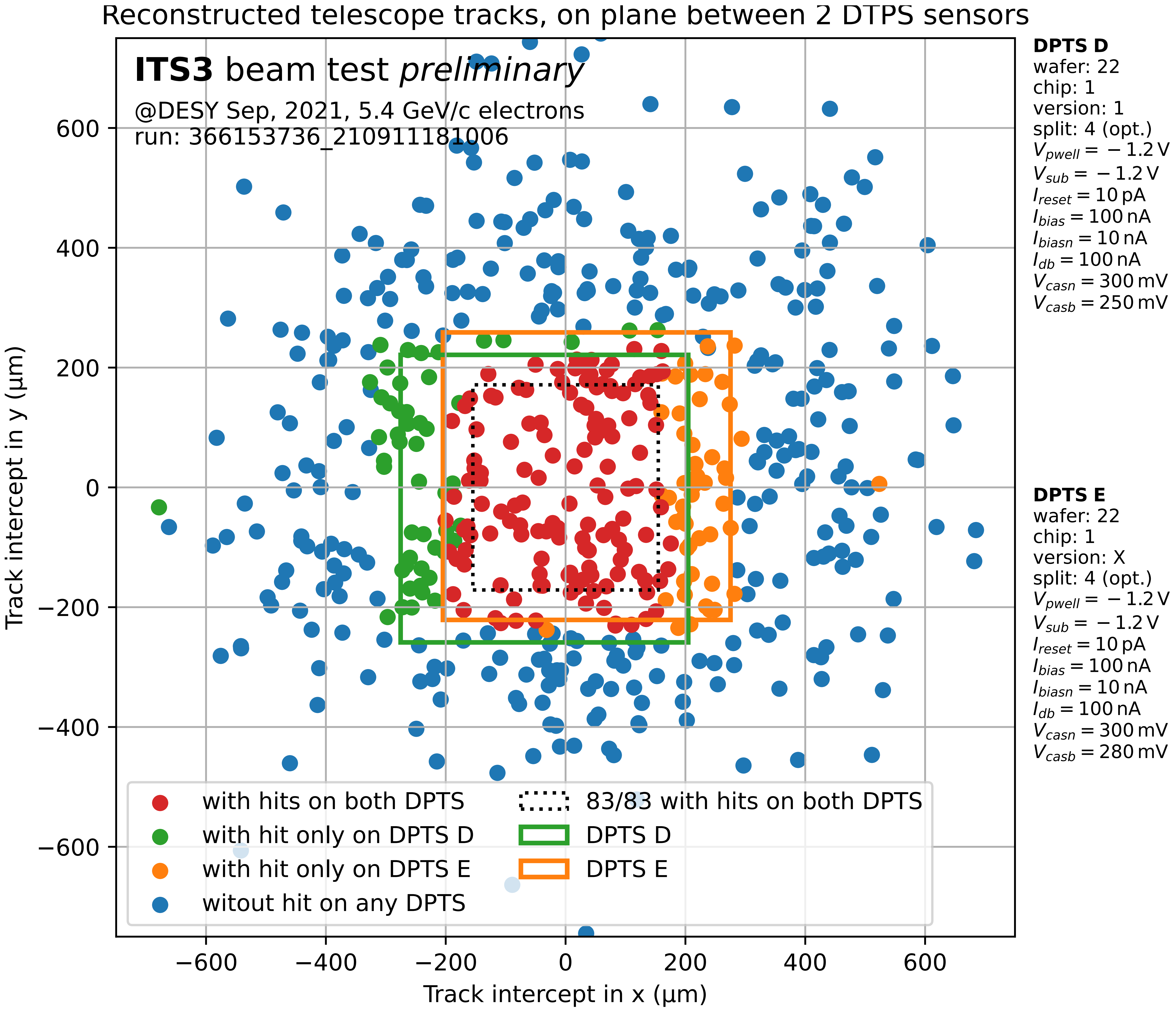
DPTS beam test results



first few % of total statistics analysed

- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen
- The area matches precisely the DPTS
- **166/166** tracks in region of interest
  - similar for second chip **(162/162)**

DPTS beam test results



Reconstructed telescope tracks, on plane between 2 DTPS sensors

DPTS D
wafer: 22
chip: 1
version: 1
split: 4 (opt.)
$V_{pwell} = -1.2\,V$
$V_{sub} = -1.2\,V$
$I_{reset} = 10\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 100\,nA$
$V_{casn} = 300\,mV$
$V_{casb} = 250\,mV$

DPTS E
wafer: 22
chip: 1
version: X
split: 4 (opt.)
$V_{pwell} = -1.2\,V$
$V_{sub} = -1.2\,V$
$I_{reset} = 10\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 100\,nA$
$V_{casn} = 300\,mV$
$V_{casb} = 280\,mV$

first few % of total statistics analysed

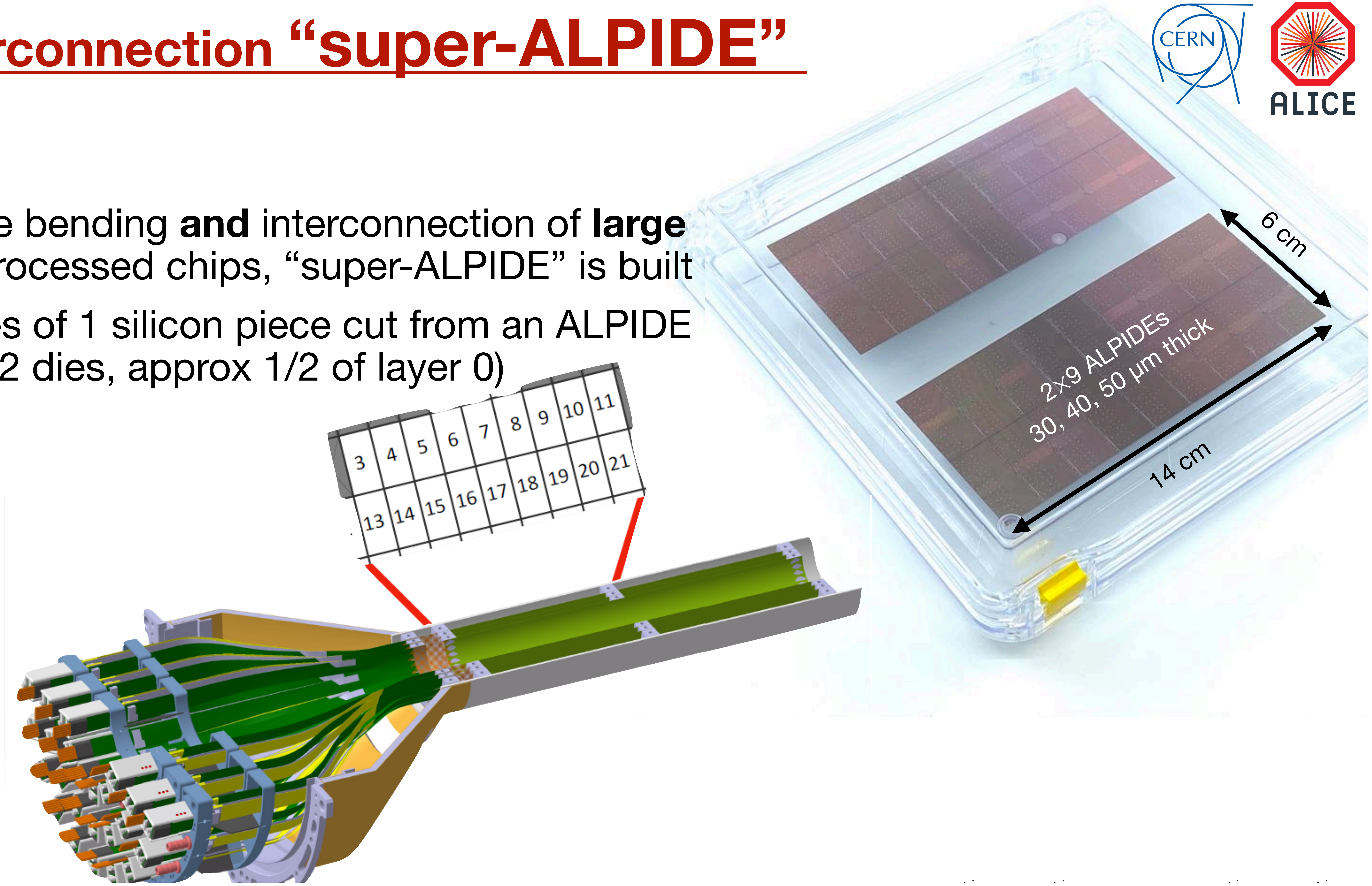
- Beam spot and trigger tuned to illuminate a small area
- Looking at tracks without hit in the DPTS, a clear 100% shadow is seen
- The area matches precisely the DPTS
- **166/166** tracks in region of interest
  - similar for second chip **(162/162)**
  - and even for both in coincidence **(83/83)**

Outlook

- Many parallel activities in progress.
- Test on APTS (analog pixel test structures): functional but noise issue in measurement setup.
- 2 more test beams for MLR1 in 2021:
  -CERN SPS 10-15 November
  -DESY 29 November – 6 December
- Shall start preparation of ER1 tests soon

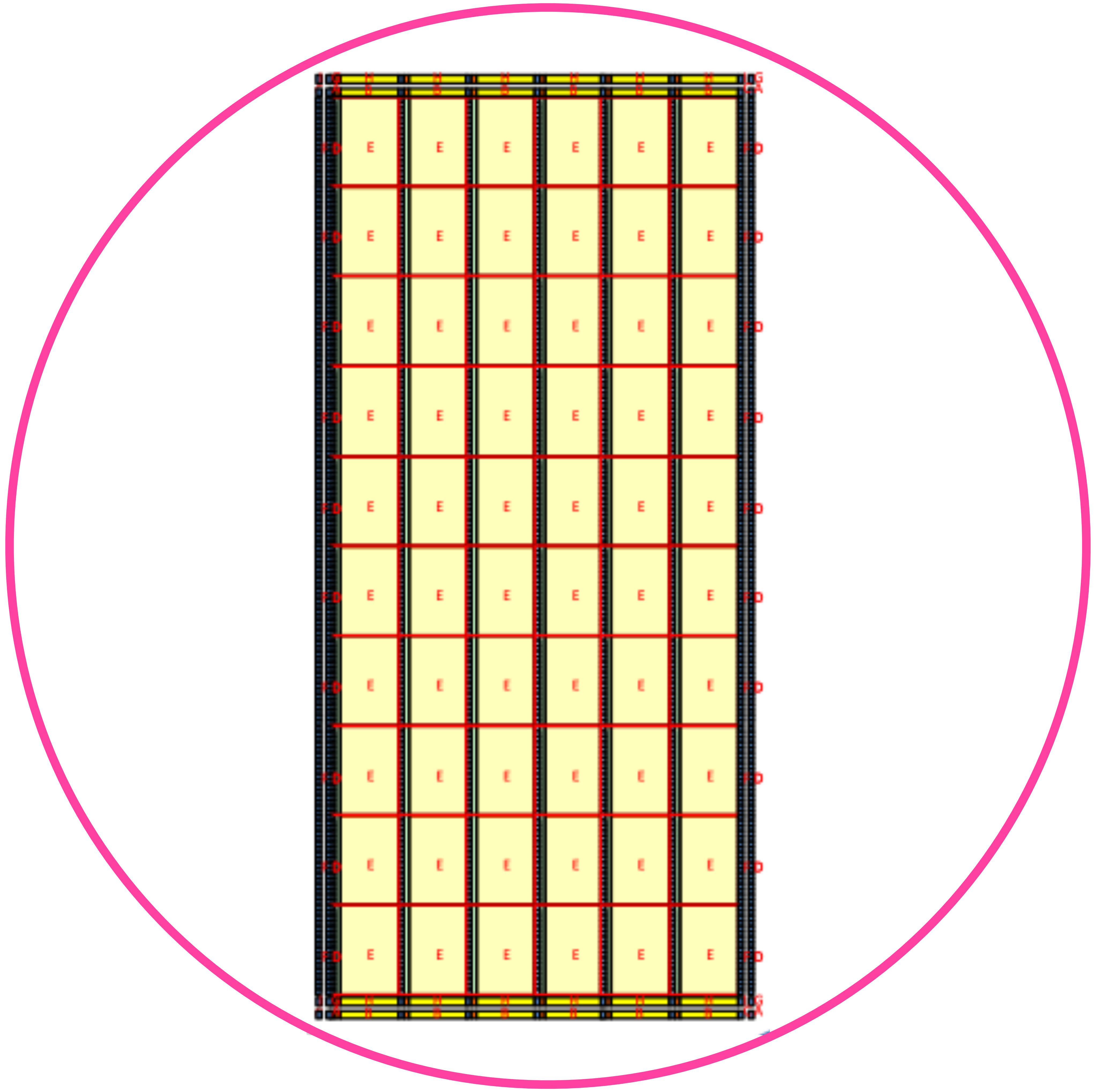
Layer interconnection “super-ALPIDE”

- To study the bending **and** interconnection of **large** pieces of processed chips, “super-ALPIDE” is built
  - comprises of 1 silicon piece cut from an ALPIDE wafer (9x2 dies, approx 1/2 of layer 0)

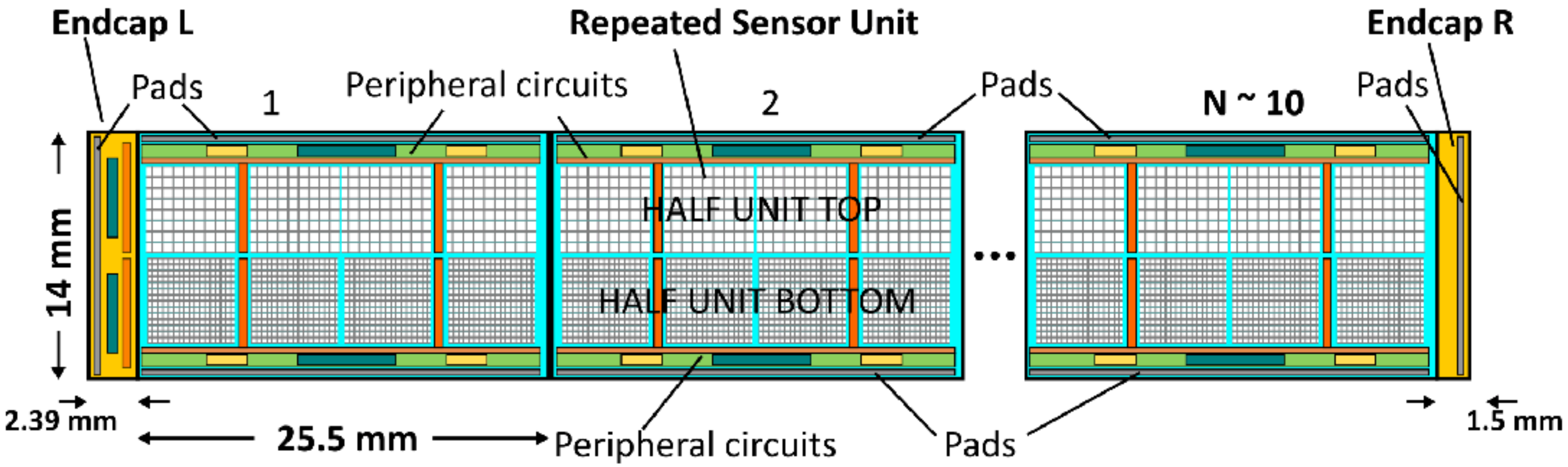


Towards a wafer-scale sensor

ER1



- Next big milestone in sensor design: **stitching**
- Design activity at full swing
  - building blocks are defined and work is distributed
  - builds on very encouraging, **silicon-proven**, feedback from MLR1



Last crucial ingredient for the TDR

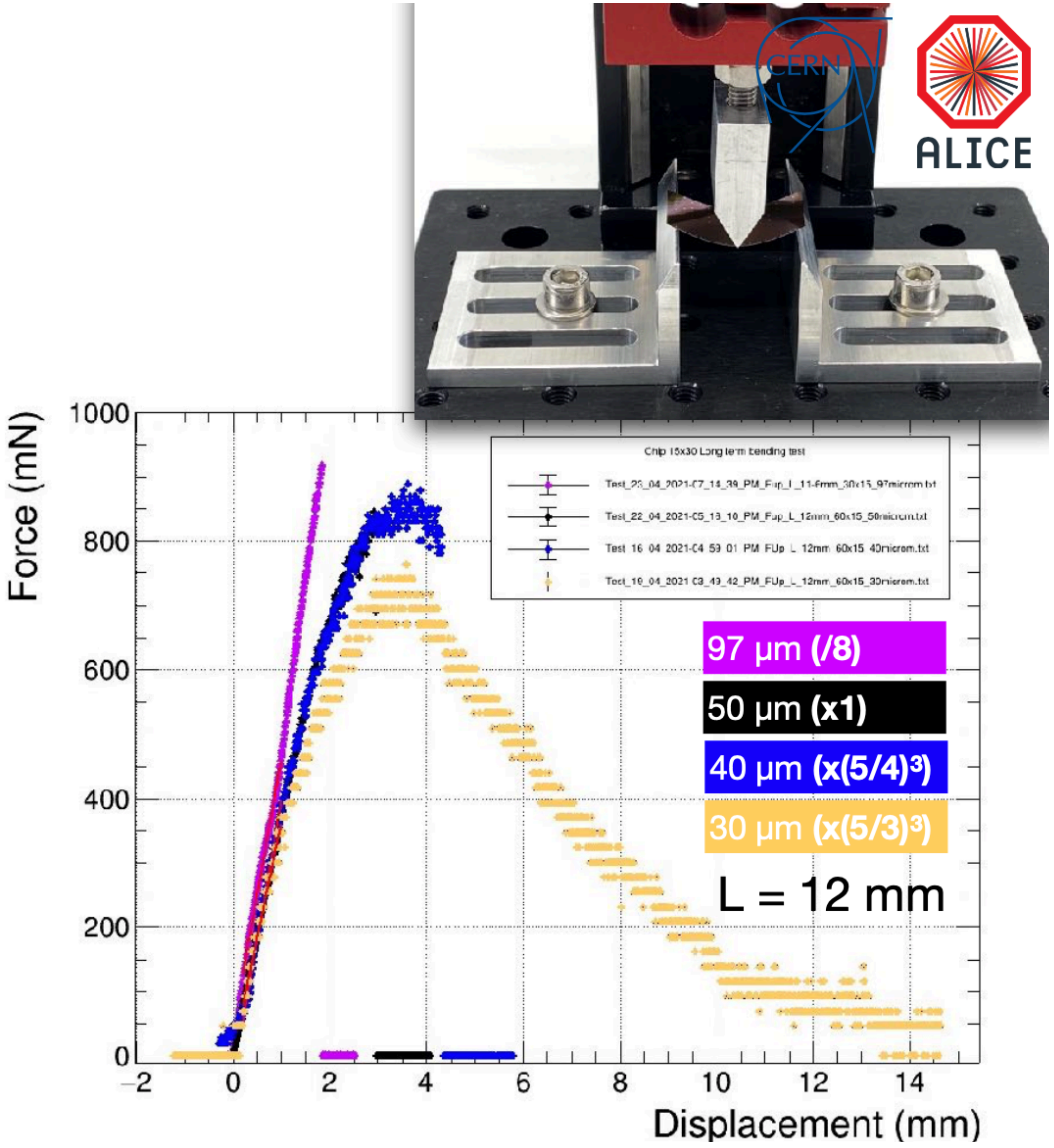
Chips for ER1: to be updated and mapped into floorplan

Design	Purpose	Institute	# of test sites	Comments
MOSS	stitched sensor prototype develop stitching know-how, more conservative Focus on technology options, power distribution, signal routing, yield	INFN, IPHC, NIKHEF, CERN	-	1D stitching Matrix as simple as possible
MOST	Stitched sensor prototype, develop stitching know-how, more aggressive Study yield with high density layout parts and fine power segmentaton Low power and transmission of timing information over long distance	NIKHEF, IPHC, Heidelberg, CERN, INFN	-	Many parts in common with MOSS
H2M	Hybrid to Monolithic Investigate MAPS and architectures in non-stitched sensor	DESY and CERN	2	
CE65++	Pixel optimization vehicle Focus on optimizing pixels and front-end	IPHC	tbd	
SEU chips	Prototype with memories and flops Measure SEE cross-sections (SEL, SEU)	INFN Bari	2	
PLL NIKHEF	First step in high speed transmitter	NIKHEF	1	High speed transmission
PLL+buffer	First step in high speed transmitter	RAL	1	High speed transmission
Pixel test DESY	Pixel sensor and front end prototype	DESY	1	
Pixel test SLAC	Pixel matrix prototype	SLAC	1	
APTS	Analog pixel test structure	IPHC and CERN	tbd	
DPTS	Digital pixel test structure	CERN	tbd	
TTS1-5	Transistor test structures	CERN	10	
ADC prototype	Desired function	not covered		generated from DAC ?
Supply regulation	Desired function	not covered		Interest from several corners

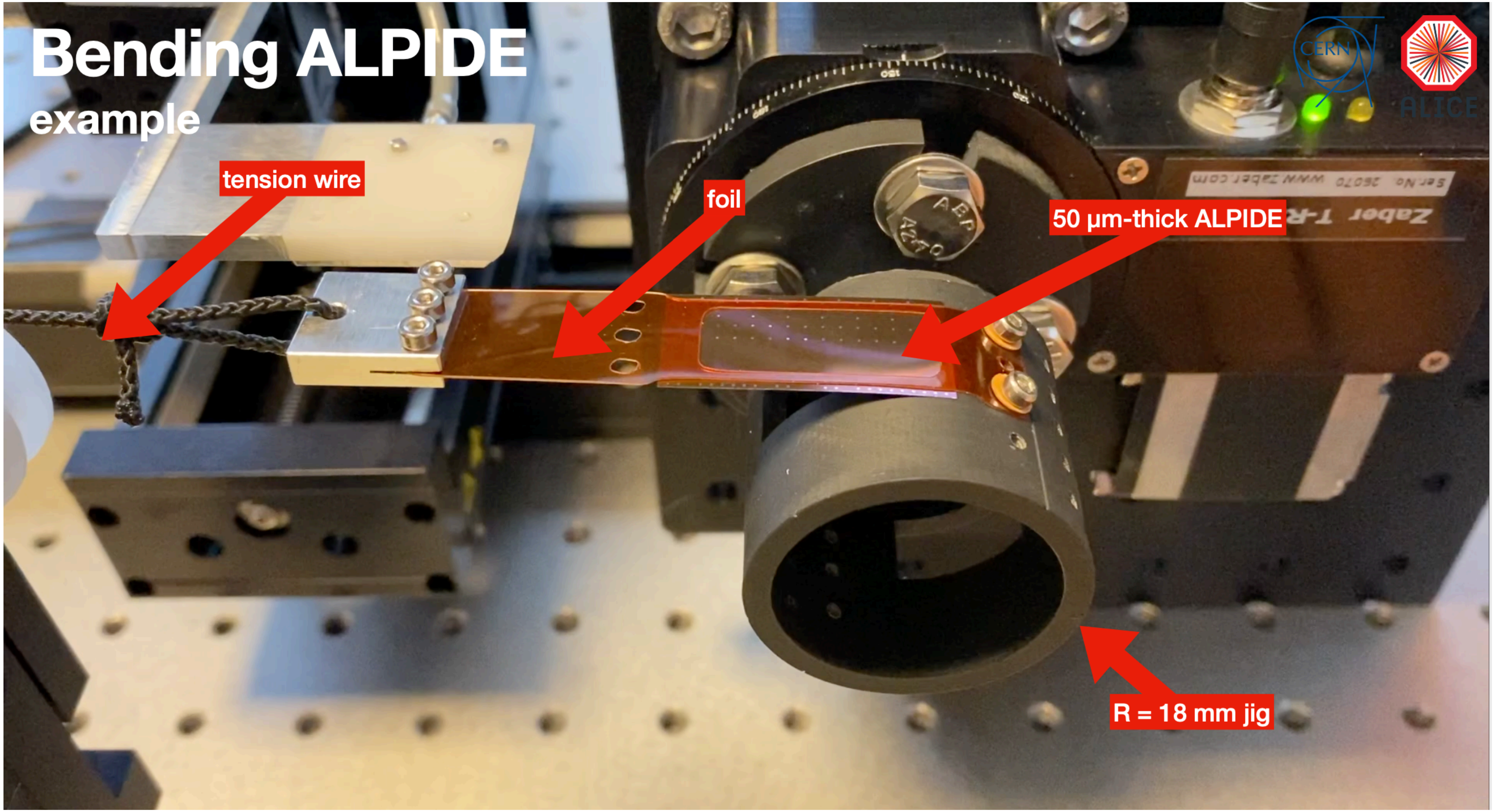
Backup

Mechanics and bending test

- **Monolithic** Active Pixel Sensors are quite flexible
  - already at thicknesses that are used for current detectors
- Bending force scales as (thickness)$^{-3}$
  - large benefit from thinner sensors
- Breakage at smaller radii for thinner chips
  - again benefit from thinner sensors
- **Our target values are very feasible!**

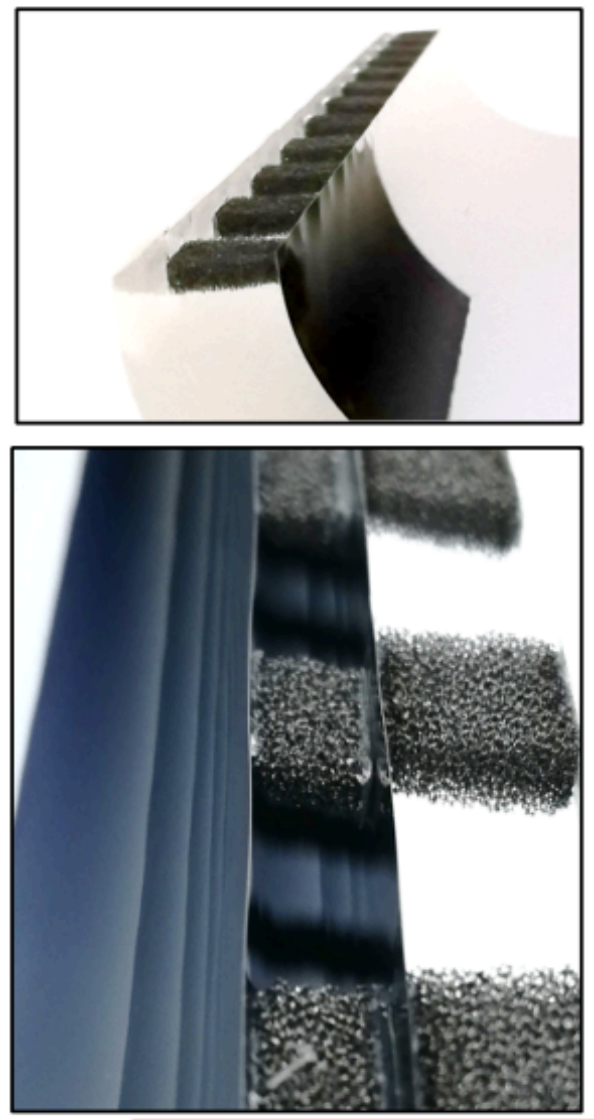


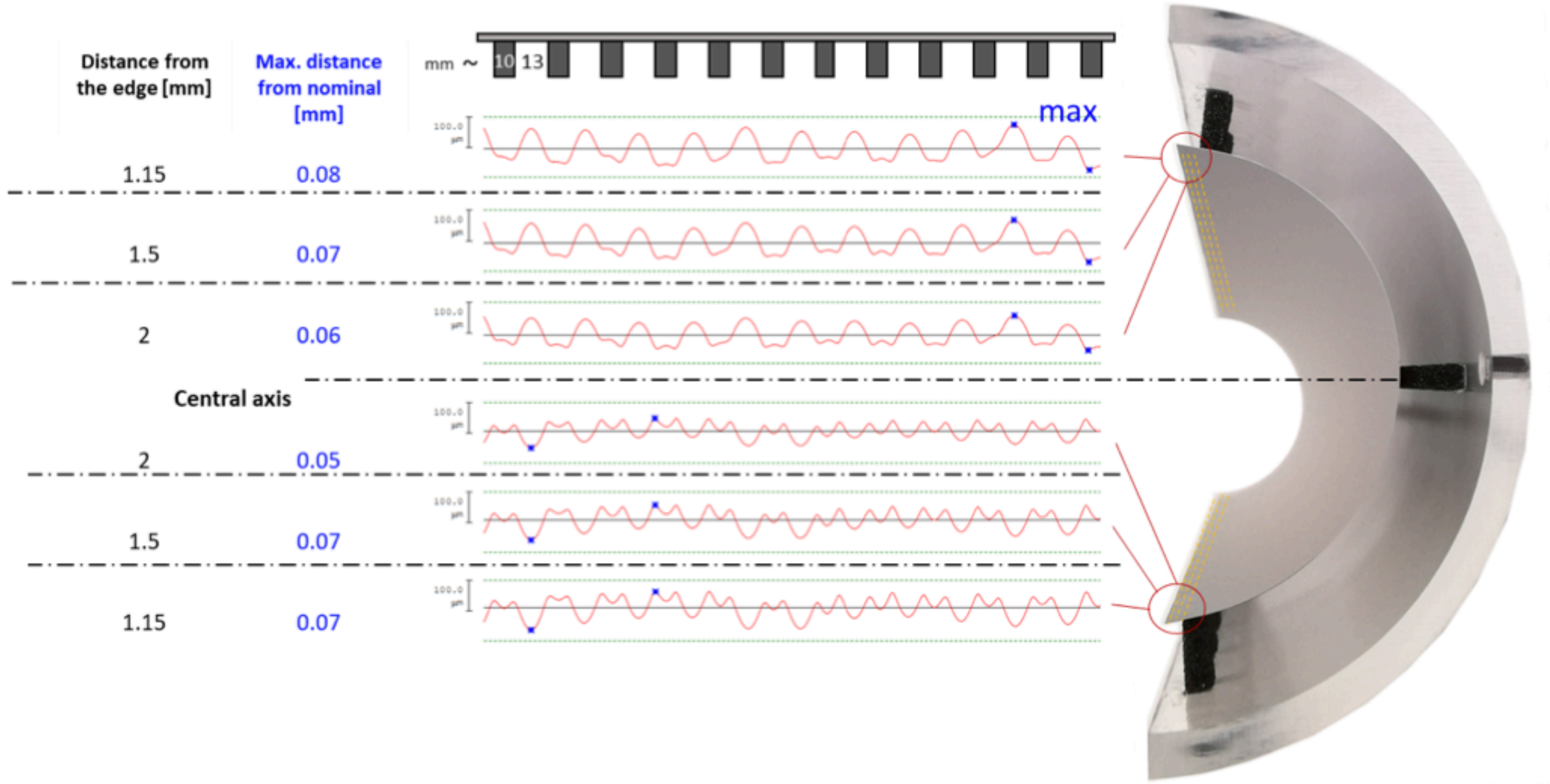
Mechanics and bending test



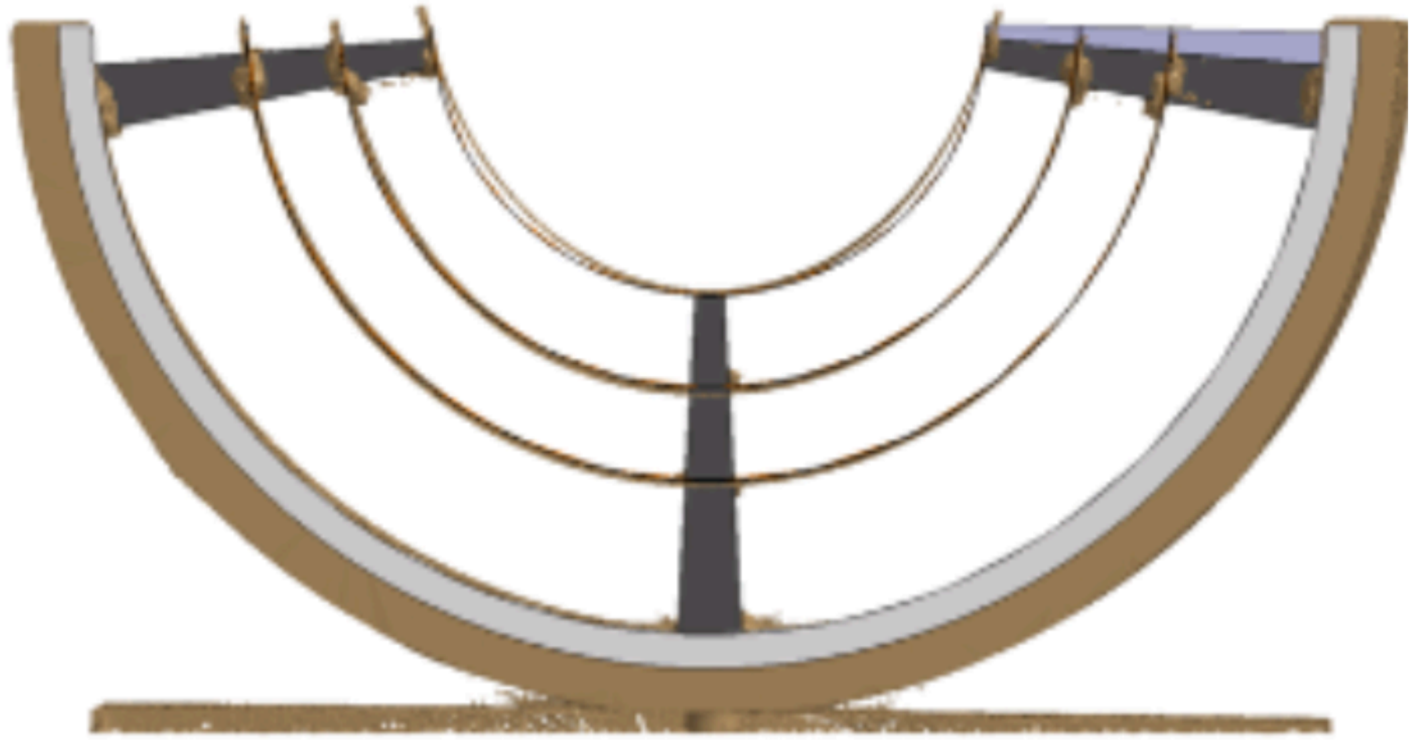
Assembly test

- Detailed analysis of the impact of the carbon foam support wedges
  - local deformations of <100 μm
- 3D X-ray of the full assembly: very good agreement





Distance from the edge [mm]	Max. distance from nominal [mm]
1.15	0.08
1.5	0.07
2	0.06
Central axis	
2	0.05
1.5	0.07
1.15	0.07

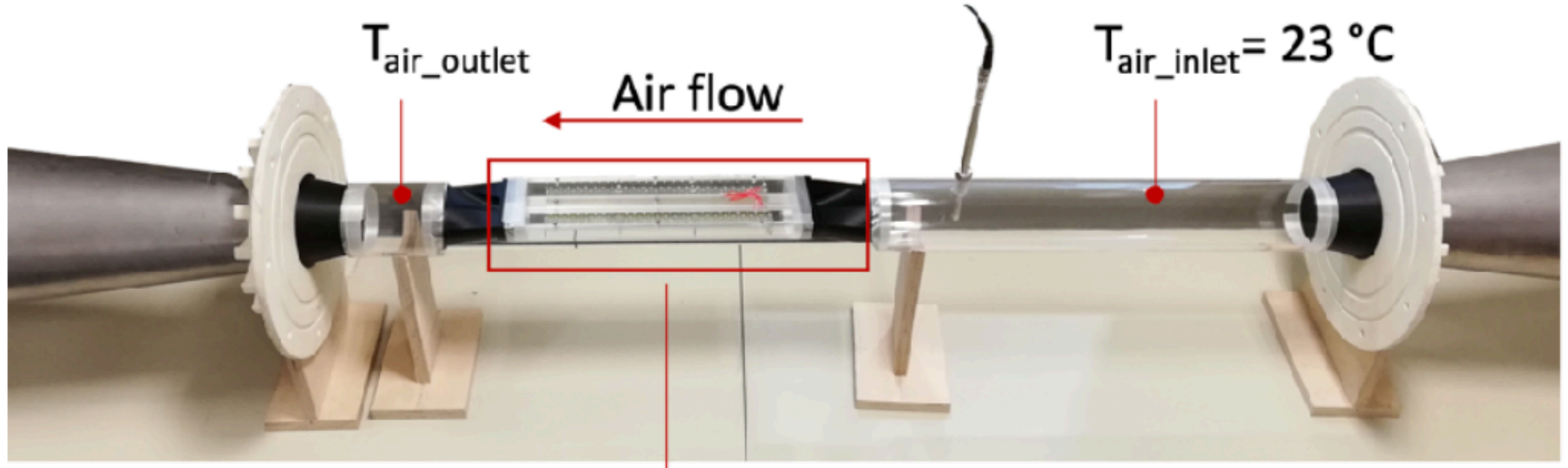


Tomography VS CAD model

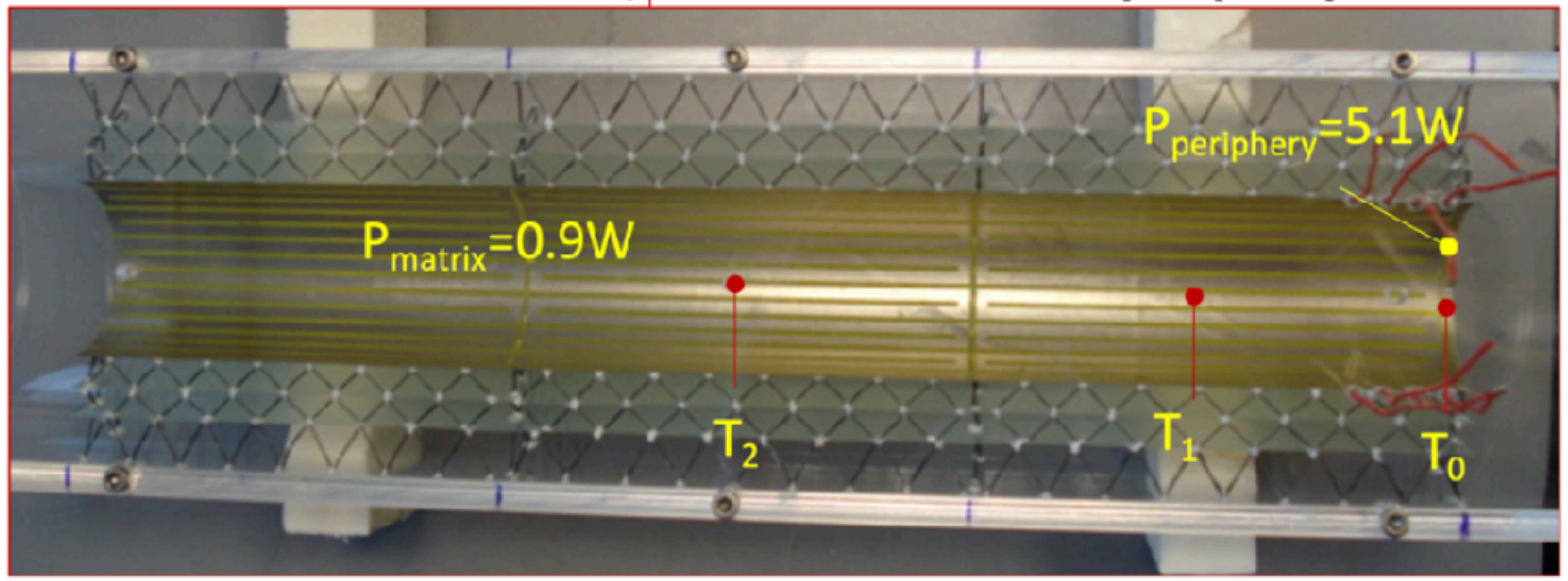
Very good results, details to be added to MC

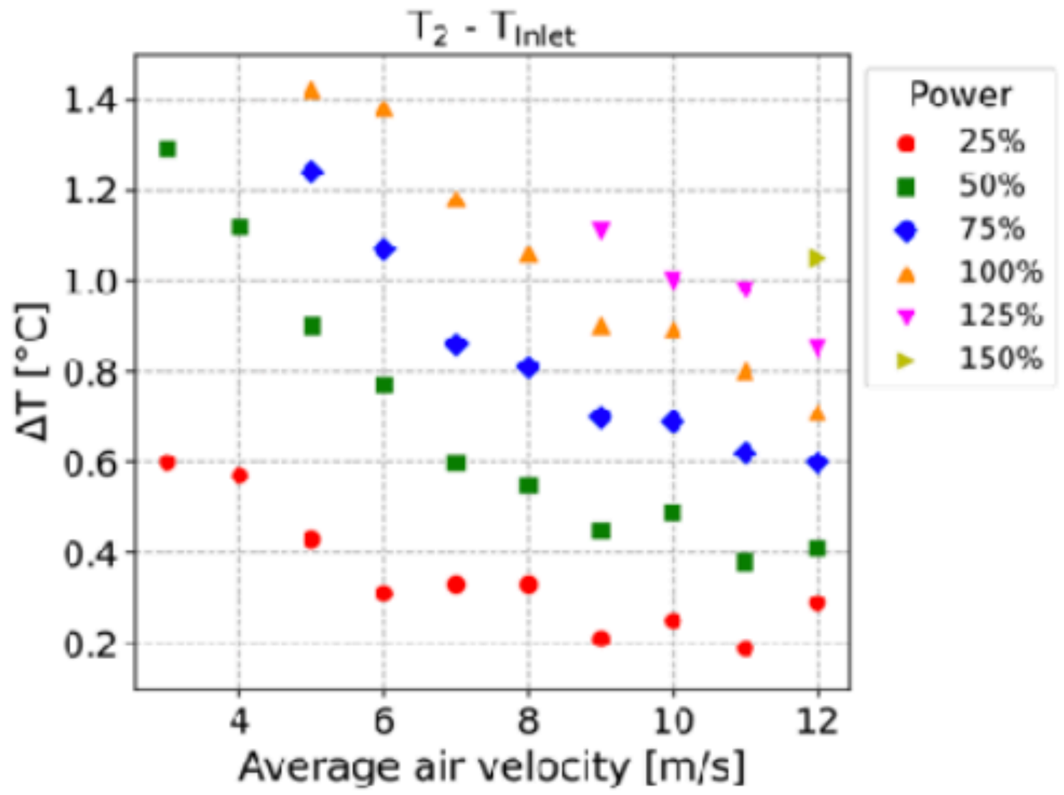
Assembly test : Cooling

- Preliminary test has been performed for a Breadboard model equipped with heaters to simulate heat in the layer 0, no carbon foam

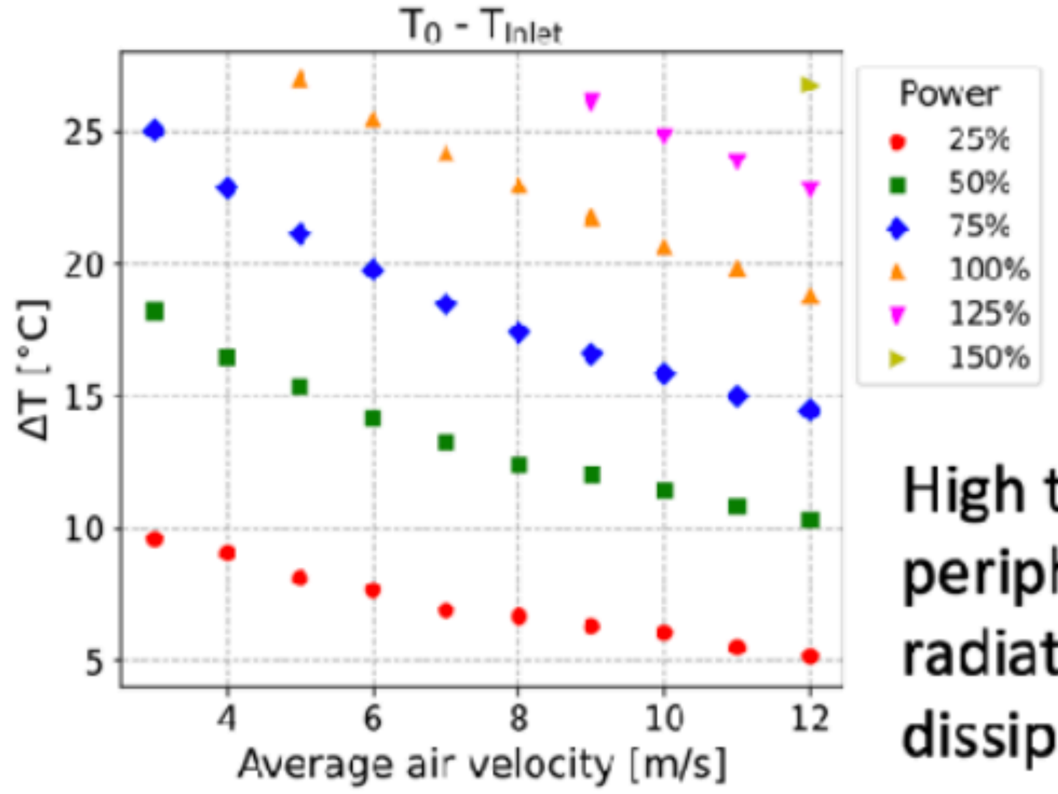


Breadboard model, no radiators at the periphery





Nominal power (100%)
Periphery= 5.1W
Matrix=0.9W



Similar results reversing the air flow direction

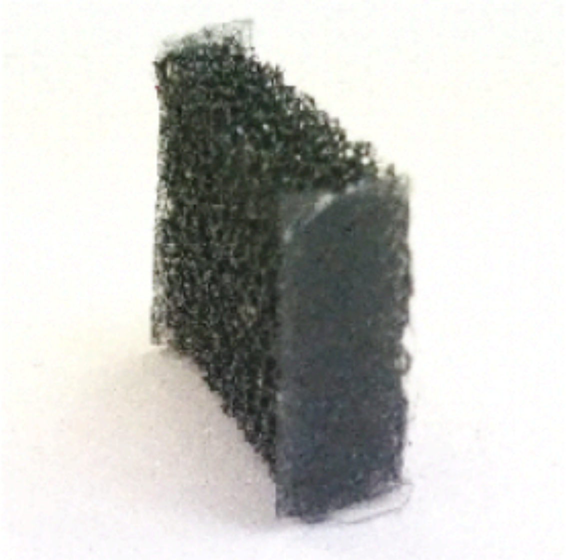
High temperature at the sensor periphery confirm the need of a radiator (carbon foam ring) to dissipate the heat

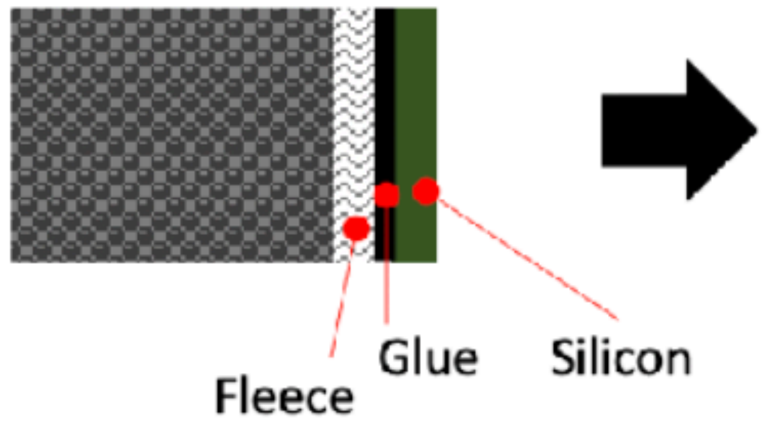
Very important input for the further design optimisation

Assembly test: Optimization of glueing

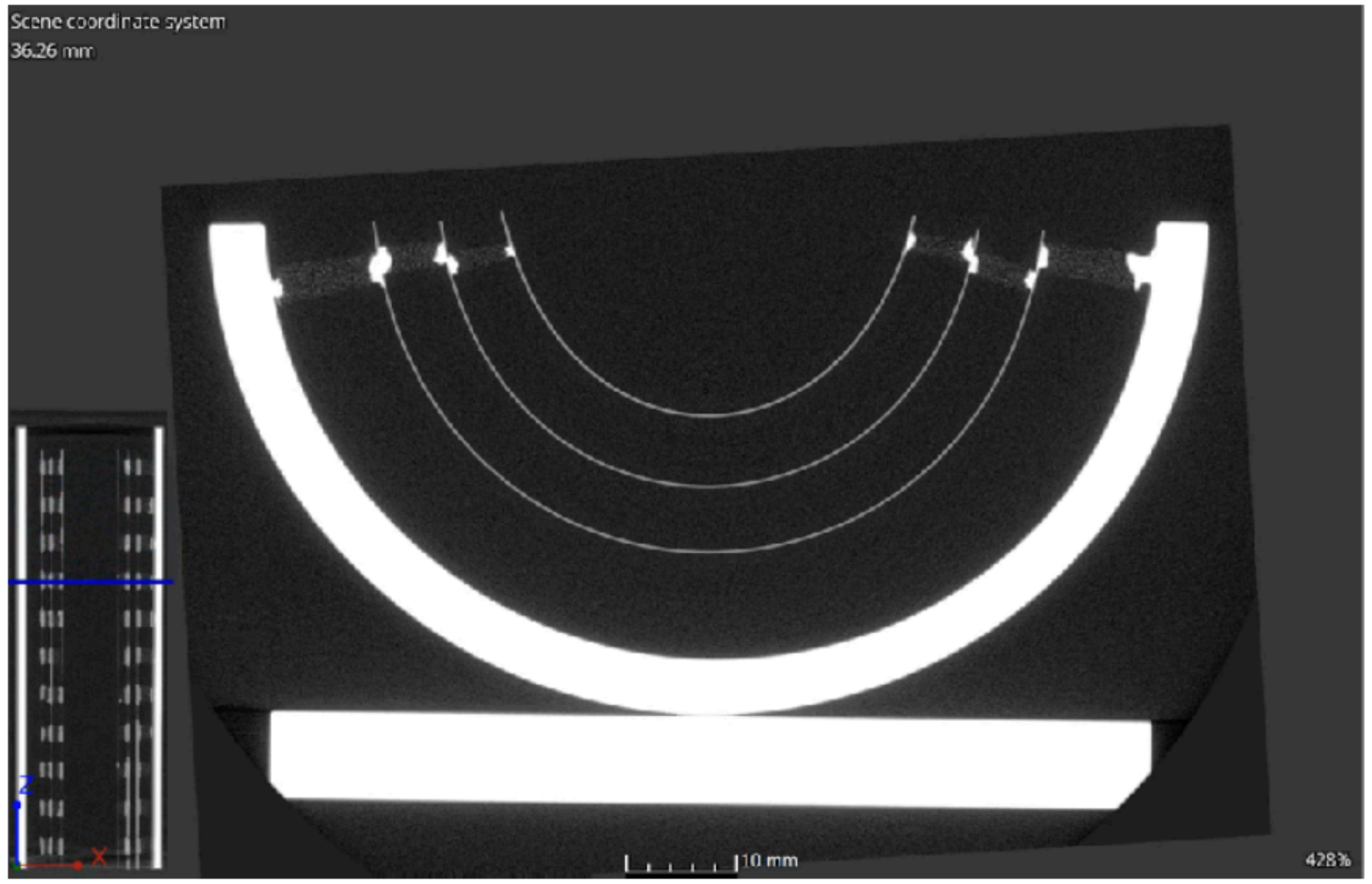
Carbon foam wedge:
ERG Duocel
[0.06 kg/dm^3]
Carbon fleece
[8g/m^2]

Glue: Araldite 2011



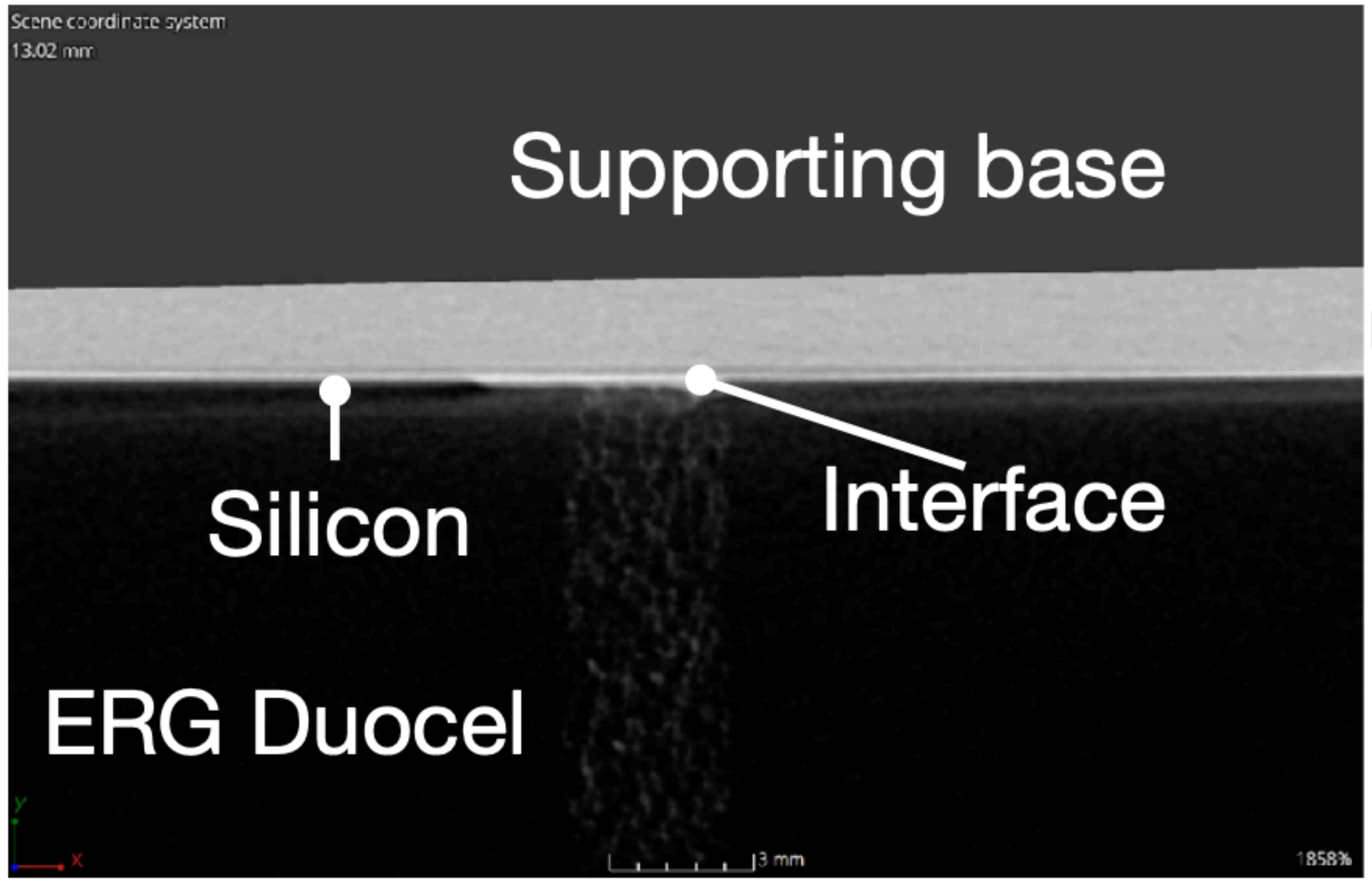


First assembly has shown glue penetration in the carbon foam by capillarity



Pre-curing steps of fleece + glue

To minimise glue penetration



Helps to really put the material budget down as much as possible