U.S. MAGNET DEVELOPMENT PROGRAM

# General MDP Meeting Instrumentation


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2021

| Milestone # | Description | Target |
|---|---|---|
| AIIId-M1 | Development of a new generation of self-calibrating acoustic emission diagnostics hardware | December 2020 |
| AIIId-M2 | Finalizing software algorithms for acoustic data analysis, completing analysis for the CCTs and 15T dipole | December 2020 |
| AIIId-M3 | Development and test of a linear quench localization sensor on a Bi-2212 subscale and/or ReBCO CCT series | March 2021 |
| **AIIId-M4** | Test of a large-scale Hall array and imaging current distribution in HTS tape stacks and coils | May 2021 |
| AIIId-M5 | Completing spot heater studies to improve voltage-based diagnostics and address "silent" quenches | July 2021 |
| AIIId-M6 | Demonstration of inverse acoustics-based probing of interfaces in a dedicated small-scale coil | September 2021 |
| AIIId-M7 | Development of multi-element and flexible quench antennas and localization of quenches in using flexible quench antenna arrays | September 2021 |
| AIIId-M8 | Characterization of training-like behavior in different impregnation materials under load using a Transverse Pressure Insert (TPI) measurement system | December 2021 |
| AIIId-M9 | Development and test of a standalone acoustic quench detection and localization FPGA-based system | December 2021 |
| **AIIId-M10** | Development and test of a non-rotating new magnetic probe prototype | December 2021 |
| **AIIId-M11** | Demonstration of a programmable fully-cryogenic FPGA "smart" sensor core with digital readout and analog front-end (SQUID) amplifiers | December 2021 |
| **AIIId-M12** | Calibration of FBG fibers in a small cryostat. Installation on an MDP magnet and strain measurement during a quench. Design a proof of principle experiment for quench 3D spatial detection and coil azimuthal strain mapping and install fiber on MDP magnet. Use fibers for energy spectrum analysis and HTS quench detection. | December 2022 |

Maxim, Reed, Geon Seok (M1–M4)

Stoyan (M5)

Maxim (M6)

Joe, Stoyan, Reed (M7)

Emanuela (M8)

Maxim, Reed (M9)

Maxim, Joe (M10)

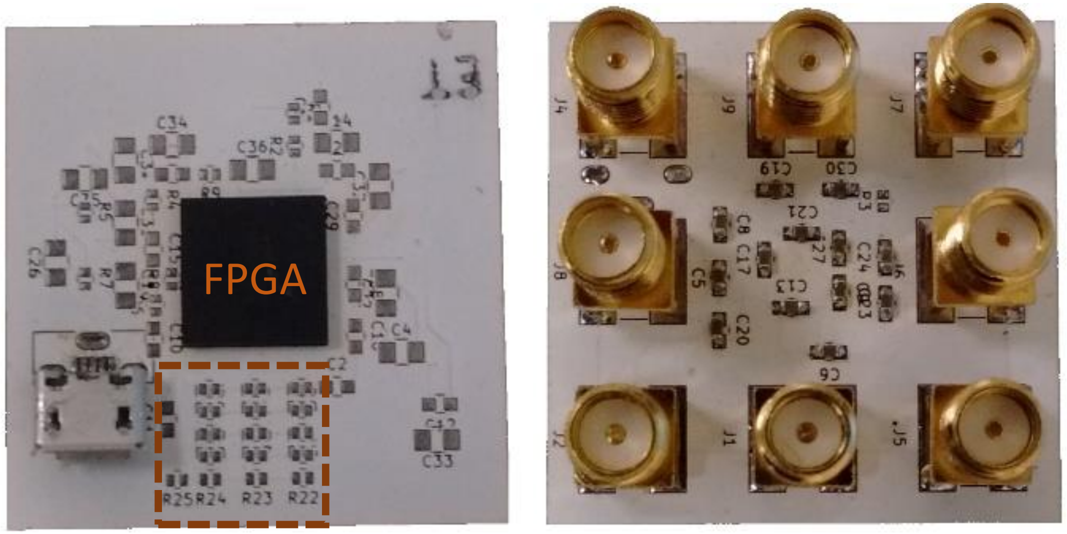
Marcos ← (M11)

Maria (M12)

# FPGA BOARD AND HYBRID FLASH FOLDING ADC

## Cryo FPGA Implementation version 1

JTAG

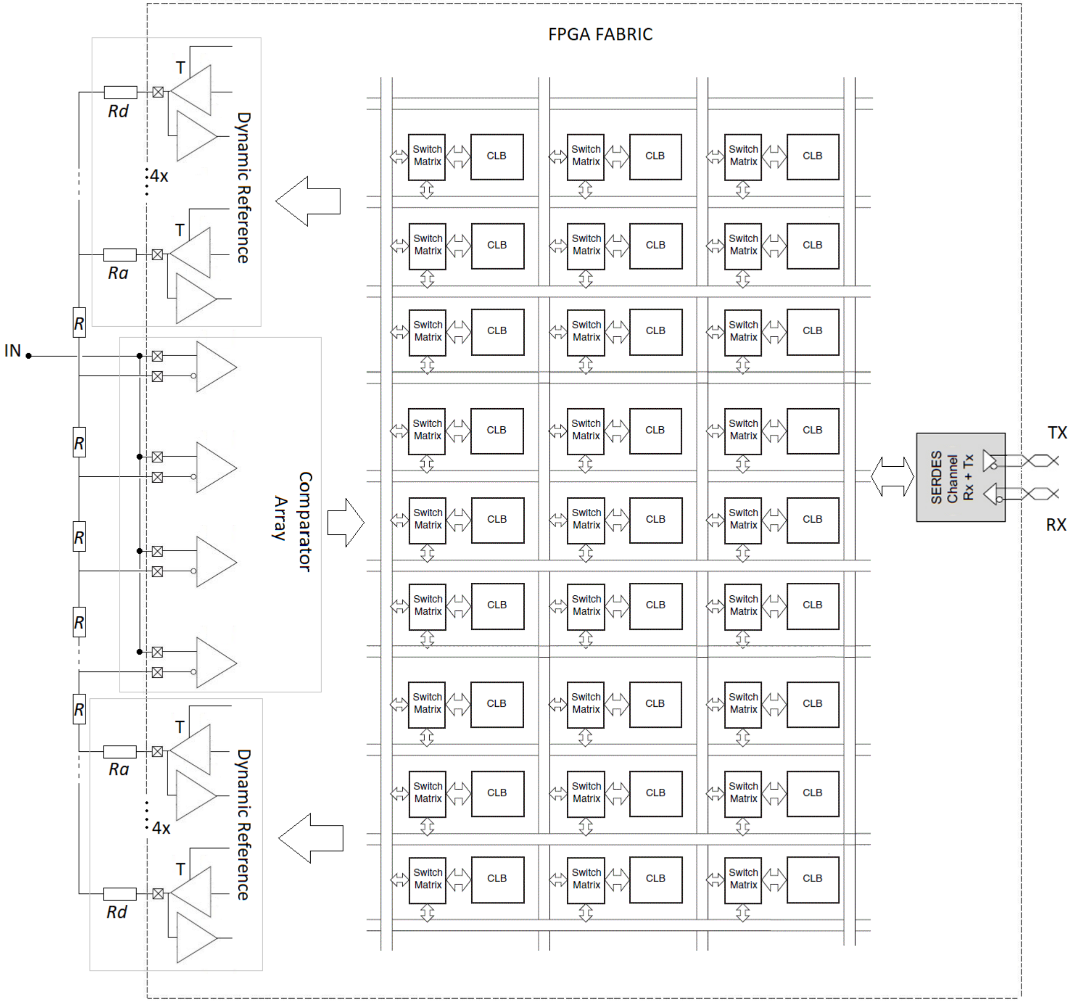



### Resistor Array:

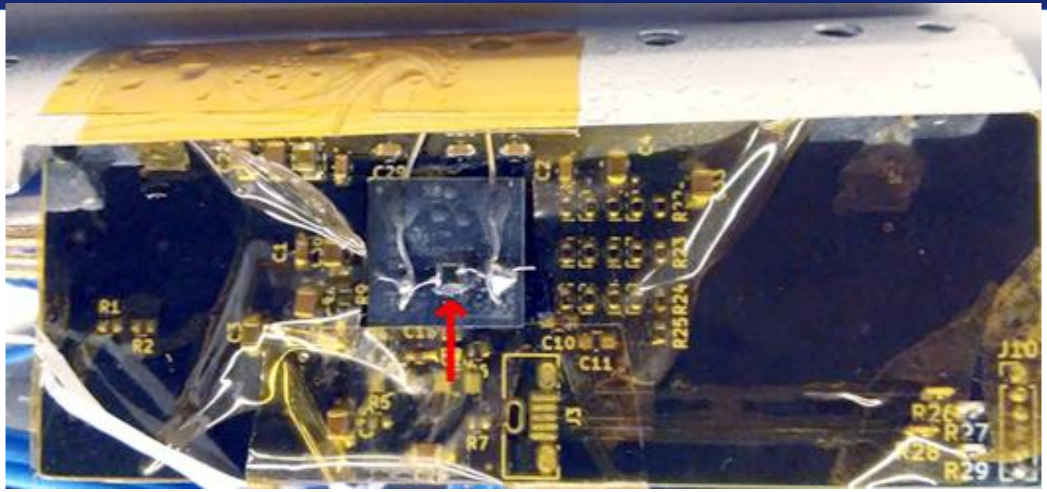
- Connected to FPGA differential buffers
- ADC built in 1MSPS, 12b
- Uses FPGA bank reference

### SMA interface:

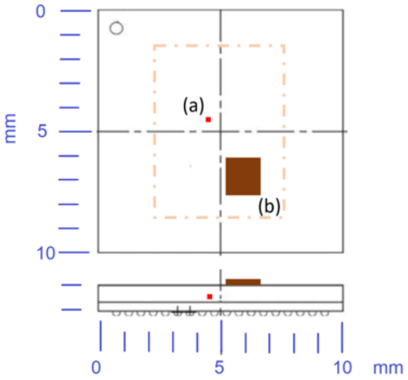
- Power (Core and I/O)
- Analog In
- Digital In
- Digital Out



# TEST STAND AND TEMPERATURE MONITORING



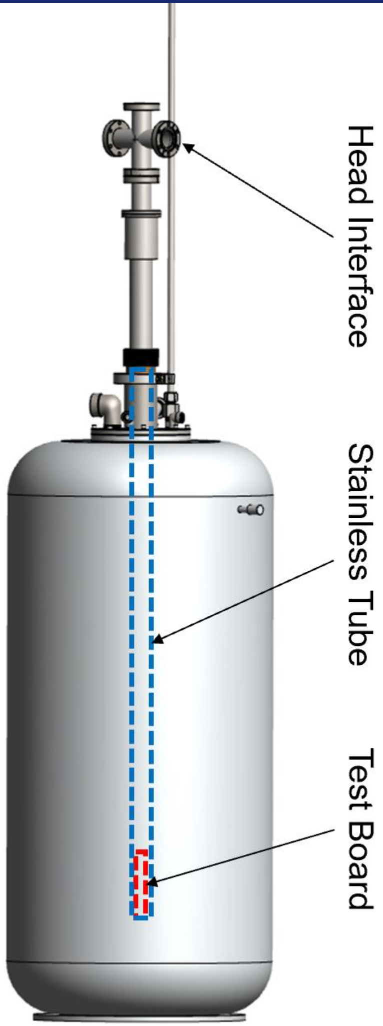
The RuO  thermometer indicated by the red arrow glued on top of the FPGA (shown with an arrow)

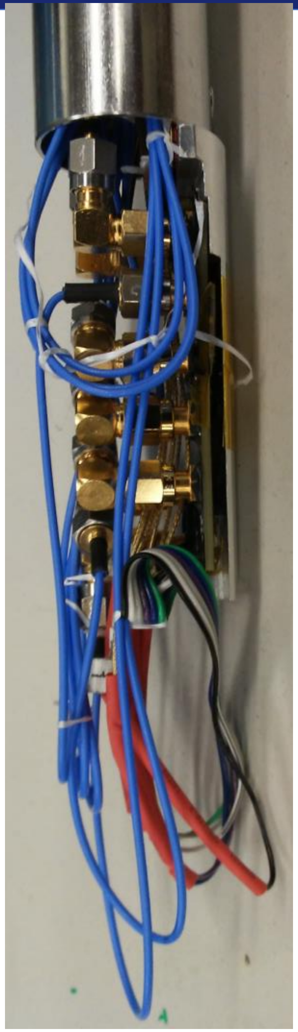



(a) Internal Thermometer

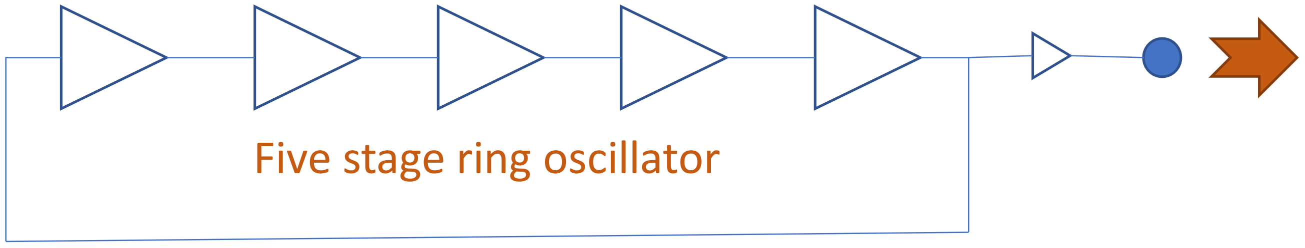
(b) RuO Thermometer

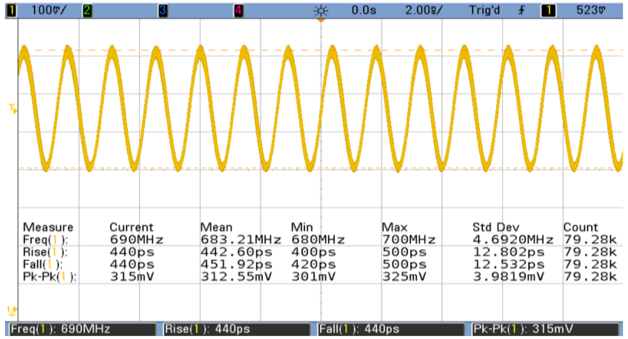
Maxim and Bleximo

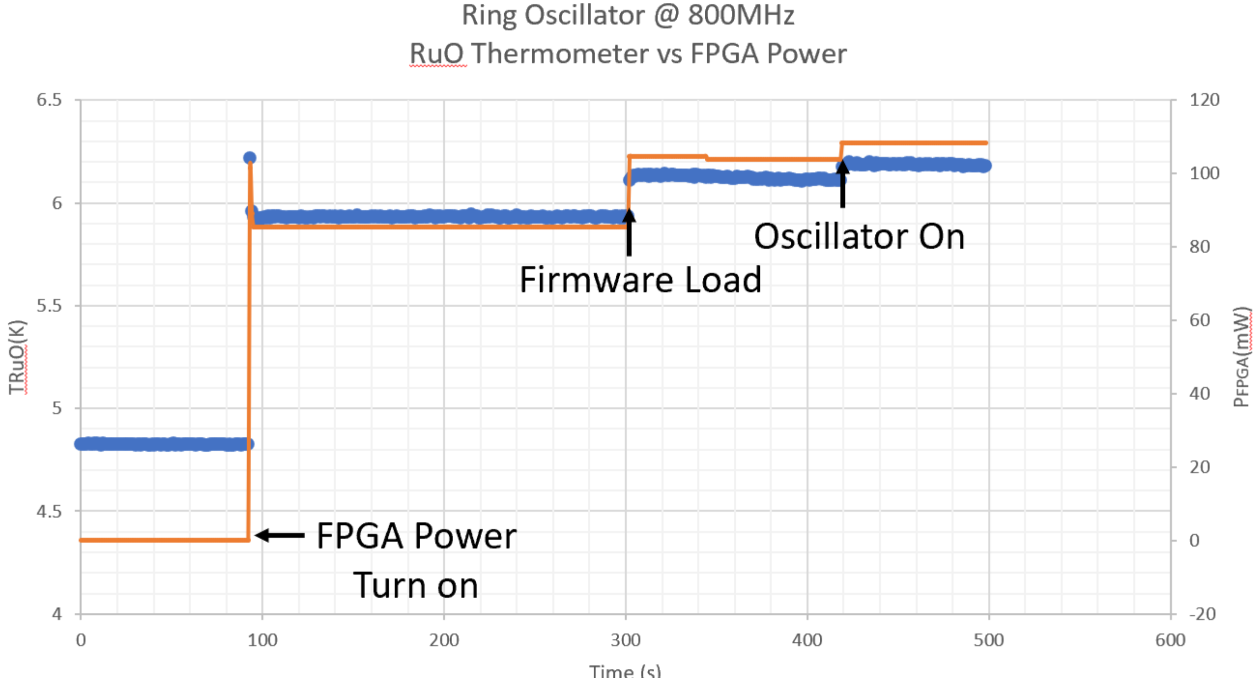


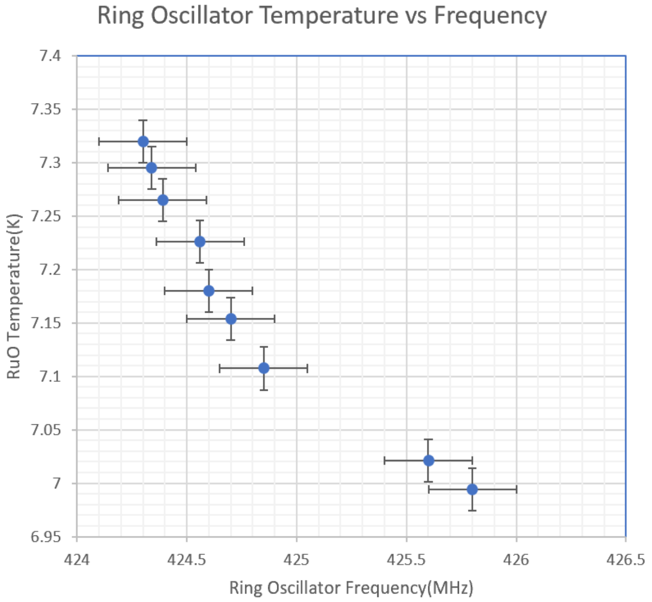



# INTERNAL TEST CIRCUIT: Ring Oscillator



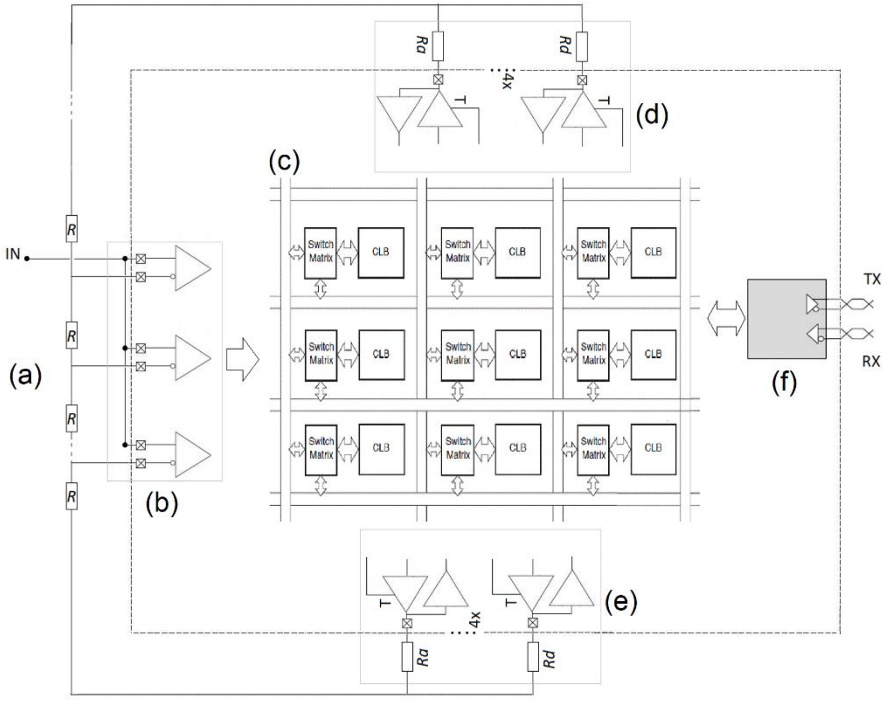



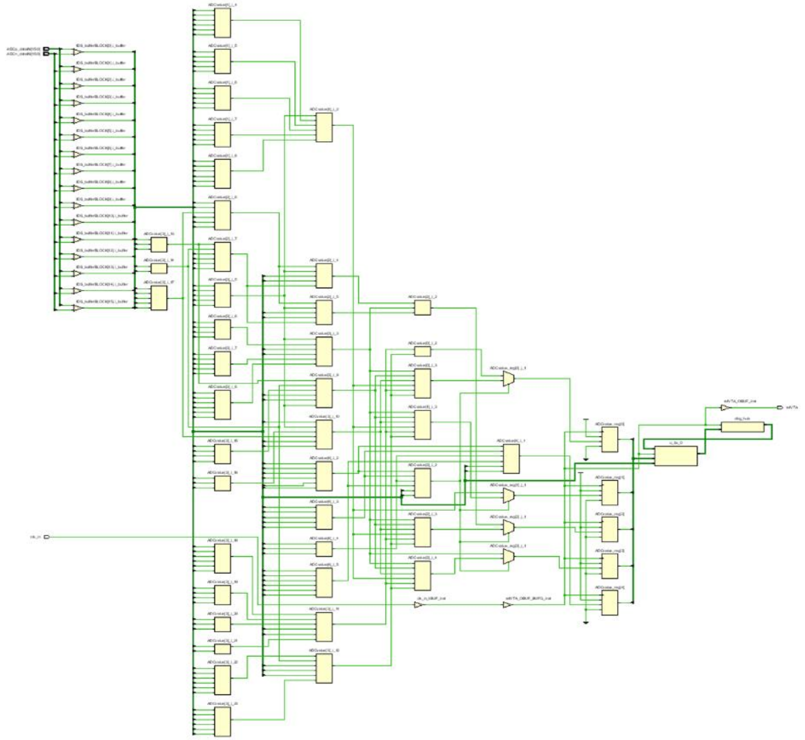




Seven stage ring oscillator

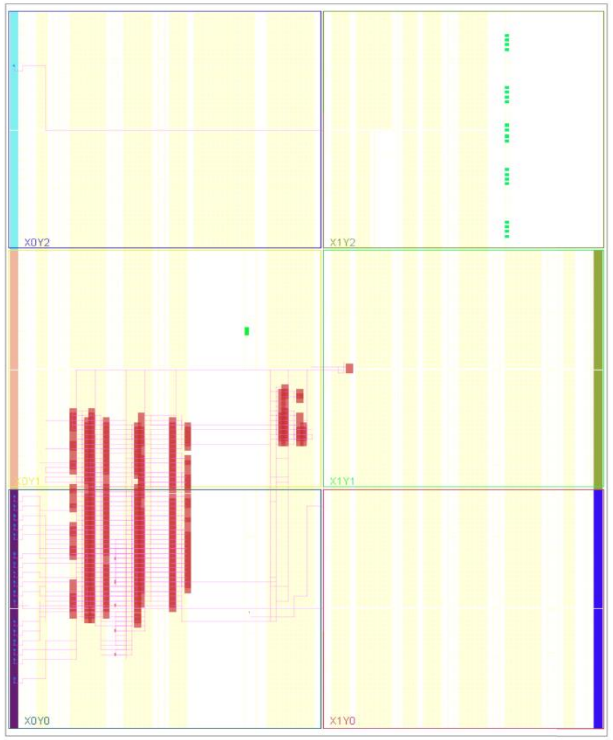
# 4b FLASH FOLDING ADC IMPLEMENTATION




Reconfigurable Flash Folding Architecture. With this architecture it is possible to change the ADC resolution on the fly.

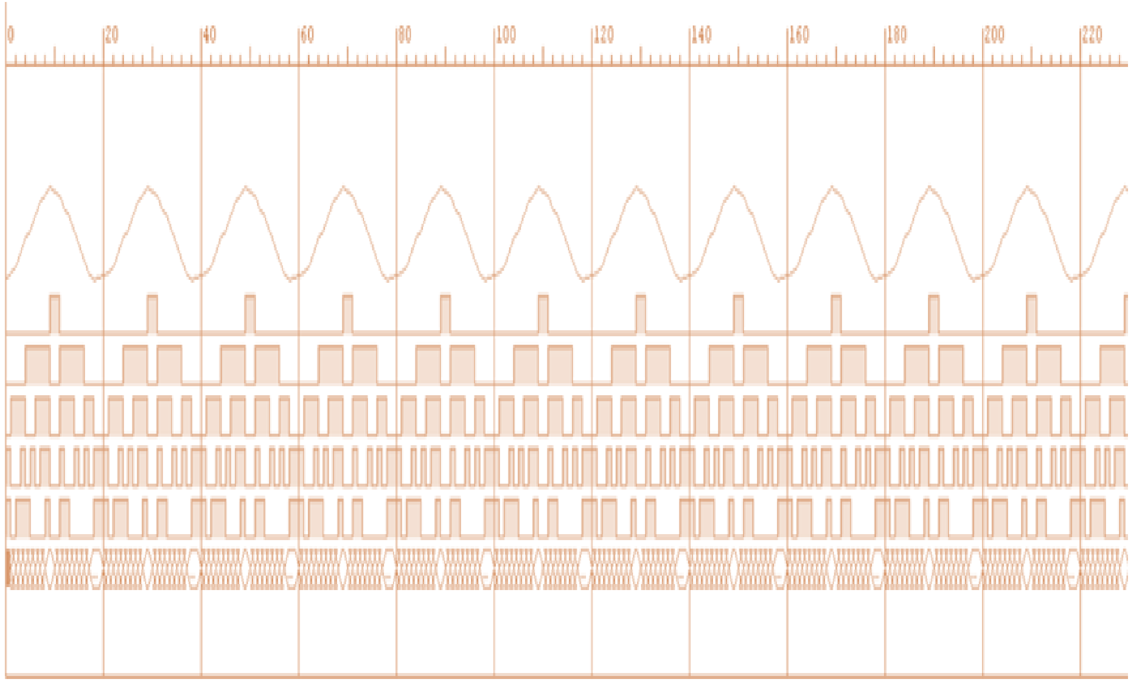


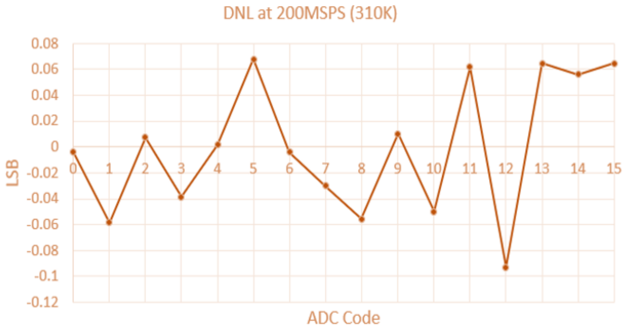
Logic implementation is based on LVDS buffers for discrimination, LUTs for decoding, and a Ring Oscillator for Clock.

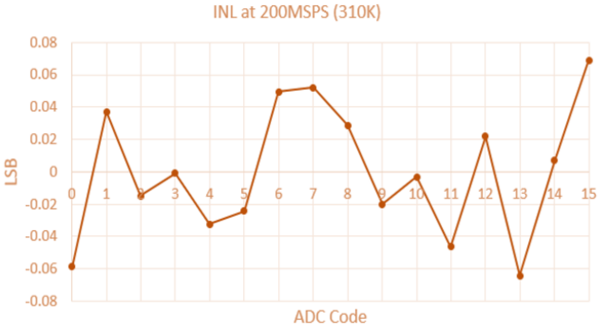


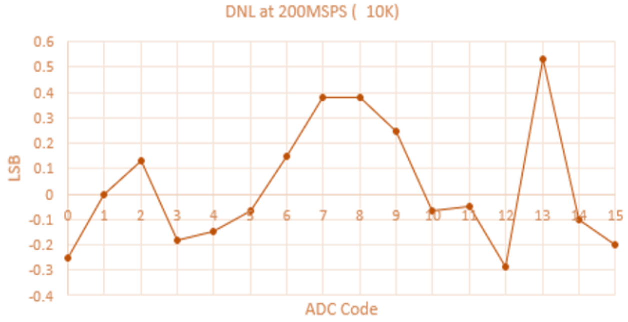

Implementation utilized under 15% of the FPGA logic resources.

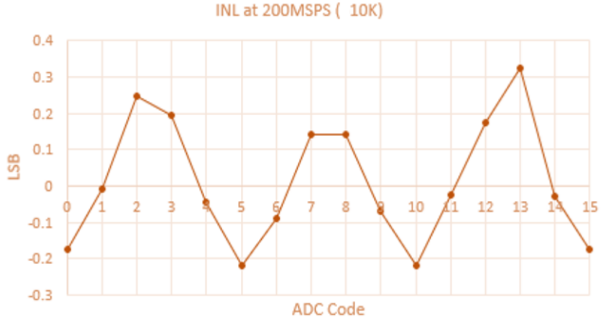
# 4b FLASH FOLDING ADC RESULTS



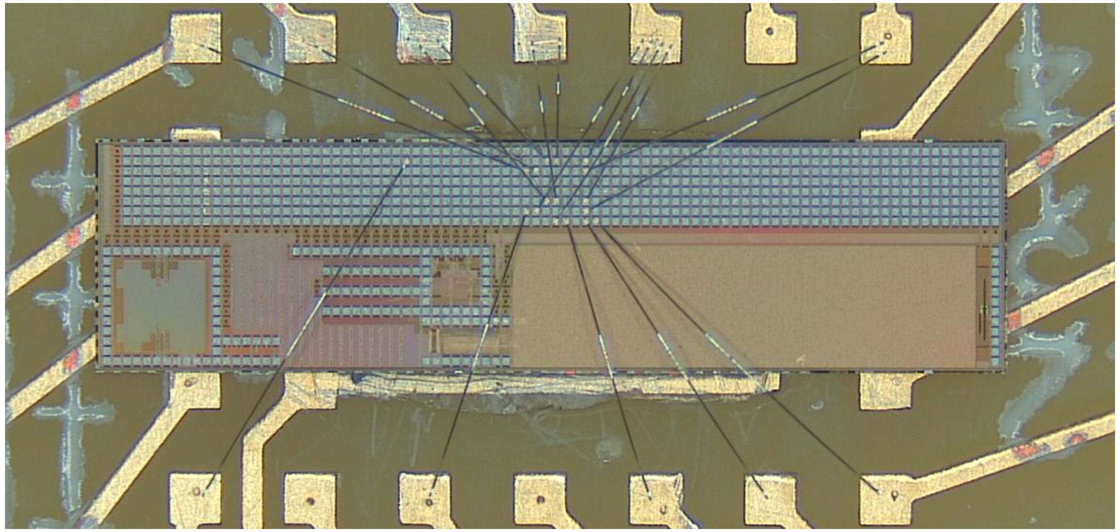



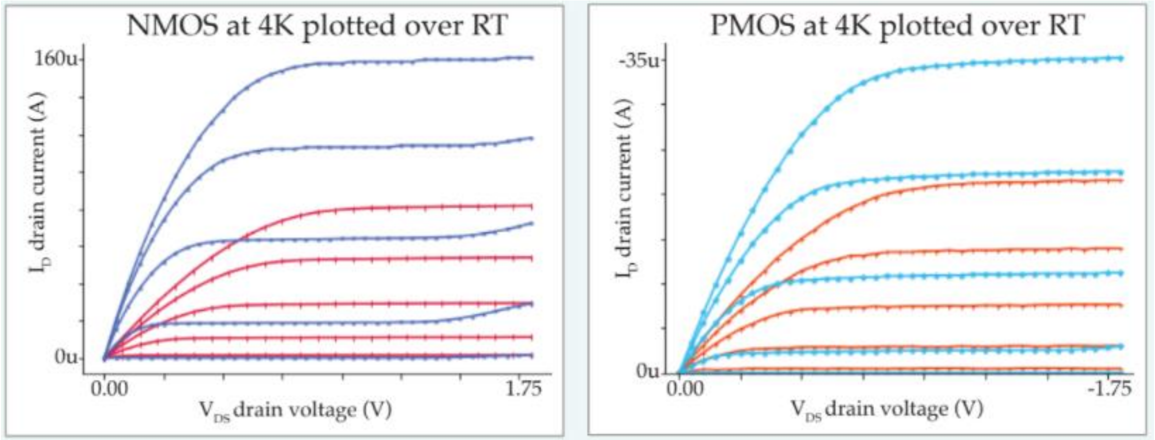



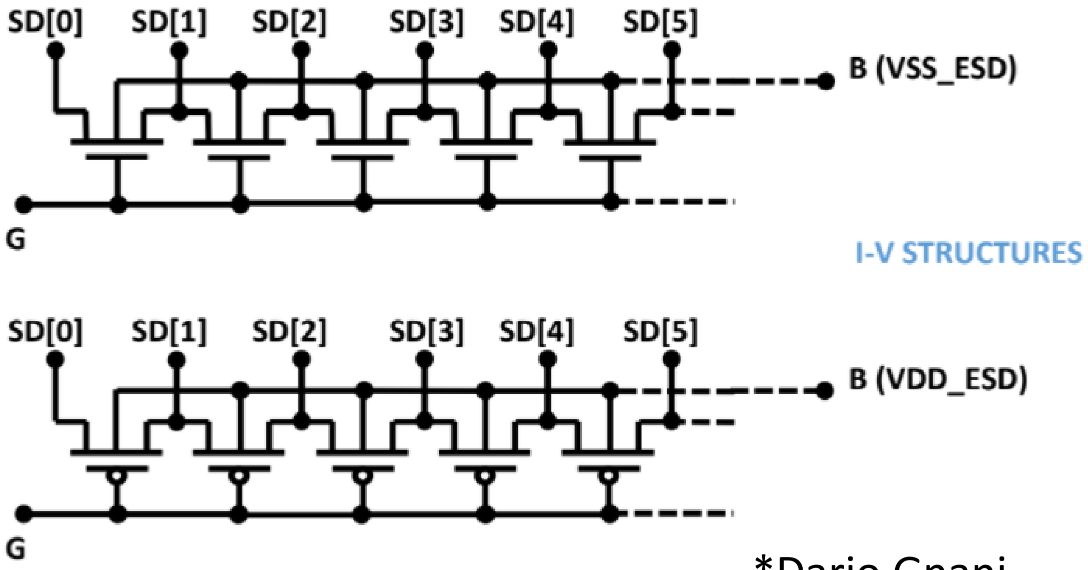

Digitization of a sine wave viewed through Chipscope. On top the reconstructed analog signal and in the bottom its digital makeup.

ADC noise performance at room temperature and at 10K. Notice that although thermal noise decreases with temperature the non-linearity actually increased.

# SEA-OF-TRANSISTORS



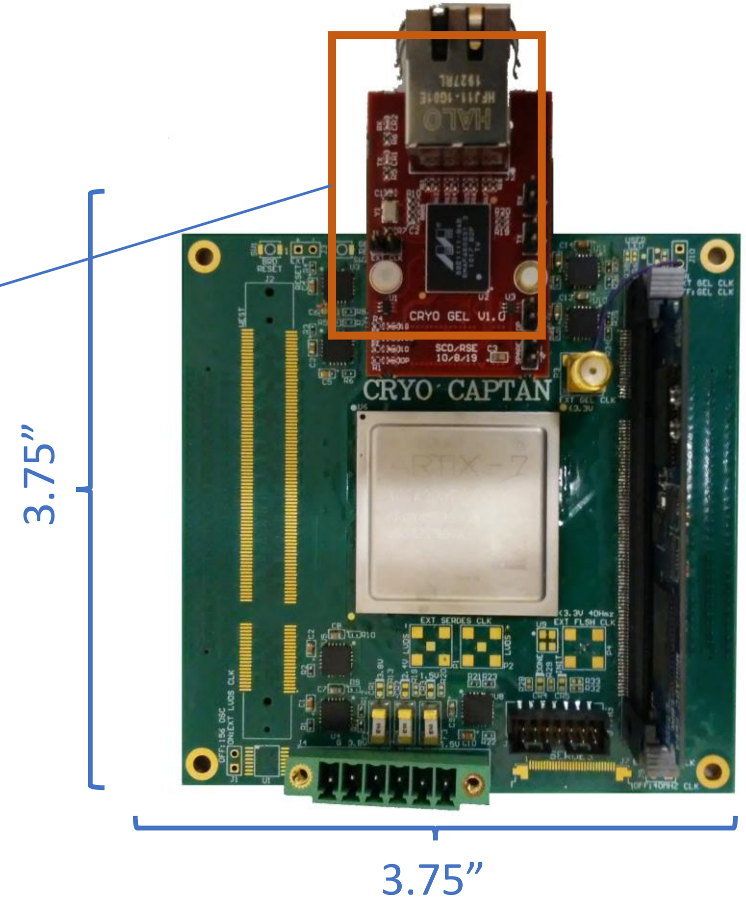



*Dario Gnani

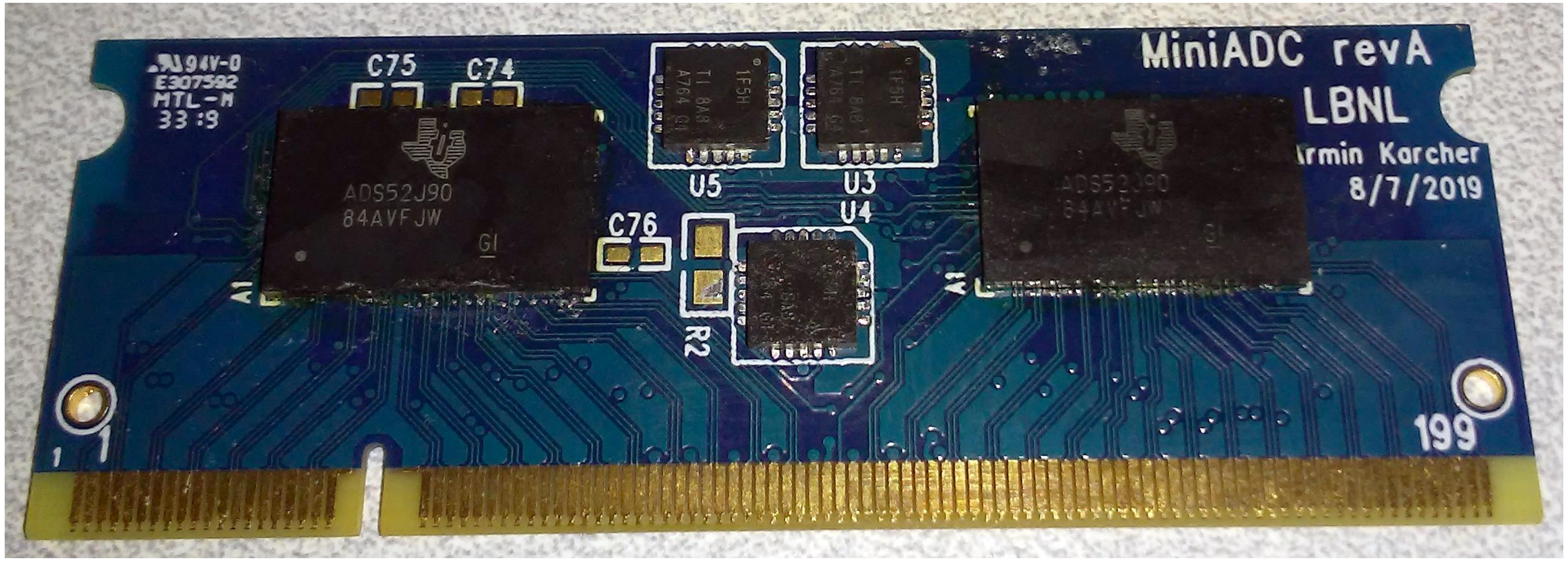
# CryoDAQ – LBNL-Fermilab

- Large Artix FPGA (28nm)
- 64 Analog channels
- External Clock
- Laser Driver for communications
- LDO’s
- External Clock
- Max operational clock 1GHz
- Expected around 1 W of power dissipation



# CryoDAQ ADC – LBNL-Fermilab

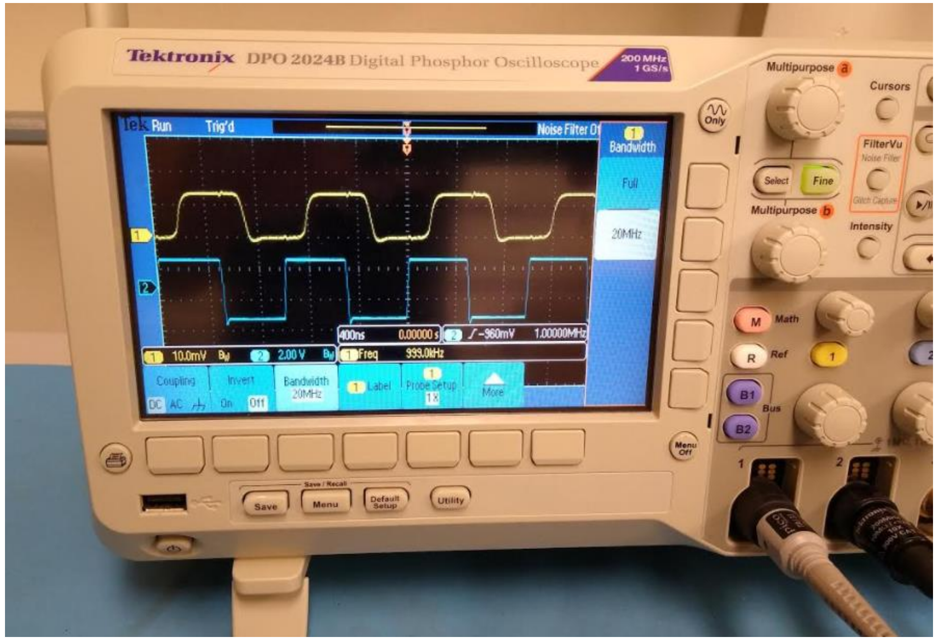
- 32 ADCs
- Sampling rate up to 100MSPS (50MHz signals)
- 14bits
- Not tested cold yet at LBNL



# CONNECTING COMPONENTS

POF Receiver

POF Under Test




LN - Blue TX, Yellow RX (1MHz)

POF Receiver – When cold requires the receiver voltage bias to be increased. Generally the transmitter needs to work on top of a higher light intensity. Clock speeds up to 100MHz are achievable with POF.