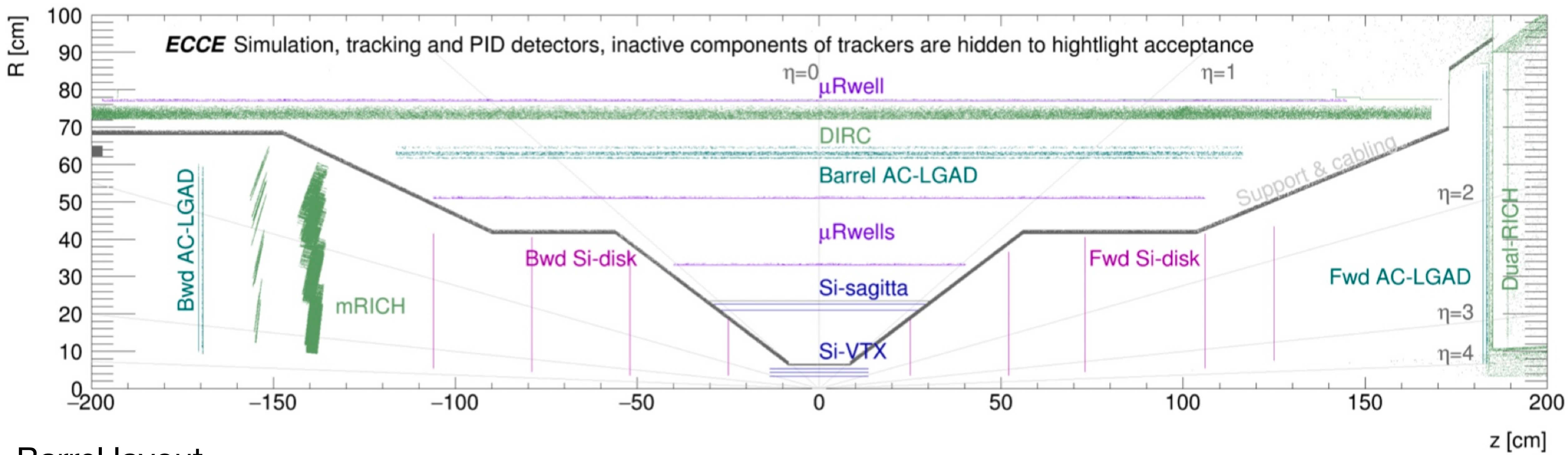


Optimizing EIC tracker configuration

Rey Cruz-Torres
RNC EIC Meeting
June 28th, 2022

Barrel

The ECCE configuration



Barrel layout

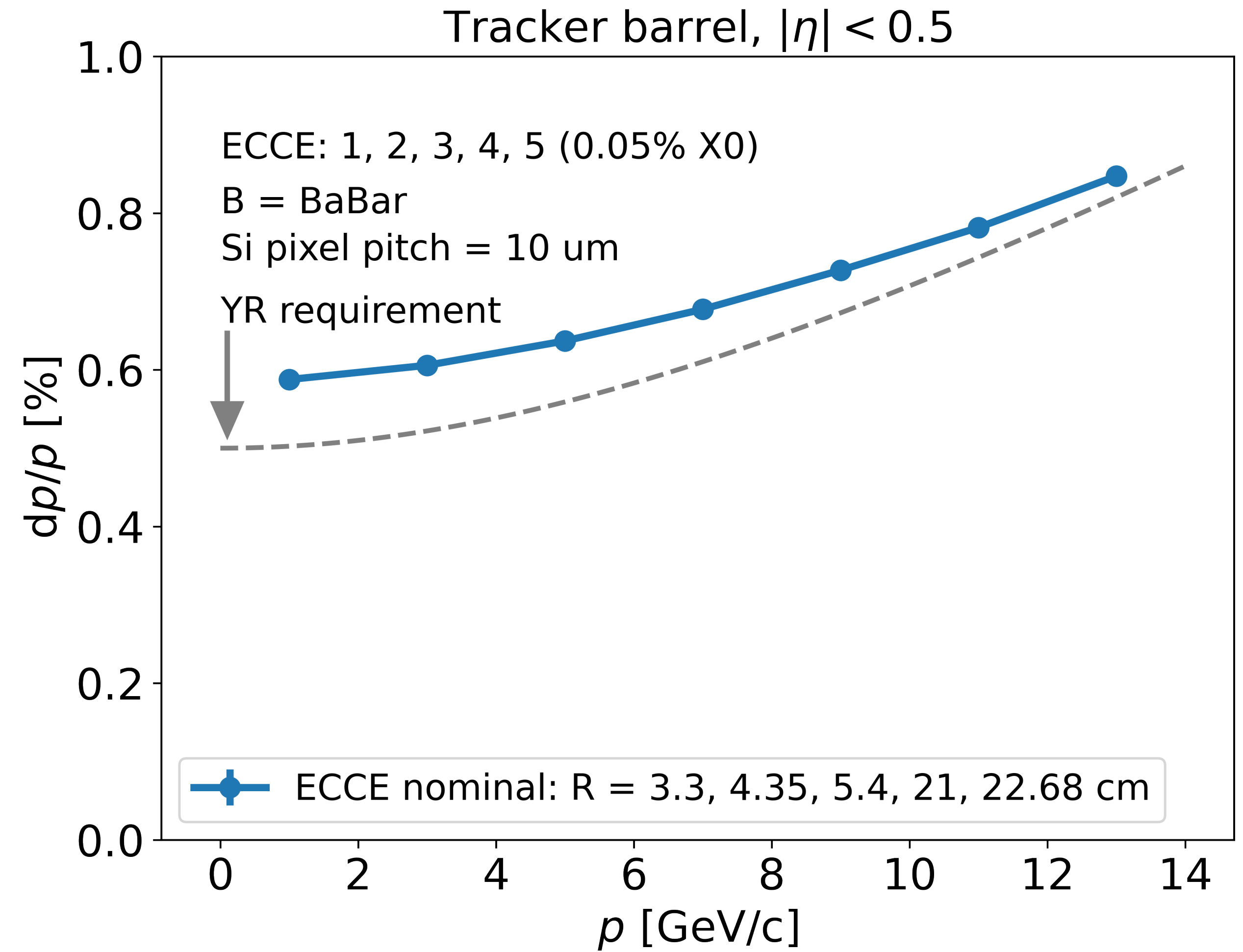
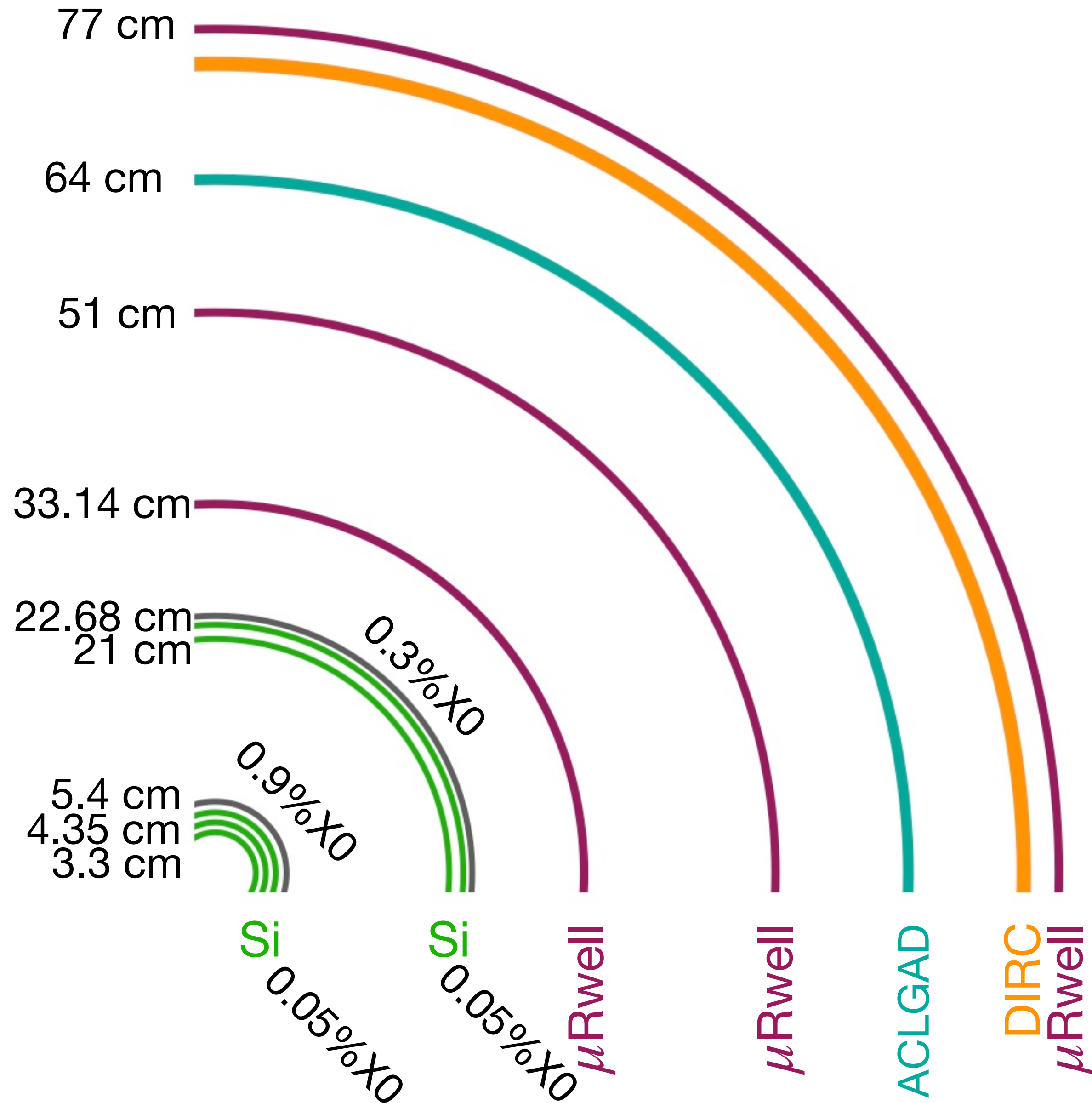
Si	r (cm)	length (cm)	X
1	3.3	27	0.05
2	4.35	27	0.05
3	5.4	27	0.05
4	21	54	0.05
5	22.68	58	0.05

	r (cm)	length (cm)	point res
uRwell1	33.14	80.16	55 um
uRwell1	51	212	55 um
ACLGAD	64	140	30 um
uRwell3	77.0175	342	55 um

Pitch = 10 um

And also two support cylinders:
- r = 6.3 cm, 0.9% X0
- r = 23.5 cm, 0.3% X0

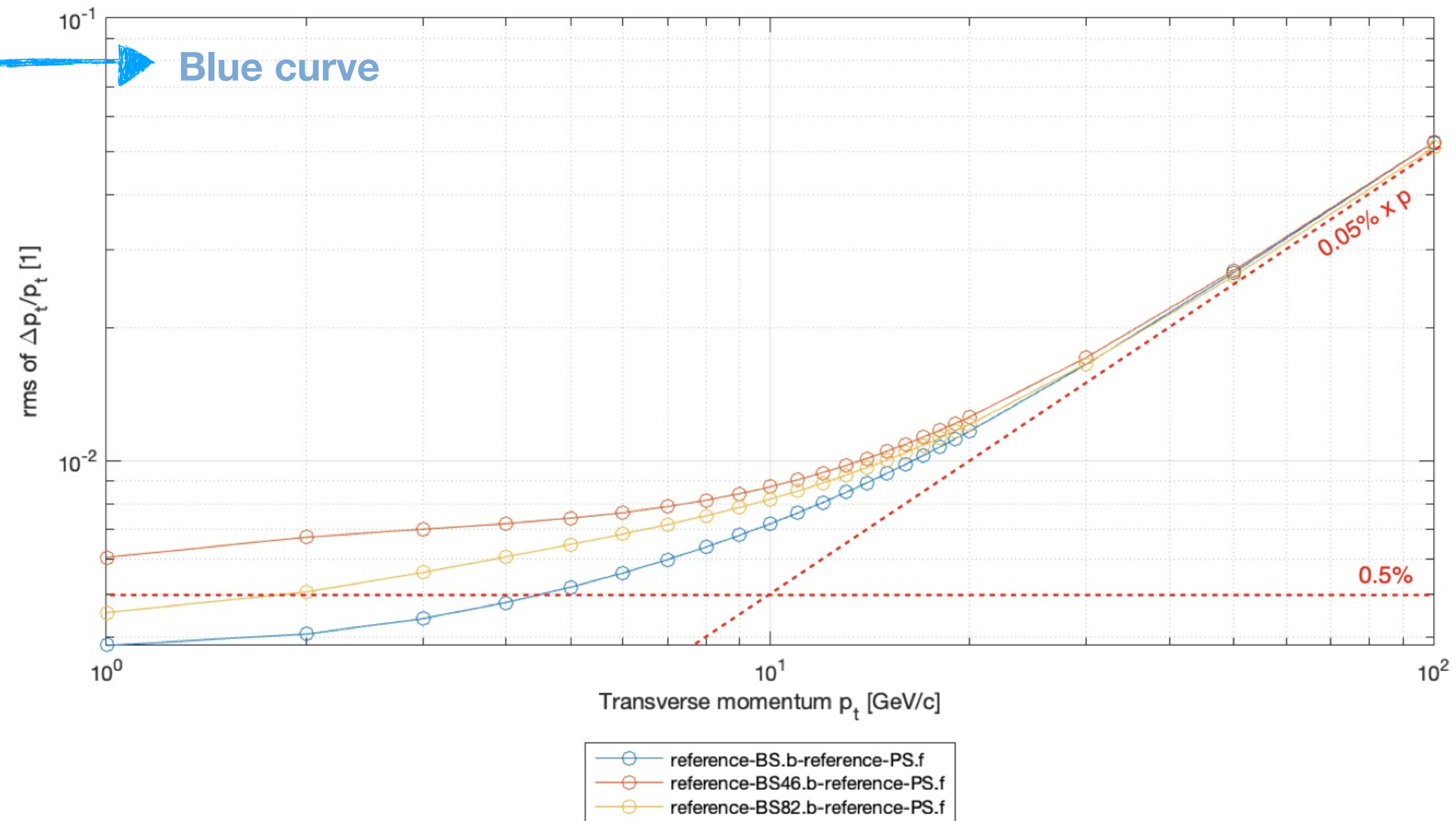
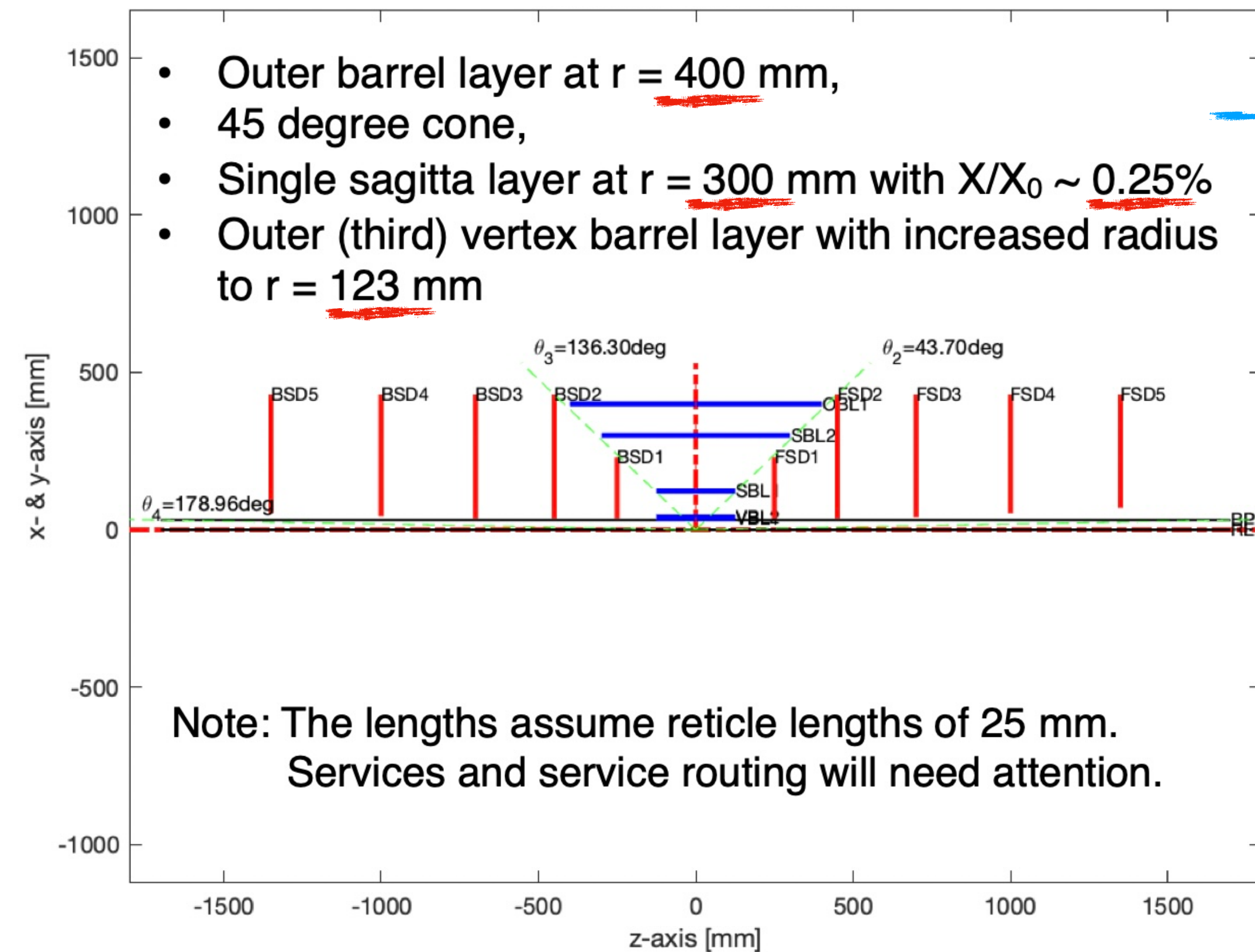
Momentum resolution performance of ECCE Barrel



Barrel optimization with fast simulations

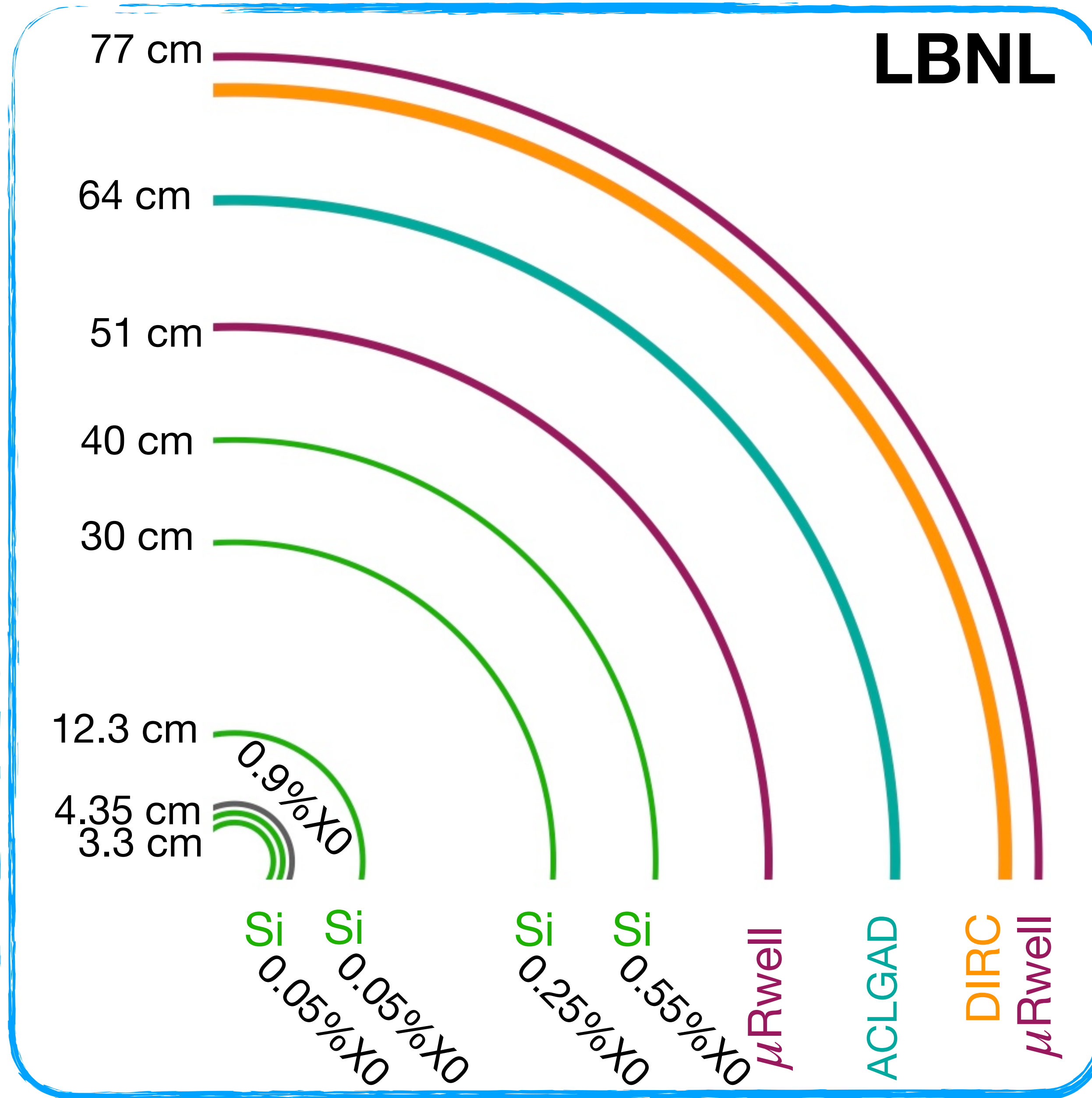
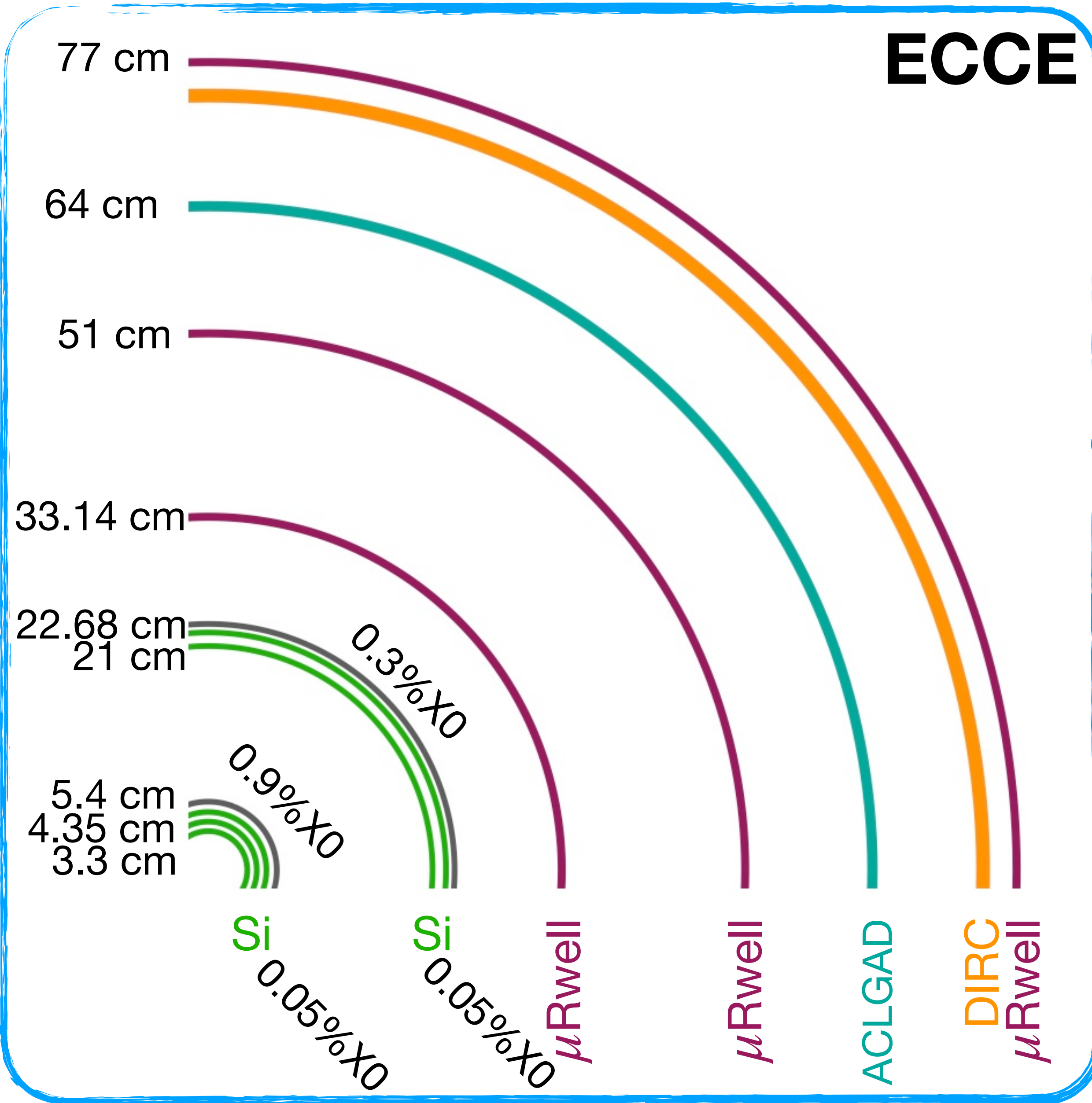
Work by E. Sichtermann

See slides from <https://conferences.lbl.gov/event/974/>

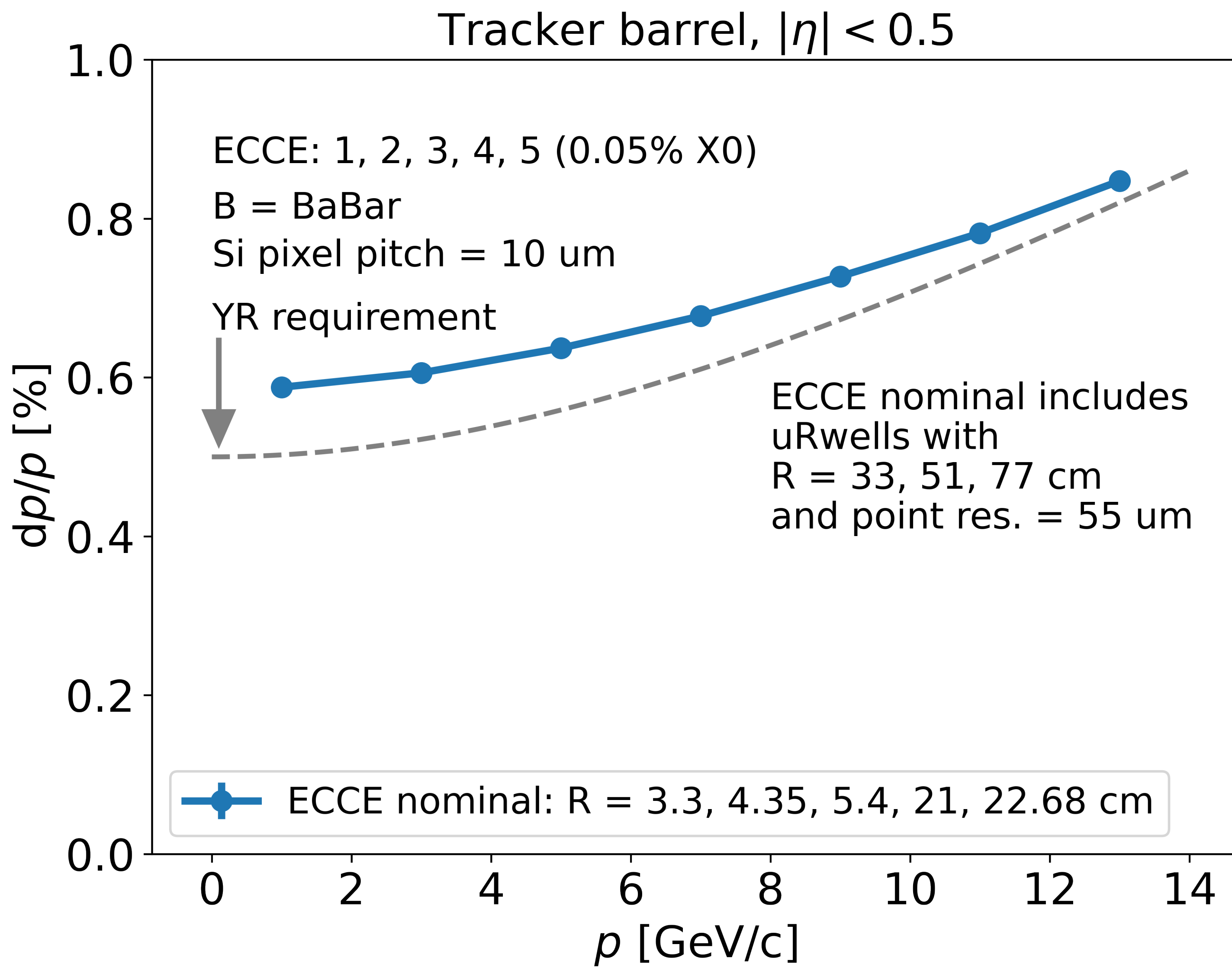


It seems sensible to simulate this in Fun4All already now, even though other changes will be needed. Volunteers ;-)?

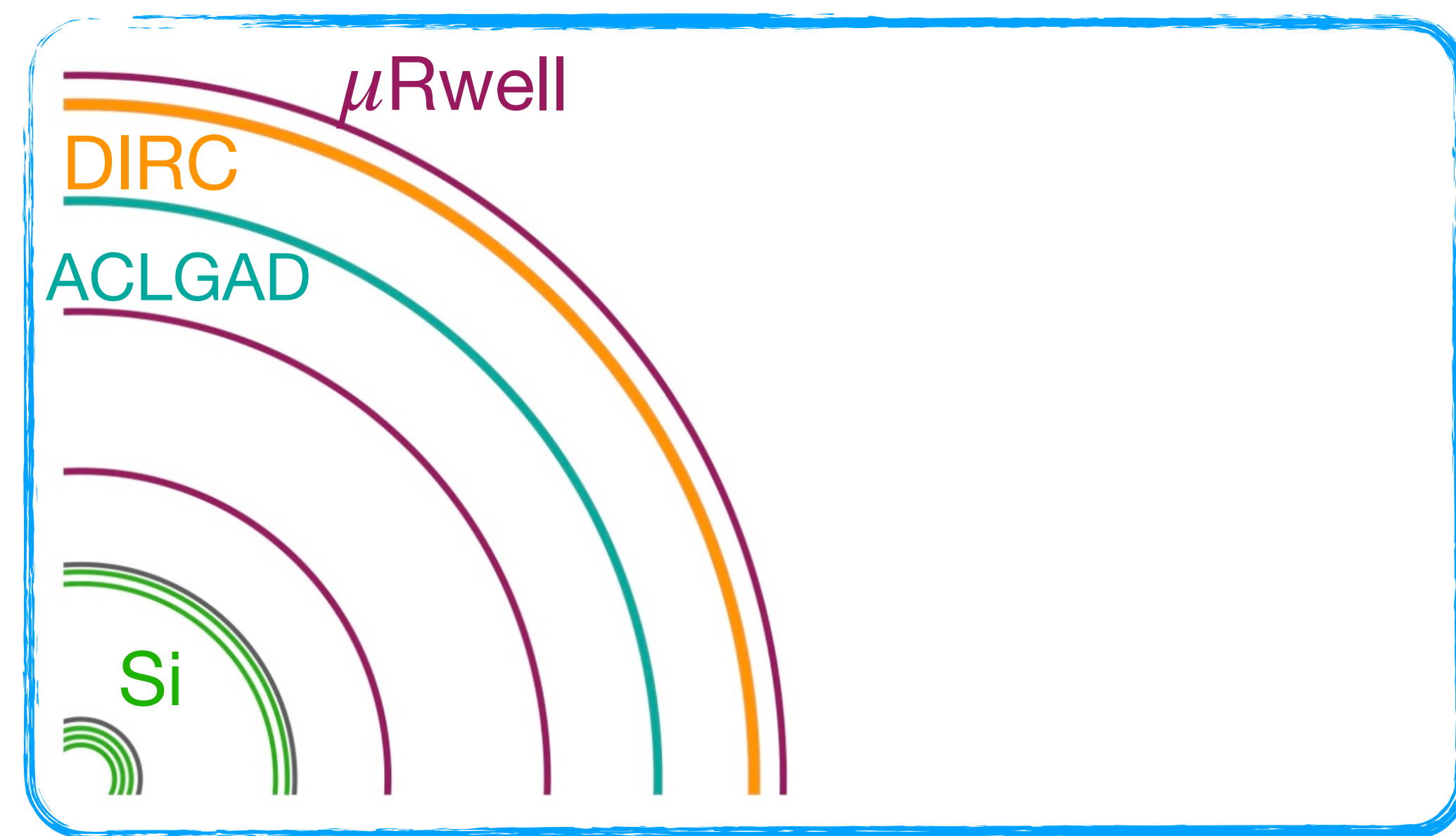
New proposed barrel configuration



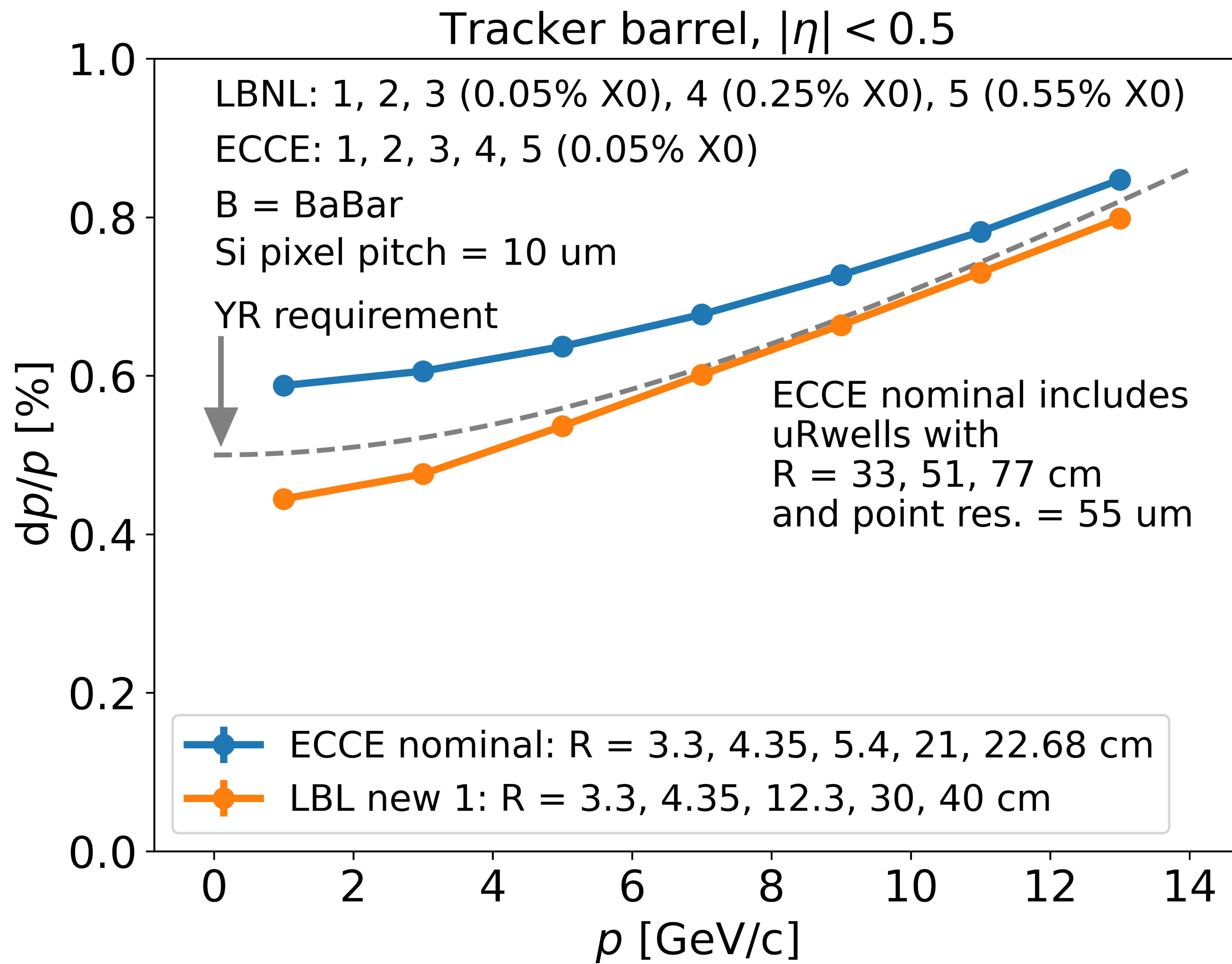
Momentum Resolution Performance



ECCE nominal configuration



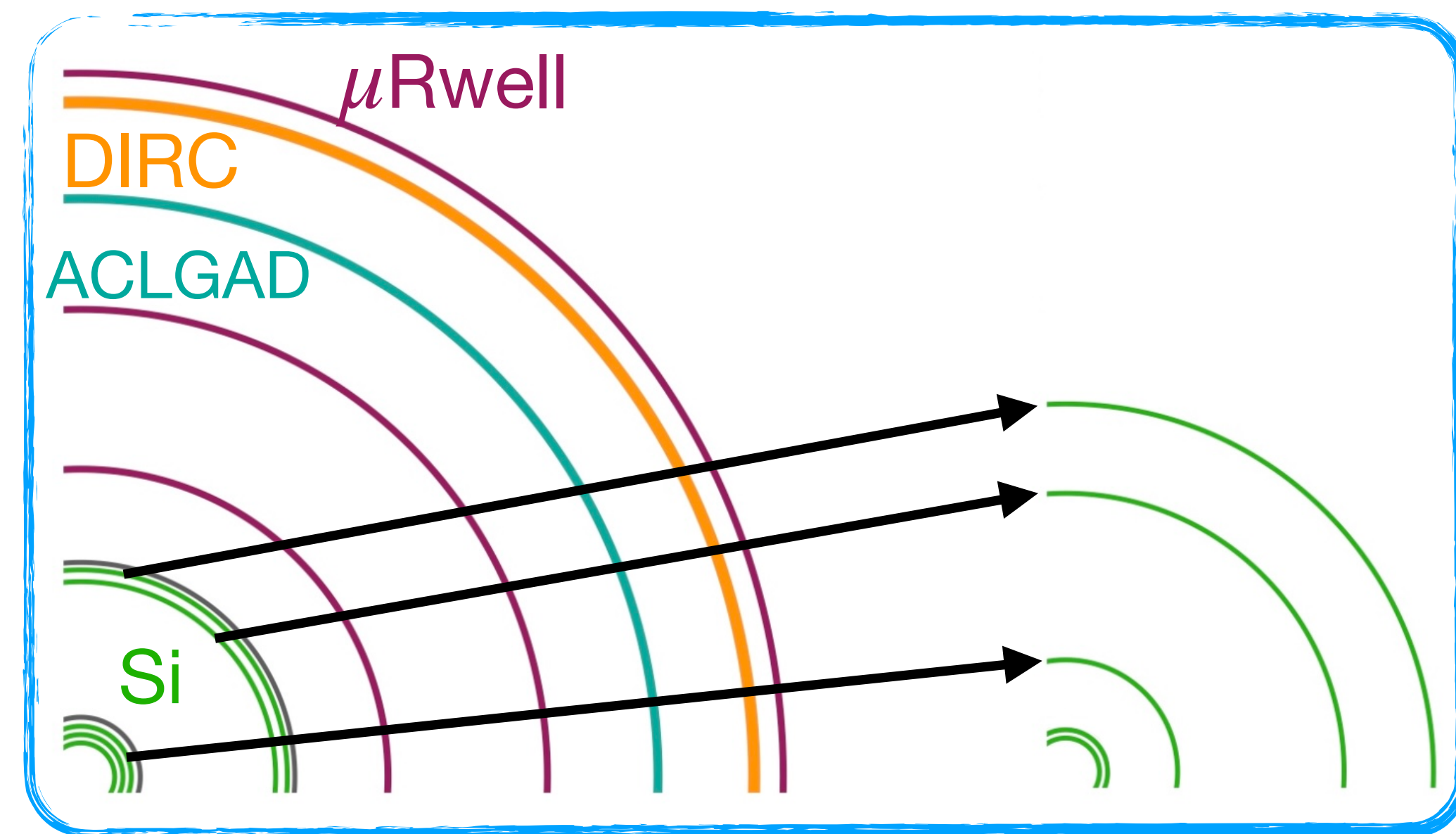
Momentum Resolution Performance



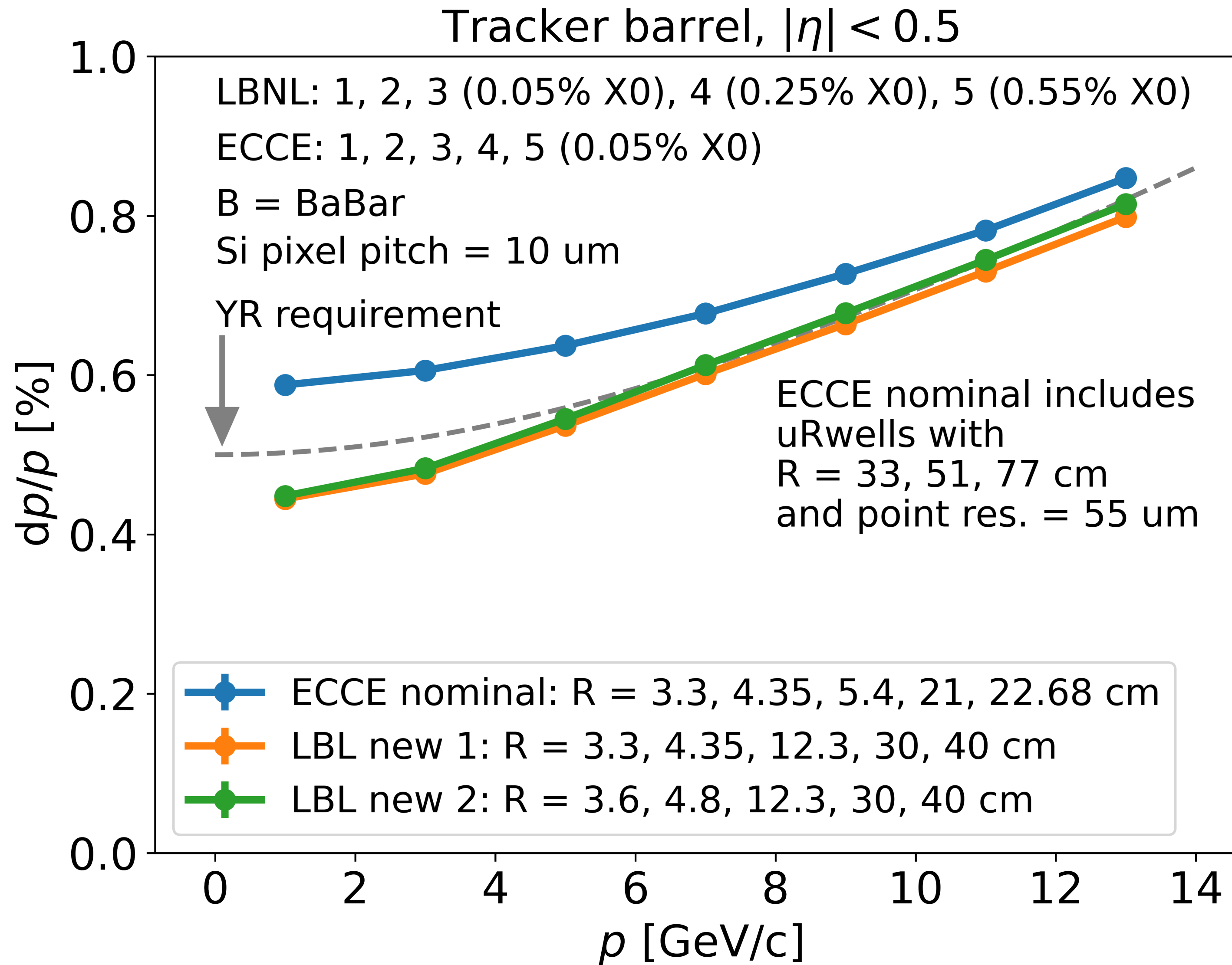
ECCE nominal configuration

LBL (Ernst's) configuration:

after increasing R of third vtx layer and sagitta layers (and changing X)



Momentum Resolution Performance



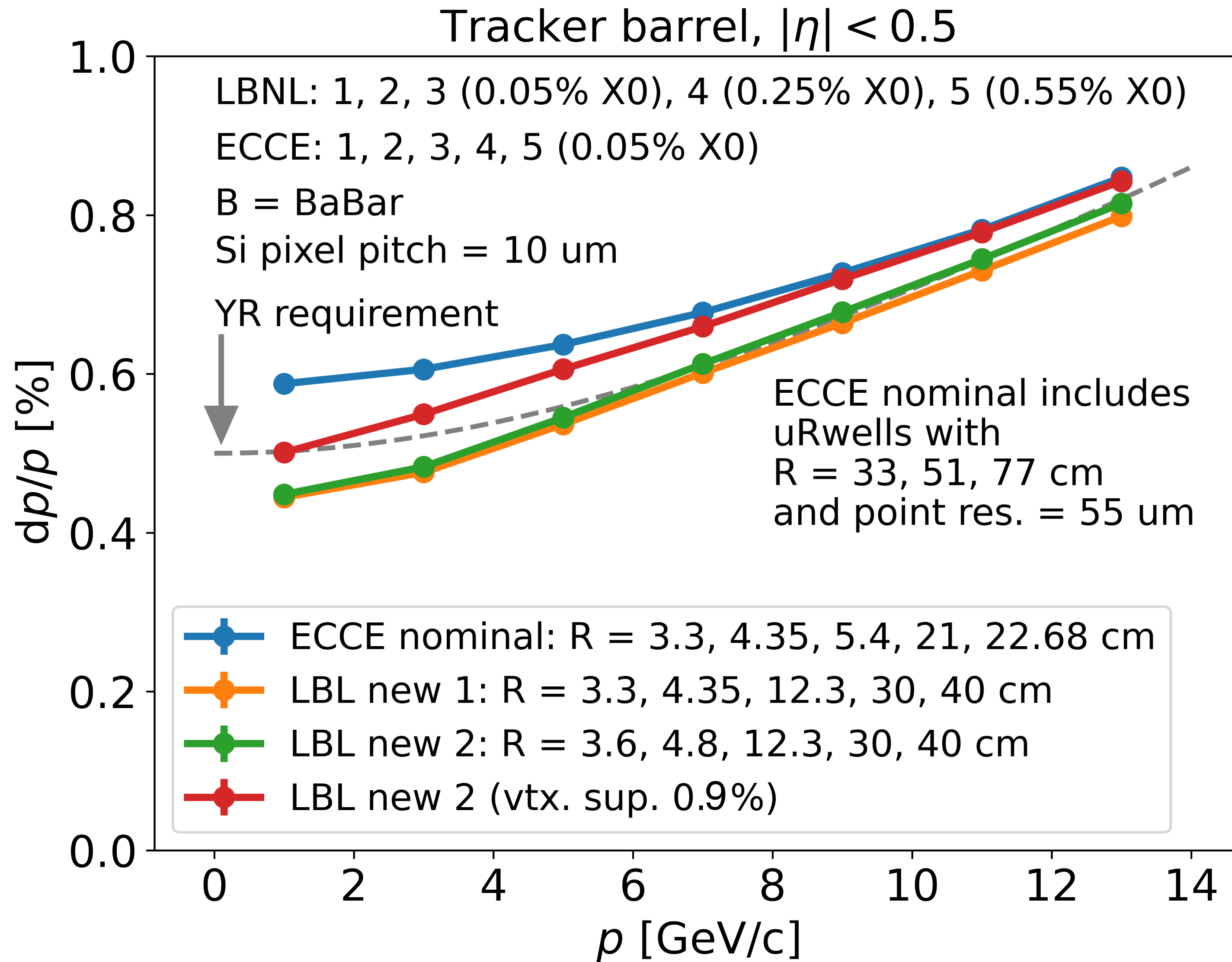
ECCE nominal configuration

LBL (Ernst's) configuration:

after increasing R of third vtx layer
and sagitta layers (and changing X)

after also increasing R of two
innermost vtx layers
(for beampipe bakeout)

Momentum Resolution Performance



ECCE nominal configuration

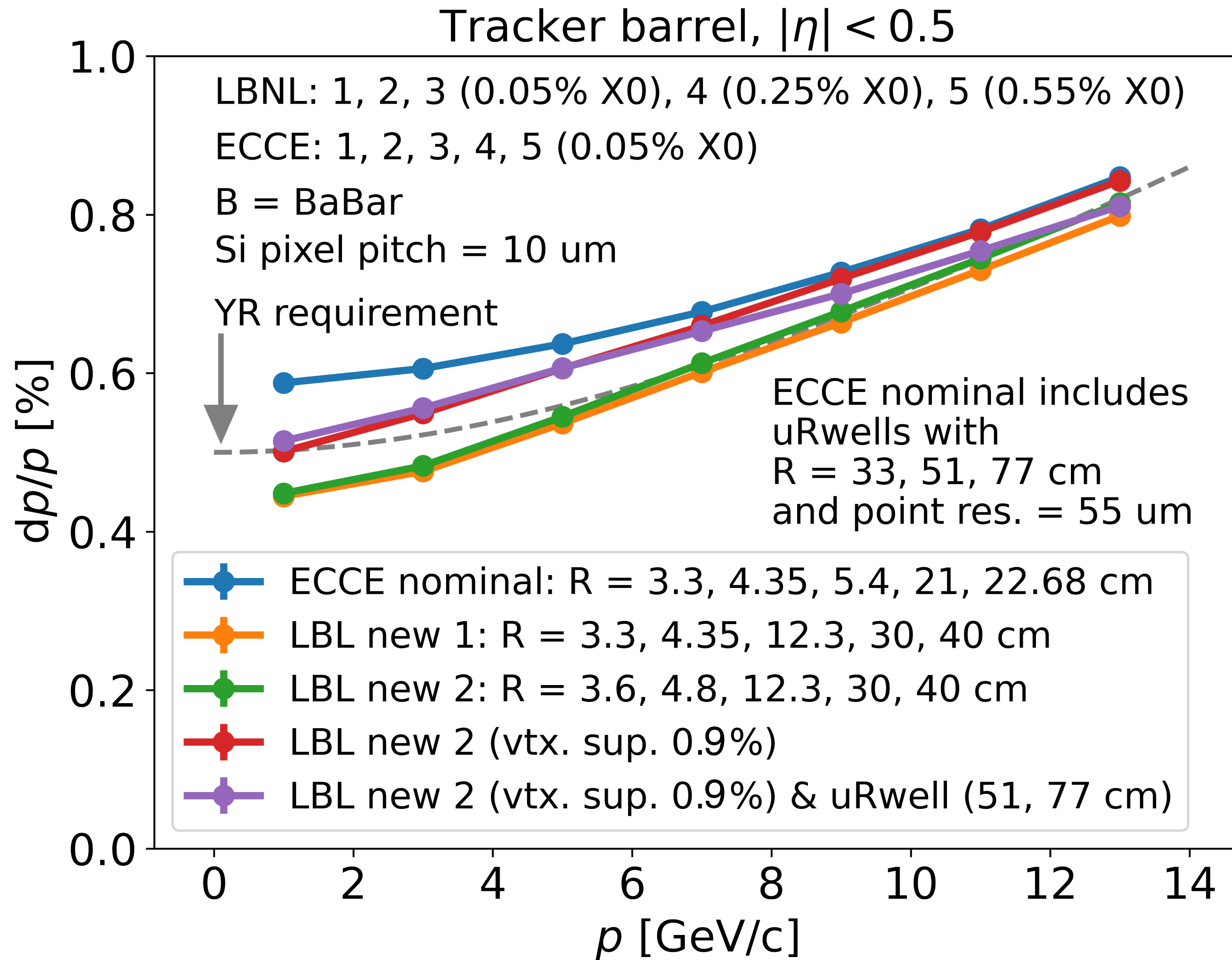
LBL (Ernst's) configuration:

after increasing R of third vtx layer
and sagitta layers (and changing X)

after also increasing R of two
innermost vtx layers
(for beampipe bakeout)

after adding 0.9% X0 cylinder
outside vtx layers

Momentum Resolution Performance



ECCE nominal configuration

LBL (Ernst's) configuration:

after increasing R of third vtx layer
and sagitta layers (and changing X)

after also increasing R of two
innermost vtx layers
(for beampipe bakeout)

after adding 0.9% X0 cylinder
outside vtx layers

after turning on outermost
two uRwells